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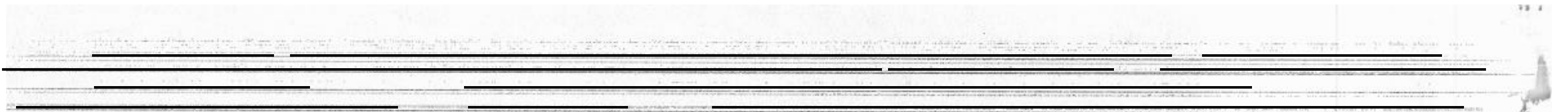
THE APPLICATION OF FAILURE ANALYSIS IN PROCURING AND SCREENING OF INTEGRATED CIRCUITS

by L. D. Hanley, J. Partridge
E. C. Hall

October 1965

MIT

CAMBRIDGE 39, MASSACHUSETTS



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GUIDANCE AND NAVIGATION

Approved: *[signature]* Date: 11/15/65
MILTON B. TRAGESER, DIRECTOR
APOLLO GUIDANCE AND NAVIGATION PROGRAM

Approved: *[signature]* Date: 11/16/65
ROGER B. WOODBURY, DEPUTY DIRECTOR
INSTRUMENTATION LABORATORY

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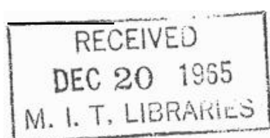
The publication of this report does not constitute approval by the National Aeronautics and Space Administration of the findings or the conclusions contained therein, It is published only for the exchange and stimulation of ideas.



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THE APPLICATION OF FAILURE ANALYSIS IN PROCURING AND SCREENTNG OF INTEGRATED CIRCUITS

ABSTRACT

The procedure for the testing, screening, and lot rejection of integrated circuits for the Apollo Guidance and Navigation computer is described. The procedure, based on a knowledge of failure modes failure mechanisms and contributing causes to failures in the manufacturing of devices, attempts to increase the reliability of integrated circuits. This is accomplished by screening and analyzing weak devices and using the generated data to quantitatively assess the lot for acceptance, rework or rejection. The technique, which is primarily aimed toward high-usage high-volume devices, was developed after extensive testing of many tens of thousands of integrated circuits. The process documents included in the appendix contain stress test procedures, classification of failure modes, numerical rejection limits per class of failure modes, internal visual rejection criteria, and leak test procedures.

To emphasize the need for the described technique data is presented showing variations among vendors and variation among procurement lots shipped from a single vendor, The contributing factors to the variations are discussed.

A discussion of the evolution of the process documents is presented. The ultimate goal of the documents is the elimination or minimization of detected failure modes. Failure studies have shown that some failure modes are screenable with high confidence whereas attempts to screen other types of failure modes merely decrease the life of the device. In the latter case, the detection during short term stressing of devices which exhibit long time dependent failure modes is a low probability event. After one-hundred-percent nondestructive testing, sample destructive testing, failure analysis and failure mode grouping the classes of failure modes in a lot are then weighted in accordance with

screenability and detectability. Failure of a lot to fall within the acceptable limits will instigate. action.. as to whether. the lot will be rescreened, resubmitted to tighter acceptable limits, or whether a portion of the lot or the entire lot will be rejected. The decision for lot or sublot rejection is based on the traceability of the nonscreenable failure modes to a critical manufacturing process. The approach presents a continuous monitoring procedure for qualification of parts and vendors, and creates an incentive on the part of the vendor to eliminate causes of failures.

by L. David Hanley
Jayne Partridge
Eldon C. Hall
October, 1965

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THE APPLICATION OF FAILURE ANALYSIS IN PROCURING AND SCREENING OF INTEGRATED CIRCUITS

INTRODUCTION

Small-sample stress testing as applied to device procurement has dubious application for systems with increased high reliability goals, As a result, one-hundred-percent nondestructive stress testing has become fashionable. Unfortunately, even the testing and stressing of entire lots, by itself, cannot assure the elimination of nonscreenable failures. In an attempt to fill in this gap, an approach will be presented using semiconductor integrated circuits as an example, whereby the frequency of field failures can be decreased beyond the point presently possible through one-hundred-percent testing alone This approach is based on the knowledge of failure modes, failure mechanisms, and contributing causes during device manufacturing, all of which can be applied to the screening and acceptance criteria of procurement lots, The technique was developed after extensive testing, data analysis, and failure analysis of integrated circuits.

There were two major factors which aided the study and development of the screening and lot acceptance procedures. One was the decision to use only one Nor gate, as shown in Fig, 1, for all logic functions in the Apollo Guidance and Navigation computers. This resulted in high volume procurement, an absolute necessity for establishing proven low failure rates of any new device in a short period of time, The second was the choice of an extremely simple circuit which aids an effective screening process. The accessibility of the circuit elements enables quick detection and diagnosing of insidious failures without extensive probing as required with more complicated circuit. For some failures, as for example those which are induced by surface conditions. it is desirable to be able to study the characteristics of the integrated circuit components without opening the package.

It became immediately obvious that small-sample stress testing could not guarantee that each purchased lot would meet the Apollo

integrated circuit failure rate requirements. The MIL-S- 19500D statistical sampling procedure was both not applicable nor practical.. Furthermore, as long as all failure modes were not completely screenable, one-hundred-percent screening alone was not sufficient to attain the required high reliability goals. A study of the various failure modes of integrated circuits created the dilemma whereby some of the failure modes were easily screened by standard screening techniques and others only occasionally detected. No assurance could be made with any reasonable confidence that the devices with these troublesome defects had been removed from the lot. To overcome this problem, lot acceptance criteria were established which would identify with high confidence those lots in which insidious failure modes were not prevalent and screening had been adequate. Providing an effective failure mode detection system, the procedure for lot acceptance is based on one-hundred-percent nondestructive tests and sample destructive testing. All the failures generated from the testing are completely analyzed. The failure modes are then classified by groups and compared to the acceptance criteria, It must be emphasized that the lot is accepted or rejected not only because of the number of failures but also on whether the failure modes generated were nonscreenable or insidious and long-time dependent.

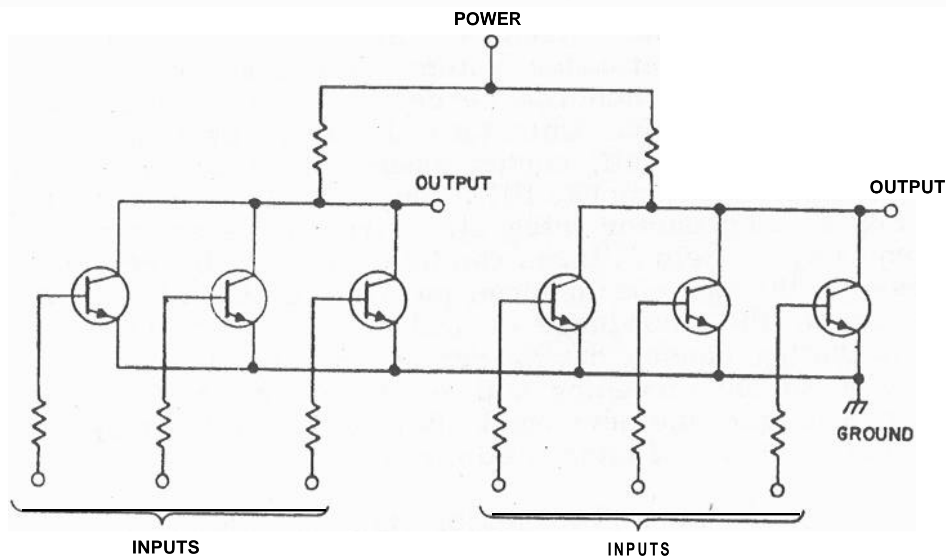

Figure 1

Schematic of the silicon monolithic dual three input nor gate.

VENDOR SELECTION & FLIGHT QUALIFICATION PROCEDURE

To assist the understanding of the lot acceptance procedures, a general discussion of the semiconductor part vendor selection and flight qualification procedures will be given as performed for the Apollo Guidance and Navigation computer.

The process begins with an assessment of the vendor's ability to supply devices, the institution of component standardization in designs, and the preliminary study of device failure modes. A block diagram of this preliminary evaluation which precludes any production procurement is given in Fig. 2. The qualification procurements which supply parts for the qualification testing and engineering evaluations established the manufacturer's device processing. One of the indirect results of the initial procurements is the early detection of new failure modes. The conclusions of the failure analyses are then fed back to the manufacturer who in turn attempts corrective action. This cyclic procedure is continued until the most obvious problems have been eliminated. Additionally, the early detected failure modes coupled with past experience are utilized to design the qualification testing.

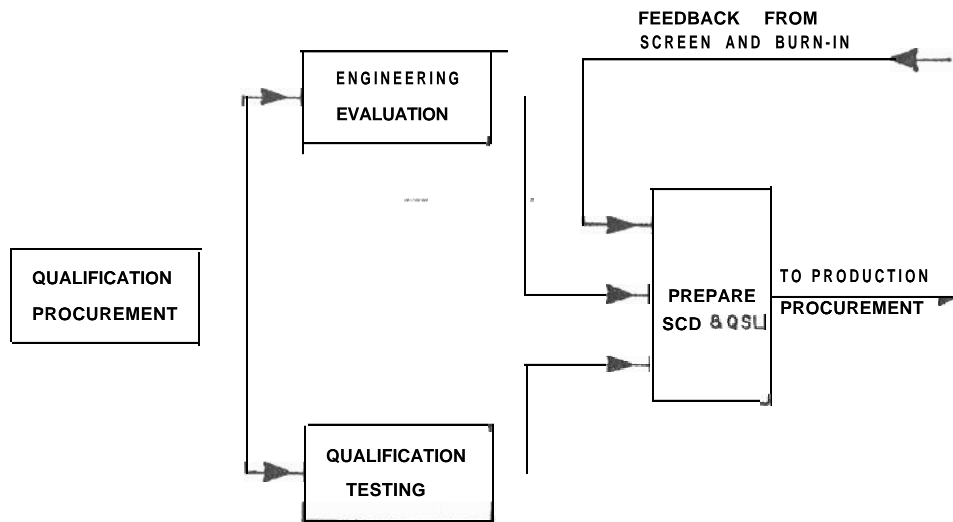

Figure 2

Block diagram of the vendor selection procedure.

The formalized qualification testing begins when the vendors have supplied devices representative of their finalizedmanufacturing process. It is extremely important that all qualification and engineering testing be performed on devices fabricated from the identical process used to supply computer production devices. The qualification tests subject the devices fromvarious vendors to the extremes of and, to a limited extent, beyond usage conditions in an attempt to detect failure modes which could occur in normal applications.

The engineering evaluations are performed simultaneously with the qualification procedures to determine device speed, fanout capabilities, noise immunity, and operating temperature range. From this evaluation, the optimum computer design is developed. It is at this time that tests are conducted to determine the electrical parameters which will insure proper device operation in every usage mode and to establish the logical design rules for the computer.

The qualification and engineering evaluations determine those vendors who are capable of supplying the semiconductor part and who do not exhibit any gross reliability problems. The qualification tests alone are insufficient to determine the ability of a vendor to control his process but large-volume production procurement data fed back from screen and burn-in supplies extensive vendor history.

Utilizing the data generated during the engineering evaluations and qualification tests, the specification control document (SCD) is prepared. The SCD is the document to which production parts are bought. Based on the qualification by vendors, the qualified suppliers list (QSL) is formed which specifies the vendors from whom the production parts shall be procured.

Once the SCD and QSL have been released, production procurement may begin. Figure 3 pictures the general flow of parts and data as required for flight qualification. The devices procured by lots proceed through the screen and burn-in (S&BI) test sequence.

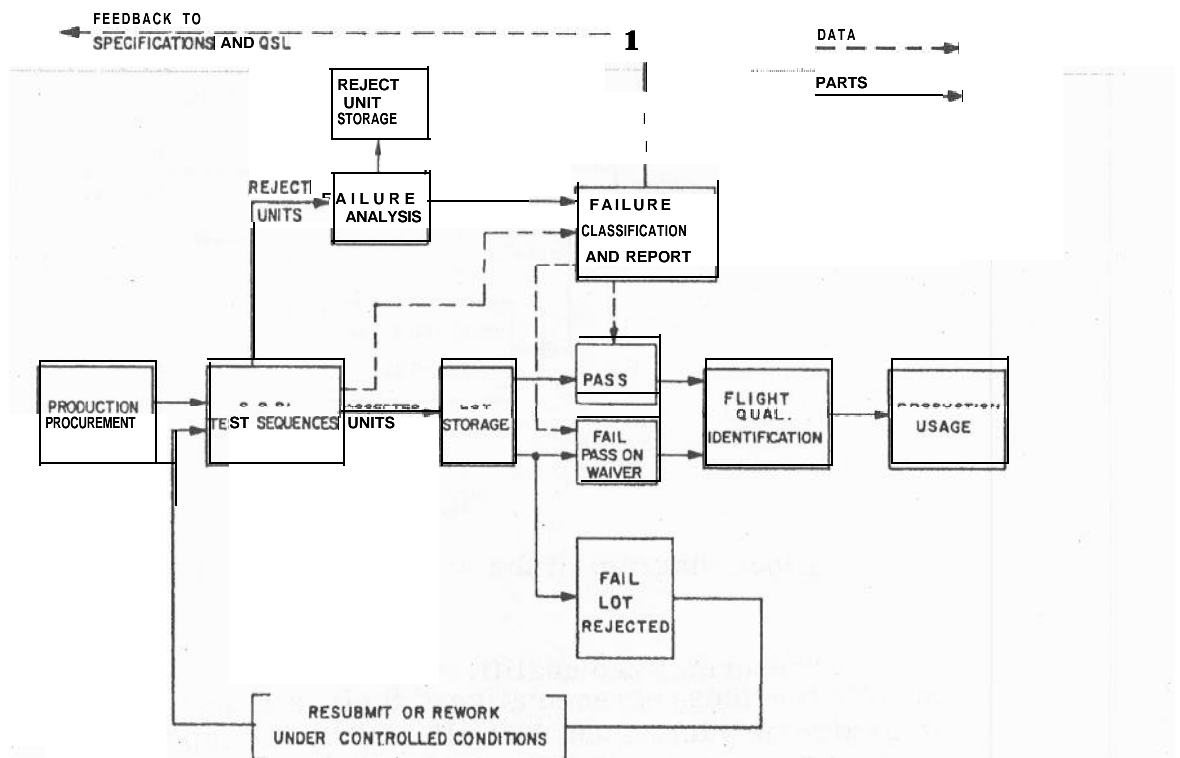

Figure 3

Block diagram of the flight qualification procedure.

Upon completion of screen and burn-in the lot is stored until failure analysis is completed. All failed units are catalogued, analyzed,

and. classified to complete the lot assessment, followed by a written report. If the lot passed, all the devices that passed all tests can be identified as a flight qualified part with a new part number and sent for productionusage, Only the semiconductor part with the flight qualification part number can be used in flight qualified computer assemblies. From failure analysis, rejected parts proceed to reject storage where they will be available for future study if required.. In the event that the lot failed because of circumstances not completely defined through failure classification, the lot can be flight qualified by waiver. The waiver must be authorized by NASA and will accompany the computer. In certain limited cases, parts from a failed lot may be resubmitted for rescreening.

The accumulated data from the screen and burn-in procedure and failure analysis are utilized to further evaluate the vendor production capability and his device quality and reliability.. This in turn affects a vendor's continued status as a qualified supplier.

LOT ACCEPTANCE SPECIFICATIONS

The specifications which control the implementation of the process described; in Fig.. 3. for the dual Nor gate, are given in the appendix. These documents will be briefly described to summarize the salient features,

A. ND 1002248

The Apollo Guidance and Navigation Specification, ND 1002-248, is the central document on which each procured lot qualification is based. This document specifies the procedures required for lot acceptance resulting in flight qualified parts. In particular, ND 1002248, specifies the details of:

1. The operational and environmental stress test procedures and sequence commonly referred to as the screen and burn-in procedure. The screen and burn-in procedurewas designed to detect failure modes which could occur during the normal stress and environmental application of the device.

2. The electrical parameter tests to be performed during the screen and burn-in procedure, The tests as defined were determined during the engineering evaluation and were chosen to detect failures and assure proper computer operation,

3, Definitions of failures. Failures have been defined as catastrophic, several categories of non-catastrophic, induced, and inspection failures,

4. Allocation of failures, The conditions are defined for removal from the screen and burn-in procedure of failures which are to be forwarded to failure analysis.

5. Classes of failure modes.. Failure modes are classified according to screenability' and detectability. This

classification will be discussed in detail in a later section.

6. Maximum acceptable number of failures per class of failure mode for all 100% electrical parameter test stations

7. Maximum acceptable number of failures for nonelectrical tests and all sample electrical parameter tests,

8. The report required for each flight qualified lot. The report must contain the complete history of the lot with the specific data and analysis required for flight qualification.

9. Data and failed parts storage. In order to assure traceability and future analysis should field failures occur, the conditions of data and failed parts storage are given.

10. Contractual requirements to implement lot qualification.

B] ND 1002257

The Apollo Guidance and Navigation specification, ND 1002-257, defines the rejection criteria for internal visual inspection of silicon monolithic integrated circuits. This specification was included in the appendix because of the affect of the criteria on lot acceptance, ND 1002257 serves a dual purpose in that it is applied by the device manufacturer during a one-hundred-percent preseal inspection for removal of defective parts, and by the customer on a sample basis as a destructive test for lot acceptance, Some of the problems in a lot may only be detected by destructive internal visual inspection. Certain failure modes can only be observed after the sealedand branded device has been exposed to operational and environmental stresses,

The internal visual inspection criteria were defined after most, if not all, of the failure modes of silicon monolithic integrated circuits were determined, No device is rejected merely on the basis of aesthetics. Devices are rejected only when a fault which contributes to a known, potential failure may be visually observed. The rejection criteria of ND 1002257 do not attempt to reject all of thevisually observed faults contributing to failure, because of the difficulty of precisely or quantitatively defining faults which are subject toindividual interpretation, It has been our approach that ultimate reliability will be improved by rejecting to major, easily observed defects rather than by rejecting to a long complicated list of qualitatively defined defects,

C] ND 1002246

The Apollo Guidance and Navigation Specification, ND 1002-246, which was written after a series of correlation tests, states the

procedures for leak testing of flat packages, It was determined that ~-the standard -fine and- gross leak--tests are insufficient for detecting the entire range of leakers for all flat package designs, This specification was included because lack of adequate hermeticity abets some of the insidious time-dependent failure modes,

FAILURE MODE CLASSIFICATION AND ACCEPTANCE NUMBERS

The essence of the lot acceptance procedures as specified in ND 1002248 is contained in the classification of failure modes and associated acceptance numbers. Although any failure which occurs in a critically highly reliable system is undesirable, failure modes may be grouped in accordance with available methods of elimination, A previous report[1] lists the failure modes, detected in silicon monolithic integrated circuits along with some contributing causes and stress dependencies. Anupdated list of the detected failure modes is given in ND 1002248, section 4.2.2. These failure modes which were generated after one-hundred-percent testing may be classified in the following manner:

1. Special Cases of Noncatastrophic Failures (Group 0)

These include devices which do not meet the electrical specifications at incoming electrical tests, devices which drift out of the electrical specification limits during stress testing but do not exceed a given percentage drift, and devices whichnever exceed the electrical specification limits during stress testing but which exceed a given percentage drift. These failures do not necessarily impede computer operation,

2. Screenable Failure Modes (Group I)

The contributing causes and stress dependencies of these failure modes are sufficiently well known so that the failure modes are screenable to a high confidence through electrical and stress testing.

3. Nonscreenable but Detectable Failure Modes (Group II)

Failure modes which are classified in this manner usually exhibit intermittency, serious surface problems, or require severe stressing for screenability. These failure modes are not screenable at normal, nondestructive stress levels, but are generally detected in finite amounts at normal, nondestructive stress levels if they are insidious within the lot.

4. Nonscreenable Difficult-to-Detect Failure Modes (Group III)

These failure modes are generally long accumulative time dependent at nondestructive stress levels, As a result, detection of such failure modes during short-term nondestructive testing becomes a low probability event. Also placed in this category are failure modes which are nonelectrically detectable, as for example, a chip detached from the header where the header does not provide electrical contact and the bonds or lead wires are not broken,

5. New Failure Modes or Failure of Unknown Causes (Group IV)

If such failure modes occur, studies must be performed to determine the screenability and the destructive effects of the various stress tests.

The failure mode classifications described above were listed by groups in order of decreasing screenability and detectability. Table I of ND 1002248, section 4.2.3, gives the maximum allowable percent failures for each failure mode classification for each lot processed through screen and burn-in. As the degree of screenability and detectability decreases, the failuremode classification is more heavily penalized, The Group II and III failure modes are more heavily penalized after the incoming electrical test, because it is of mor'e concern when these devices fail after they were known. to be good. Note that a maximum limit is still placed on the screenable failure modes. This is done for two reasons. First, one can never be one-hundred-percent confident that all potential failures have been eliminated. Second, the limit sets a guard against a multiplicity of failure modes which is indicative of poor workmanship and sloppy control. The limits set on the Group 0 failure modes are, in general, a guard against careless testing.

The percentages of Table I were based on a screen and burn-in study of over 200,000 Nor gates. Lots which have not passed the limits of Table I have exhibited reliability problems predicted by the results of screen and burn-in and failure analysis.

Table II of ND 1002248, gives the limits of the leak tests and sample tests of the screen and burn-in procedure. Theoretically, package leaks are screenable, but the limits guard against poorly executed leak test procedures, All the sample tests performed, with the exception of the emitter-base back bias and physical dimensions tests, are considered destructive. The additional handling required by the shock and vibrations testing have induced failures in the flat package. The emitter-base back bias test which is performed to detect surface instabilities will indicate the surface problems of the entire lot. Although the limit set on the internal visual inspection appears loose, the limit reflects problems in interpretation and subjectivity.

METHODS OF LOT REJECTION AND ACCEPTANCE

Because the provisions of ND 1002248 do not explicitly define, at this time, the various methods of possible lot rejection, a discussion will be presented here,

1. Lot Rejection

Any large lot of a semiconductor device fabricated from a continuously operating production line does not necessarily consist of homogeneous product and is certainly a function of start-to-finish yield. However, there are some failure modes which when detected are known to be prevalent in the entire lot. An example of such a failure mode is interconnect corrosion which is caused primarily by the presence of excess oxygen and moisture although thinning of metalizationand heat areaggravants. The primary causes of this failure mode are usually traced to improper wash and dry techniques

of the unsealed assembled device, device storage and device sealing. Another example requiring lot rejection are failure modes due to surface instabilities. Surface problems depend on the variabilities of most of semiconductor processing and, if not eliminated, are known to be prevalent in many lots of semiconductor devices Lot rejection is necessitatedwhen failure modes whose causes originate in the production line affect the entire lot.

2. Sublot Rejection

Since each lot of integrated circuit Nor gates is composed of many diffusion lots, sublot rejection is possible if failure modes are related to the diffusion sublots, and traceability is maintained after dicing and subsequent assembly. It is the intent of ND 1002248 to reject devices with-the possibility of insidious failure modes and accept devices with excellent reliability potential, The assumption that sublots are handled nearly identically implies that if one unit exhibits insidious or long-time dependent failure mode, many undetected devices will contain that failure potential. Failure modes whose causes originate in the variations of diffusion, oxidation metalization, and etching may not be insidious in all diffusion lots'. Examples of such, failure modes are contained in Section 4.2.2 of ND 1002248 and are al, b3, b8, c2, and c4.

3. Rescreen and Rework

Some of the listed failure modes are amenable to rescreen by the stressing which triggers or selects out failures. Most of these failure modes are generally in the Group 0 and Group I category. If this resubmittal procedure is applied, tighter acceptable limits should be met.

There are also certain applicable screen procedures which are not part of the screen and burn-in procedure because of their lack of universal application, or their effectivity or lack of destructivity have not been proven. For example, x-raying of TO-47 package integrated circuits has shown to be an excellent screen procedure for excess lead length and leads shorting to one another. However, the technique is useless for devices which employ aluminum leads, (aluminum is transparent to x-rays) and the applicability to flat packages has not been proven.

As effective nondestructive screen procedures are developed, use of such procedures on an individual or universal basis may be instituted,

4. Waivers

Since no specification is perfect, unforeseen contingencies of the specification may cause lots to fail for reasons other than device faults and poor stressing procedures, In these events, waivers become necessary.

VARIATION AMONG MANUFACTURERS AND LOTS

The previous sections have dealt with a description of the system incorporating the lot acceptance procedure by failure modes, Data will now be presented indicating the need for such an acceptance procedure because of the variations among manufacturers and lots of a single manufacturer.

Table I is a summary of reliability data accumulated up to October 1964 for the single Nor gate in a TO-47 package. This data has been previously discussed in detail.1 The data is presented here to show the extreme differences in reliability performance among manufacturers. The screenand burn-in procedure is as described in ND 1002248 except that Y2 centrifuge, emitter-base back bias, vibration, and shock testing were-not performed, The electrical failure definitions during screen and burn-in were any inoperable devices or any device exceeding the electrical specifications. The percentages include approximately 0.05 to 0.1% combined induced failures and testing errors. The initial qualification results are also included in Table I where the failure definition was an inoperable device. The extreme differences among the manufacturers is also reflected in the failure modes generated during both the initial qualification and screen and burn-in. For the data in Table I Manufacturer A rarely exhibited the nonscreenable, and/or long-time dependent failure modes while both Manufacturers B and C consistently did. The inoperable failures generated at computer use conditions for Manufacturers B and C were of the nonscreenable, long-time dependent failure modes.

VENDOR	INITIAL QUALIFICATION % FAILURES	SCREEN & BURN-IN % FAILURES		FAILURE RATES AT USE CONDITIONS 90% CONFIDENCE
		TOTAL *	POST STRESS * *	
A	5	1.8	0.3	0.005%/10^3 hrs (0 FAILURES)
B	26	3.8	1.7	0.3%/10^3 hrs (2 FAILURES)
C	58	5.0	2.5	1.8%/10^3 hn (26 FAILURES)

* TOTAL = ALL ELECTRICAL AND MECHANICAL FAILURES

* * ELECTRICAL FAILURES AFTER INCOMING ELECTRICAL TESTS

TABLE I

A summary of vendor reliability evaluation.

It is interesting to note that the same devices used to generate the data of Vendor A of Table I have since exhibited a failure rate of 0.0018%/10^3 hours at 90% confidence as of 30 August 1965 with no operational failures. The same devices of Vendors B and C have not improved their failure rates because additional failures have occured.

The data of Table I once again points out the fact that there are differences in the 'quality and reliability of devices produced among different manufacturers. Even though the general technical procedures of designing and building semiconductor devices are well known throughout the industry, the approaches to production control, problem detection and elimination, and process refinement varies widely among manufacturers. It is necessary for a qualified manufacturer not only to minimize the number of failures but also to maintain process control such that a multiplicity of failure modes does not occur, and long-time dependent failure modes do not exist, If it is not the ultimate goal of a manufacturer to design and build reliability into his device, effective improvement can never be realized through device evaluation, stress testing and quality control,

The more subtle differences in quality and reliability may be observed invariations of lots shipped from one manufacturer. The data of Fig. 4 indicates the numerical variations for the single Nor gate in a TO-47 package from one qualified manufacturer. Here, only the inoperable failures are plotted and induced failures and testing errors have been eliminated from the data., These single Nor gates were exposed to the screen and burn-in procedure as -described in ND IO02248 except that Y2 centrifuge, emitter-base back bias, vibration and shock testing were not performed. Each point represents a shipment lot of 2000 to 5000 .Nor gates. Figure 4a shows the percent catastrophic failures at the incoming electrical tests. Figure 4b shows the percent catastrophic failures which were generated after stressing with incoming catastrophic failures removed. There are fewer points plotted in Fig. 4b than in Fig. 4a, since some lots not used for flight hardware were not exposed to screen and burn-in.

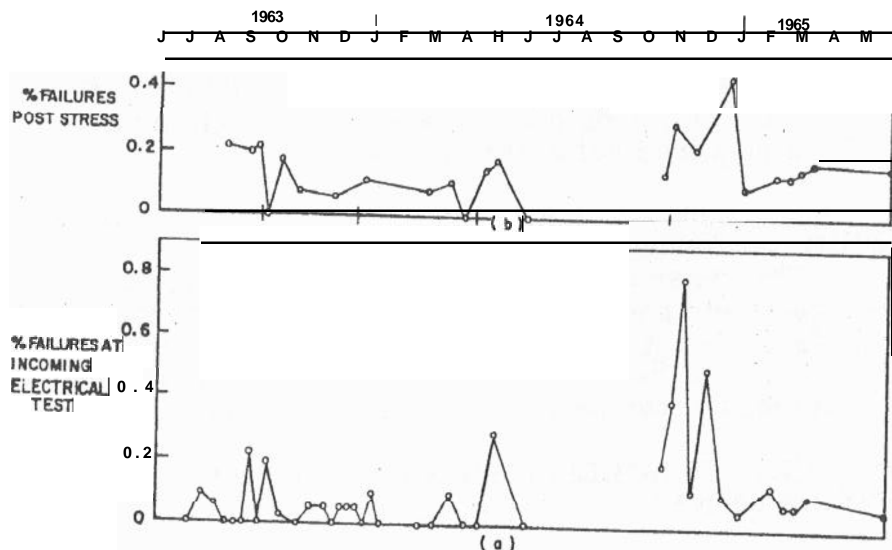

Figure 4

Vendor's performance through screen and burn-in vs time.

Examining only the numerical differences among lots of the same device shipped from the same vendor, Fig 4 shows that the percent catastrophic failures developed an average stabilized region of 0 to 0.1% at incoming electrical test and 0.1 to 0.15% at electrical tests after stressing, Most high points above these levels have been correlated to events occurring at the manufacturer. The high points prior to October 1963 represent the tail end of the manufacturer's learning curve. The high point at late April 1964 may have occurred due to reallocation of line personnel inanticipation of line shut down. There was no buying of the threeinput Nor gate between June and October 1964, so that the line producing the integrated circuit was temporarily discontinued, As a result when the production line was reinstated, several lots after October 1964 indicated a new region of instability, At that time rapid feedback to the manufacturer from the customers resulted in subsequent decrease of catastrophic failures during the screen and burn-in procedure,

One aspect of problem areas which the data of Fig. 4 does not indicate are the failure modes generated during screen and burn-in. With very few exceptions, the lots prior to June 1964 exhibited only the less troublesome or screenable failure modes and usually each lot would exhibit only one predominant failure mode. This was not the case for lots shipped after October' 1964. These lots exhibited. a variety of failure modes including the nonscreenable type, but they were waivered because of someuncertaintyof the lot reject levels. It is interesting to note that several of these lots have already exhibited failures after screen and burn-in. Confidence in the reject levels has since been established.

It might appear that the high points of Fig. 4 represent only a small percentage of catastrophic failures. But once again we must be reminded of the very low failure rates that must be achieved. Referring again to Table I it is seen that Manufacturer A developed a total of 0.3% failures after 100% stress tests were performed. Looking only at the catastrophic failures due to device faults, the percentage becomes 0.2 to 0.25%. This sample of devices exhibited one predominant failure mode of a screenable type and subsequently proved that a failure rate of 0.00 18 $/10^3$ hours at 90% confidence is attainable. In accordance with the data of Table I and the failure modes generated, the lots with the larger number of failures of Fig. 4 do not represent a negligible percentage fallout in light of the required reliability goals,

One might ask how a manufacturer can achieve excellence in reliability performance, and then for a short period of. time relax his control. The reasons are encompassed in a "state-of-the-art" process where incomplete knowledge of all the variables or insufficient control of all the variables (including the human variable) causes inadvertent changes, As a "state-of-the-art" device approaches excellence in performance, the recipe for producing the device becomes critical.

UPGRADING RELIABILITY THROUGH THE LOT ACCEPTANCE SPECIFICATIONS

The lot acceptance specifications provide a direct and indirect means of upgrading component reliability. In addition to rejecting unacceptable lots, it is readily seen that the lot acceptance specifications present a formal means of continuously monitoring a manufacturer. Other than occasionally rejecting a lot, the procedure provides extensive

vendor history with time. If the manufacturer shows a consistent degrading of performance, he is then eliminated as a qualified source until he shows proven recovery. This is an effective means of maintaining a list of reliable vendors.

On the positive side,, the screen and burn-in evaluation process sets a procedure for rapid dynamic feedback of information both to the components manufacturer and to the customer analysis, testing, and reliability groups, This information, in turn, has the potential of eliminating failure mechanisms. After failure analysis, the customer may find some failure modes are eliminable by allowing controlled process changes, by modifying specifications, or by refusing to qualify certain designs (i.e., package, device design, or metalization patterns) which have been found to contribute to failures,.. The manufacturer receives from the customer extensive data and failure information which increases the incentive to study the problems, find the failure causes and, consequently, eliminate or control them, Both manufacturer and customer are roused to study screen procedures because of the failure modes which defy present screening or are difficult to detect.

The lot acceptance specifications themselves are open to constant study and revision, The appended specifications represent a first approach toward accomplishing an assurance of needed reliability goals and have already shown their effectivity. However, as more data is accumulated, as semiconductor processing and screening procedures reach new levels, and as failure mechanisms become better known, modifications must be employed. Since the procedure must be realistic with respect to needed failure rates, this does not necessarily mean that all acceptable limits will be tightened. On the contrary, the limits may be loosened and failure modes reclassified as more assurance of process control and screenability is developed. Tightening of the limits becomes necessary if failures occur during field use, indicating that the rejection criteria are insufficient.

The entire approach requires an intimate cooperation between the customer and vendor with resultant understanding of the problems of both. The mutual‘ cooperation is necessary to achieve success of the mission.

COST

The approach presented by ND 1002248 has the potential of quantitatively defining reliability cost, By establishing limits for the number of failures per failure mode for lot acceptance, it has been shown that failure rates of 0.0018% per thousand hours are achievable. The approach also makes possible future correlation to field failure rates by the formalized procedure of the lot acceptance specification,

The cost of applying ND 1002248 may occur in one of two ways. The customer, buying from reliable component manufacturers, may absorb the cost by buying an excess of units and not using the rejected lots or sublots of parts in high reliability equipment. The component manufacturers may absorb the cost by guaranteeing the device will meet the specification and thus accept the return of rejected lots, For high volume usage devices, where adequate competition is possible, the latter

approach appears to be the least expensive and. most -desirable. The component manufacturer is incentively induced to increase his yield to the acceptance specification while adequate competition and-low unit price prevents a component manufacturer from attempting to screen out failures. Attempts by manufacturers to "test in" reliability does not remove nonscreenable and insidious long-time dependent failures which is one of the primary reasons for lot rejection by failure mode. The actual added cost of applying ND 1002248 lot rejection to the manufacturer has been shown to be equivalent to the cost of standard Group B sample testing.

In any event, the cost of assuring the success of space missions is finite and justified. However, for any program, the cost required to increase component reliability must be weighed against the cost of retrofit due to field failures. In short, the most effective positive method of building an economically reliable system is to build the system with reliable parts.

REFERENCE

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PROCESS SPECIFICATION
SPECIAL CONDITIONING OF NOR GATES
(Flat Packs)

1. SCOPE

1.1 PURPOSE

This specification establishes the minimum requirements for the acceptance of integrated circuit nor gates for use in flyable deliverabie end items, The procedures described herein shall be performed by the G&N Industrial Contractor as part of incoming inspection, screen, and burn-in,

2. APPLICABLE DOCUMENTS

2.1 EFFECTIVE ISSUES

The following documents of the issue in effect on the date of this document form a part of this specification to the extent specified herein,

SPECIFICATIONS

Military

MTL-STD- 750	Test methods for semiconductor devices

Apollo G&N

ND 1002246	Leak test procedures for nor gates.
ND 1002257	Internal visual rejection criteria for integrated circuits.

DRAWINGS

Apollo G&N

100632 1	Specification control drawing for dual nor gate (flat packs),

REPORTS

MIT/IL E- 1679	Progress Report on Attainable Reliability of Integrated Circuits for System Applic- ation.

3. REQUIREMENTS

3.1 GENERAL

The provisions of this specification shall be applicable to all phases of acceptance of integratednor gates to the extent specified herein. Specific requirements or provisions not covered by this specification shall be as specified on the applicable drawing or purchase order. In the event of conflict between the requirements of the applicable drawings, this specification and other documents cited herein, the requirements of the applicable drawings and this specification shall govern in that order.

3.2 PROCESS CONTROL

The process covered by this specification shall be controlled in accordance with the process control. provisions of 4.2.

3.2.1 Lot Control

Each lot (6.2.1) of up to 5000 units as supplied by the vendor in compliance with 1006321 shall be identified and maintained by the contractor throughout the test sequence, 3.3.1.

3.2.2 Serialization

All units of a lot shall be serialized by the G & N contractor. A unit shall be identified by the lot number and the unit serial number,

3.3 TEST PROCEDURES

3.3.1 Test Sequence

Each lot of nor gates shall. be subjected to tests in the following sequence:

a. External visual inspection (Test # 1).

b. Physical dimension, lead tension, and fatigue inspection (Test 2).

c. Electrical test (test #3).

d. Thermal cycle test (test #4).

e. Helium leak test (test #5).

f. Nitrogen bomb, oil bubble tests (test #6).

g. High temperature bake test (test #7).

h. Centrifuge Y_1 test (test #8).

i. Continuity open and short test (test #9).

j. Centrifuge Y_2 test (test # 10).

k. Electrical test (test #11).

m. Propagation delay (test #12).

n. Emitter base back bias (test # 13).

o. D.C. current gain measurement (test #14).

p. Operation life test (test #15).

q. Electrical test (test #16).

r. Vibration test (test #17).

s. Shock test (test #18).

t. Continuity test (test #19).

u. Internal visual inspection (test #20).

A flow diagram of the above sequence is attached.

3.3.1.1 Removal of Failures

Catastrophic failures only shall be removed from the test sequence at the point of detection and subjected to failure analysis, The point in the test sequence 3.3.1 where the failure was detected must be recorded and a set of electrical readings as specified in Paragraph 3.3.2.3 shall be performed. **All** electrical failures at the end of the test sequence 3.3.1 shall be subjected to failure analysis except the incoming marginal failures as defined in 6.2.3 (a), may be returned to the vendor.

3.3.2 Tests

3.3.2.1 External Visual Inspection

Each lot of nor gates shall be subjected to an external visual inspection in accordance with MIL-STD-750, method 2071, and Specification Control Drawing 1006321 with additional requirements to be negotiated with the vendor, and to be included in the purchase order.

3.3.2.2 Physical Dimension, Lead Tension, & Fatigue

A sample of 10 nor gates shall be subjected to the physical dimension examination of MIL-STD-750, method 2066, and Specification Control Drawing 1006321. Five of the 10 units shall be subjected to the lead tension and lead fatigue tests. Test #2, as specified below. The five units subjected to the lead tension and lead fatigue tests are to be forwarded to test 20 of the test sequence 3.3.1. The remaining 5 units shall be forwarded to test 3 of the test sequence 3.3.1.

(a) Lead Fatigue. Leads shall be capable of withstanding the following test: The unit shall be held in a vertical position with a 2 ounce weight suspended from the lead to be tested Two cycles of bending shall be performed A cycle consisting of moving the body of the unit, 45 degrees from the vertical in one direction, and back 45 degrees to the original position, No mechanical damage shall be evidenced after the test.

(b) Lead Tension. Each lead shall be capable of withstanding an axial pull of 1 pound for a period of 30 seconds. No mechanical damage shall be evidenced after the test,

3.3.2.3 Electrical Test (Test #3 of 3.3.1)

The entire lot shall be subjected to electrical test as described in Specification Control Drawing 1006321 with the limits as specified, The test to be performed on all base currents, I_B, all output voltages, V_O, both output currents, I_O, both collector emitter threshold currents, I_{CEX} and both collector emitter sustaining voltages, V_{CEO} sust. D.C. current gain h_{FE} shall be measured on only one transistor of each gate and RL shall be measured on one gate only,

3.3.2.4 Electrical Test (Test #11 and #16 of 3.3.1)

The electrical test shall be the same as performed for 3.3.2.3 except that the maximum limits as defined in Specification Control Drawing 1006321 shall be raised 4% the minimum limit decreased 4% and the V_{CEO} sust. test will not be performed.

3.3.2.5 Thermal Cycle Test

The units shall be subjected to thermal cycle consisting of 3 cycles of the following: The units shall be stabilized for 30 minutes minimum at +150°C ± 5°C in an oven. They shall then be transferred to an oven operating at -65 ± 5oC in less than 10 seconds, The units shall stabilize for not less than 30 minutes and then be returned to the ±150 ± 5oC oven in less than 10 seconds transfer time.

3.3.2.6 Helium Leak Test

The helium leak test shall be performed in accordance with ND 1002246 using a rate of 5 x 10^{-8} cc/atm/sec, as the upper limit.

3.3.2.7 Nitrogen Bomb, Oil Bubble Tests

The nitrogen bomb, oil bubble tests shall be performed in accordance with ND 1002246; The nitrogen bomb test shall be performed first,

3.3.2.8 High Temperature Bake Test

The high temperature bake test shall be performed in accordance with MIL-STD-750, method 1031, except the temperature shall be 150 ± 5°C and the time shall be 168 ± 8 hours.

3.3.2.9 Centrifuge Y_1 Test

The centrifuge Y_1 test shall be performed with an acceleration of 20,000g in accordance with MIL-STD-750; method 2006. Plane Y_1 is defined as a force attempting to push the internal lead wires toward the bottom of the device,

3.3.2.10 Continuity Open and Short Test

The continuity test shall be performed to detect open bonds and shorts between leads, leads and case, and leads and chip. At test # 9 check 100% at test #19 check 77 units from test #18.

3.3.2.11 Centrifuge Y_2 Test

The centrifuge Y_2 axis test shall be performed with an acceleration of 20,000g in accordance with MIL-STD-750, method 2006. Plane Y_2 is a force opposite to Y_1 as defined in paragraph 3.3.2.9.

3.3.2.12 Propagation Delay (Test 12)

Propagation delay shall be performed according to Specification Control Drawing 1006321 on a sample of 200 units* from each lot.

3.3.2.13 Emitter Base Back Bias Test

The emitter base back bias test shall be performed on 200 units* as follows. Each base input shall be connected to minus 6 volts with respect to common emitter via a 10K series resistor in each base. The units shall be operated with voltage applied at a temperature of 25°C ± 5°C for a period of 72 hours.

3.3.2.14 Beta Measurement

The D.C. current gain measurement shall be performed in accordance with Specification Control. Drawing 1006321 on the same transistors as measured at 3.3.2.4.

3.3.2.15 Operation Life Test

An odd number of units (Gates) shall be connected in series with the output of the last unit supplying the input to the first unit, thus forming a "Ring" oscillator with 8 vdc ± 5% applied continuously to the power terminals of all units in the circuit, ("Ring") oscillation must occur at the initiation of the test, This test will be performed on all units for a period of 168 hours ± 8 hours. The ambient temperature shall be maintained at 25 ± 10°C.

* When samples are selected for tests # 12, # 13, & # 17, the sample shall be representative of all diffusion sub-lots included in the shipment lot.

3.3.2.16 Vibration Test

The vibration test shall be performed on random sample of 77 units.* The vibration test shall be performed in accordance with MIL-STD-750, Method 2056, 30g's from 5 to 2000 cps. limited to 0.12 inch double amplitude, 3 cycles, 15 minutes per cycle minimum;

3.3.2.17 Shock Test

The shock test shall be performed on the same units tested in 3.3.2.16. Theshocktest shall be performed in accordance with MIL-STD-750, Method 2016, 1.500 g's, 0.5 m sec, 5 blows in all axis directions, 30 blows total,

3.3.2.18 Internal Visual Inspection

The internal visual inspection shall be performed on the 82 units from test 3.3.2.17 and 3.3.2.3 and in accordance with ND 1002257.

4. QUALITY ASSURANCE PROVISIONS

4.1 GENERAL

In order to assure proper control of the acceptance process covered by this specification, the contractor shall meet all the requirements specified herein and shall provide continuous audit of the acceptance process to assure compliance with the requirements of this specification.

4.1.1 Inspection

The contractor, through his quality assurance or control agency shall be responsible for the performance of all inspection requirements and tests specified herein.

4.2 FAILURE CRITERIA

4.2.1 Failure Analysis

All nor gates failing in the electrical tests specified in 3.3.2 (test #3, 9, 11, 14 and 16) except the non-catastrophic failures as defined in 6.2.3 (a,b,c, and e), shall be subjected to a failure analvsis sufficient to identify cause and mode of failure. For failure definitions refer to Section 6.2.

4.2.2 Failure Modes

After failure analysis all failures detected at test 3, 9, 11 and 16 of test sequence 3.3.1, except induced failures and non-catastrophic failures as defined in 6.2.3 (a, b, c, and e), shall be classified as to the following failuremodes which are described in MIT/IL Report E-1679.

* When samples are selected for tests # 12, #13, & #17, the sample shall be representative of all diffusion sub-lots included in the shipment lot,

a. Class A failure modes (class A failure modes are generally of a type readily weeded out during screen and burn-in),

1. Open bonds due to poor metalization adhesion to the silicon dioxide.

2. Open bonds due to underbonding.

3. Open bonds due to gold-aluminum eutectic formation"

4. Open bonds due to overbonding.

5. Opens due to nicks and cuts in the bonding wire,

6. Leads shorting to the edge of the chip or leads shorting to the package lid.

7. Open interconnects detected only during test 3.3.2.3 due to only scratches with no evidence of metalization corrosion at the open,

8. Shorts due to metalization scratching and smearing.

9. Shorts induced by the collector to emitter sustaining voltage test of paragraph 3.3.2.3.

10. Failures due to cracked chip.

11. Opens due to the thinning of lead wire due to poor bonding procedure.

12. Non-catastrophic failures due to surface instabilities that are not included 'in 6.2.3 (a, b, c and e).

b. Class B failure modes (Class B failure modes are of a type less readily detected during screen and burn-in as compared with Class A).

1. Shorts resulting from leads touching any other leads and shorts resulting' from leads touching metal interconnects,

2. Opens in the interconnect due to the gold-aluminum eutectic formation at the neck of an interconnect,

3. Shorts through the silicon dioxide due to poor oxide dielectric strength.

4. Shorts through the oxide because the bonds are too close to the chip edge,

5. Shorts, intermittent or otherwise, due to particles in the package.

6. Shorts, intermittent or otherwise, due to free lead material and fixed extra leads or lead material.

7. Catastrophic failures due to surface instabilities.

8. Opens in interconnect at oxide steps detected during test 3.3.2.3.

c. Class C failure modes (Class C failure modes are of a type which are time dependent and/or are not easily detected during screen and burn-in).

1. Opens in the interconnect due to corrosion.

2. Opens in the interconnect detected after test 3.3.2.3 at oxide steps.

3. Opens in the interconnect detected after test 3.3.2.3 at scratches,

4. Any failures due to electrically insulating or electrically high resistance layers forming at the silicon oxide window between the metal contact and the silicon or between the layers of metal.

5. Die separated from package header.

4.2.3 Failure Mode Grouping

4.2.3.1 Classification

Following the classification of failure modes from a lot the electrical failures will be divided into Group I - IV below and the percentage failure for the lot in each group shall be determined. Group 0 contains special cases of non-catastrophic failures.

a. Group 0. Test 3

Non-catastrophic failures as defined in 6.2.3 (a) and propagation delay failure of Test #12.

b. Group 0. Test 9, 11, 16

Non-catastrophic failures as defined in 6.2.3 (b, and c).

c. Group I. Class A failure modes,

d. Group II. Class B failure modes.

e. Group III Class C failure modes.

f. Group IV Any failure, except induced failures, not listed in Section 4.3.2 or any failure for an unknown cause.

TABLE I

Test Number (See Para. 3.3. 1)	*Maximum Percent of Failures				
	Group 0	Group I	Group II	Group III	Group IV
3	0. 5%	0.3%	0. 08%	0. 04%	0%
9, 11, and 16	1. 0%	0. 3%	0. 04%	0. 02%	0%

* For shipment lots of from 4000 to 5000 units, use the same number of allowable failures as applied to lots of 5000. For smaller lots use percentages as shown in Table I. If the number of unit failures allowable is calculated to be a mixed number, a combination of an integer and a fraction, use the integer only.

TABLE II

Test Number (See Paragraph 3.3. 1)	Maximum Percent of Failures or Maximum Allowable rejects
2	1 defective unit, Physical Dimensions
2	1 defective unit, Lead fatigue and tension
14	10 units
5	2.0%
6	2.0%
19	1 unit
20	8 units

4.3 REJECTION CRITERIA

4.3.1 Lot Rejection

The failures of a shipment lot shall be classified as specified in 4.2.2 such that the failures can beidentified with the groupings specified in 4.2.3. The maximum allowable percentages of failures from test number 3, 9, 11, and 16 of paragraph 3.3.1 according to the failure mode

groupings of 4.2.3 are given in Table I The maximum allowable percentages of failures from test numbers 2, 5, 6, 14, 19, and 20 of paragraph 3.3.1 are given in Table HI where the failure definitions are given in 6.2. Failure to meet any one of the maximum allowable percentages of Tables I and 11 or failure to comply with the test sequence of 3.3.1, the test procedure 3.3.2, the flight qualificationrequirements of 4.4, or the data requirements of 4.5 shall be cause for lot rejection,

4.3.11 Conformance to ND 1015404

Disclosure of any violation of previously agreed to contractor-supplier ND 1015404, "Critical Process" list without prior notification automatically fails the entire lot. Notice of such deviationmust -be made by the contractor to MIT/IL within 24 hours of disclosure.

4.3.2 Sub-lot removal

If the reason for shipment lot rejection can be assigned to failure modes which are traceable to a diffusion sublot(s), the entire diffusion sub-lot(s) shall be removed from the shipment lot and the provisions of paragraph 4.3.1 shall be reapplied-to--the remainder of the shipment lot. For example, failure modes which a.re traceable to diffusion sub-lot(s) are described in paragraph 4.2.2 sub-paragraphs, a 1, b 3, b 8, c 2, and c 4.

4.4 FLIGHT QUALIFICATION

4.4.1 Flight Qualified Hardware

A nor gate is flight qualified when the lot, of which the nor gate is part, is not rejected according to 4.3 and the nor gate does not fail any test of the sequence of paragraph 3.3.1,

4.4.1.1 Failure Traceability

Any nor gate failure detected in qualified flight hardware must be traceable to a lot as identified in paragraph 3.2.1 and to the unit serial number.

4.4.2 Qualification Report

Two copies of a report justifying the acceptance or rejection of a lot as flight qualified shall be forwarded to MIT/IL, prior to use in deliverable end items. The report shall include the following:

a. A summary of screen and burn-in data.

b. A detailed list of the screen and burn-in results which includes the number of failures at each test station of test sequence 3.3.1

c. A failure report of all electrical. failures, by unit serial number including induced failures, as specified in 4.3.1 which includes:

1. Photographs of each category of each photographable failure, A minimum of two photographs of each category is required where more than one exists,

2. Analysis of each failure,

3. Classification of each failure according to 4.3.2.

4. All electrical test data of. each failure,

d. Number of failures in the failure mode groups according to 4.2.3.

e. Date of purchase,

f. Total number of ordered parts,

g. Date code of parts received.

h. Lot identification-number.

i. Allocation of all parts from the lot updated to the date of issue of qualification report indicating the number of units which passed screen and burn-in, thenumber of failed units, the number of induced failures and the number of units removed from the lot for any other reason,

j. Vendor supplied Table I and Table II, sub group 1 and 3 test data.

k. A report by lot of all internal visual inspection failures (test #20 in test sequence 3.3.1) by unit serial number which includes

1. Photograph of each failure category detected.

2. Classification of each failure according to ND 1002257,

l. A list of all process changes allowed by the contractor in accordance with 1015404, paragraph 3.3.2.2.

4.5 DATA

4.5.1 Data Storage

Incoming inspection, screen, and burn-in data shall be maintained and stored by lot number and unit serial number for three years,

4.5.2 Cataloging

Nor gates failing the tests specified herein with the exception of the externalvisual inspection and leak tests shall be cataloged and stored by lot number and serial number for three years, The devices must be readily accessible for future reference.

4.5.3 Lot Storage

Units submitted to the contractor as part of the Quality Demonstration Test shall be stored by contractor's lot number for three years, The devices must be readily accessible for future reference,

5. PREPARATION FOR DELIVERY

This section is not applicable to this specification.

6. NOTES

6.1 INTENDED USE

This process conditions nor gates used in Apollo Guidance and Navigation Equipment,

6.2 DEFINITIONS

6.2.1 Lot

A shipment lot is defined as a group of nor gates submitted by a vendor in compliance with 1006321.

6.2.2 Catastrophic Failures

A catastrophic failure is defined as any device which fails the electrical tests of Table II of Specification Control Drawing 1006321 by twice the maximum or one half the minimum limits of that table.

6.2.3 Non-Catastrophic Failures

A non-catastrophic failure is any device which cannot be classed as a catastrophic failure by definition 6.2.2 but which fails according to the definitions described below:

a. A non-catastrophic failureat test 3.3.2.3 exceeds the limits of Table II of Specification Control Drawing 1006321 and does not become a catastrophic failure during test sequence 3.3.1.

b. A non-catastrophic failure at test 3.3.2.4 exceeds the limits described in 3.3.2.4 but changes parameters from 3.3.2.3 to 3.3.2.4 by less than ± 15% for base current and output voltage, ± 10% for output current or ± 20% for collector emitter threshold current. For collector emitter threshold current of less than 100 namps, an initial reading of 100 namps is assumed.

c. A non-catastrophic failure at test 3.3.2.4 does not exceed the limits described in 3.3.2.4 but changes parameters from 3.3.2.3 to 3.3.2.4 by more than ± 15% for base current and

output voltage, ± 10 for output current, or ± 20% for collector emitter threshold current. For collector emitter threshold currents of less than 100 namps, an initial reading of 100 namps is assumed.

d. A non-catastrophic failureat test 3.3.2.4 exceeds the limits described in 3.3.2.4 and changes parameters from 3.3.2.3 by more than ± 15% for base current and output voltage, ± 10% for output current, or ± 20% for collector-emitter threshold current, For collector-emitter threshold currents of less than 100 namps, aninitial reading of 100 namps is assumed.

e. A non-catastrophic failure at test 3.3.2.14 exceeds a change in D.C. current gain by ± 15% in test sequence 3.3.1 test number 11 and test number 14.

6.2.4 Induced Failures

An induced failure is a catastrophic failure which through failure analysis can be proven to be caused by exceeding the stress limits of Specification Control Drawing 1006321.

6.2.5 Leak Test Failures

A failure at test 5 of paragraph 3.3.1 is failure to meet the leak rate therein. A failure at test 6 of paragraph 3.3.1 is the failure to meet the criteria as specified in ND 1002246.

6.2.6 External Visual Inspection Failures

A failure at test 1 of paragraph 3.3.1 is failure to meet thevisual and mechanical examination criteria of Specification Control Drawing 1006321 and additional requirements negotiated with the applicable vendor.

6.2.7 Physical Dimension Failures

A physical dimension failure of test 2 of paragraph 3.3.1 is a package which does not meet the physical dimension criteria of Specification Control Drawing 100632 1.

6.2.8 Lead Tension, Lead Fatigue Failures

The lead tension, lead fatigue failures of test 2 of paragraph 3.3.1 is a partial or complete severing of a lead from the package,

6.2.9 Propagation Delay Failures

A failure at test 12 of paragraph 3.3.1 is a failure to meet the criteria of Specification Control Drawing 1006321.

6.2.10 Failures

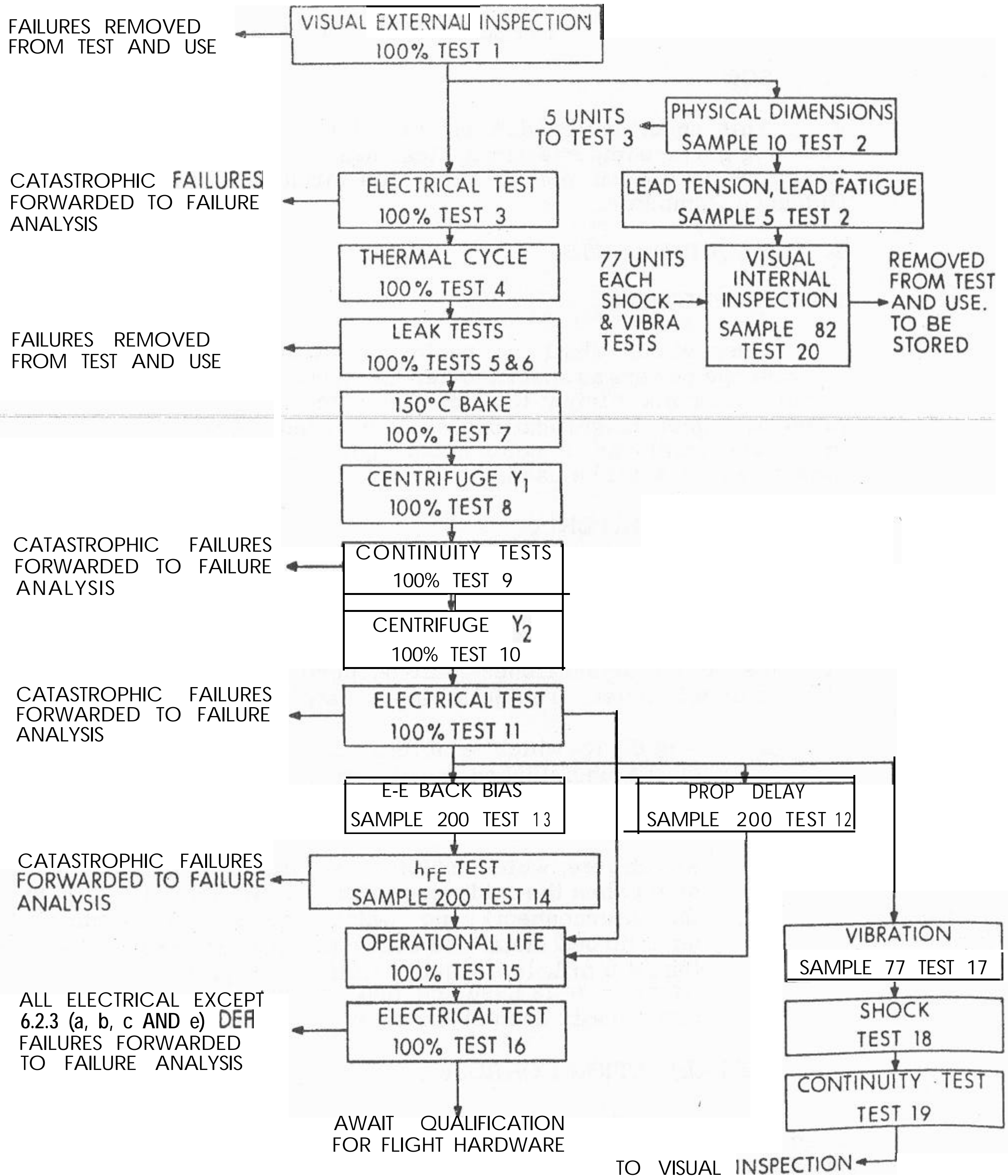
Failure of a unit in one or more tests will be charged as a single failure. A unit which could be classed by several failure modes shall be classed in the highest alphabetical mode as listed in 4.2.2. A unit which meets the definition of 6.2.3 (a, b and c) shall be counted in Group 0 only,

6.2.11 Internal Visual Inspection Failures

A failure at test # 20 of paragraph 3.3.1 is a failure to meet the criteria of ND 1002257.

6.2.12 Continuity Failure

A failure of the continuitytest is the detection of an open or a short.



FLOW DIAGRAM FOR THE TEST SEQUENCE 3.3.1

APPENDIX B

Apollo G & N Specification
ND 1002257

INTERNAL VISUAL REJECTXON CRITERIA FOR INTEGRATED CIRCUITS

1. SCOPE

1.1 This specification defines the internal visual rejection' criteria covering surface imperfections, cleaniness, workmanship, and design as it applies to silicon planar integrated circuits for use in the Apollo Guidance Computer.

2. REQUIREMENTS

2.1 INSPECTION

Inspections shall be performed with at least the minimum microscope powers as specified herein. When the minimum microscopic powers are not sufficient to determine if the herein specified faults are present, higher magnifications shall be used. When powers of 80 or more are employed, a columnated light source applied through the objective lens shall be used.

3. REJECT CRITERIA

3.1 SCRATCHES

A scratch is defined as any tear in the metalization caused by instruments such as tweezers, probes, vacuum pickups, scribing tools, etc. Inspection for scratches shall be performed at a magnification of 150 power minimum. The following constitutes rejects for scratches:

.a. Any device which exhibits a scratch which reduces the width of the undisturbed metalization to less than 0.4 mils and which exposes silicon dioxide anywhere along the scratch is a reject. (Refer to .Fig. 1).

b. Any device, which exhibits a scratch over or along an oxide step (when the oxide step intersects all but 0.4 mil or less of the interconnect) and which reduces the width of the undisturbed metalized conducting path to any contact to less than 0.6 mil, is a reject. (Refer to Fig. 2).
NOTE - It is assumed that scratches over oxide steps are electrically open at the step.

3.2 METALIZATION CORROSION

Inspection for metalization corrosion shall be performed at a magnification of 150 power minimum. Any device which exhibits any junction area covered only by unthermally oxidized silicon is a reject.

3.4 VOIDS

A void is defined as any region in the metalization where silicon dioxide is visible within the designed areas of the metalization and the silicon dioxide exposure is not caused by a scratch. Inspection for voids shall be performed at a magnification of 80 power minimum. The following constitutes rejects for voids:

a. Any device which exhibits voids at an interconnect which reduces the width of the undisturbed metalization to less than 0.6 mils is a reject (refer to Fig. 3).

b. Any device which exhibits voids at a pad or fillet which leaves the pad or fillet less than 50% of its designed area is a reject (refer to Fig. 4).

c. Any device, which exhibits voids over an oxide step (when the oxide step intersects all but 0.6 mil or less of the interconnect) and which reduces the width of the undisturbed metalized conducting path to any contact to less than 0.75 mil, is a reject (refer to Fig. 5).

3.5 MISALIGNED CONTACTS

The alignment of the metalization contact to the silicon shall be inspected at a magnification of 80 power minimum. The metalization shall make contact to the silicon over at least one half the area of the applicable window contact, Any device which does not meet this requirement is a reject.

3.6 CRACKS IN THE DIE

Inspection for die cracks shall be performed at a magnification of 80 power minimum. Any die which exhibits cracks in the active circuit, metalization, or bond areas is a reject. Any die which exhibits cracks 1 mil in length or greater which point toward the active circuit metalization or bonds is a reject (refer to Fig, 6).

3.7 BOND PLACEMENT

The placement of bonds shall be inspected at a magnification of 80 power minimum. For ultrasonic or bird beak bonds, the word "bond" refers to the tool impression. Bond placement shall be viewed directly from above. The following constitutes rejects for bond placement (refer to Fig. 7):

a. Any bond which is placed such that silicon dioxide is not visible between the outer periphery of the bond contact area and any other bonding pad or a silicon oxide edge (unthermally oxidized or "raw" silicon) shall cause the device to be rejected.

b. Any ultrasonic bond which has less' than 75% of the bond area in contact with the metalized pad shall cause the device to be rejected.

c. Any bird beak or ball bond which has the wire at the base of the bond outside the boundaries of the pad or any bond with less than 50% of the bond area in contact with the metalized pad shall cause the device to be rejected.

d. Any bond which is located in the fillet area and the longest distance between the bond periphery and edge of fillet is less than 0.4 mils shall cause the device to be rejected.

e. Any bond contact area made on the interconnect shall cause the device to be rejected.

3.8 DAMAGED LEADS

Leads shall be examined for damage at a magnification of 80 power minimum. Any lead which exhibitsnicks, cuts, crimps or scoring which cut into or deform the wire by more than 25% of the original diameter shall cause the device to be a reject.

3.9 LEAD WIRES

Lead wires shall be inspected at a magnification of 20 power minimum. The following constitutes rejectes for improper leadplacement and lead dress:

a. Leads which exhibit sufficient excess length such that there exists the capability of shorting to another lead, edge or surface of the die, or to the bottom or top of the package without deforming the diameter of the lead shall cause the device to be rejected.

b. When viewed from above, leads which cross one another or which cross any metalization which is discontinuous with the pad to which the lead is bonded shall cause the device'to be rejected.

c. Lead material greater in length than 2 wire diameters that is fixed only on one end, as for example "pigtails", shall cause the device to be rejected.

3.10 CONDUCTING PARTICLES

Inspection for conducting particles shall be performed at a magnification of 20 power minimum. Any device which contains loose or easily removable electrically conducting segments of material which are not part of the device design is a reject. Electrically conducting material. shall include any material of sufficient conductance to cause device failure of any electrical specification by shorting contacts.

3.11 WEDGE BONDS

Wedge bonds shall be inspected at a magnification of 20 power minimum. Wedge bonds which are made at the post such that the diameter of the wire at regions where the wire does not make metallurgical contact to the post is constricted to less than 1/2 of the normal wire diameter shall cause the device to be a reject.

4. PAD, FILLET, AND INTERCONNECT AREAS

The pad, fillet, and interconnect areas shall be negotiated by the purchaser with the vendor prior to procurement.

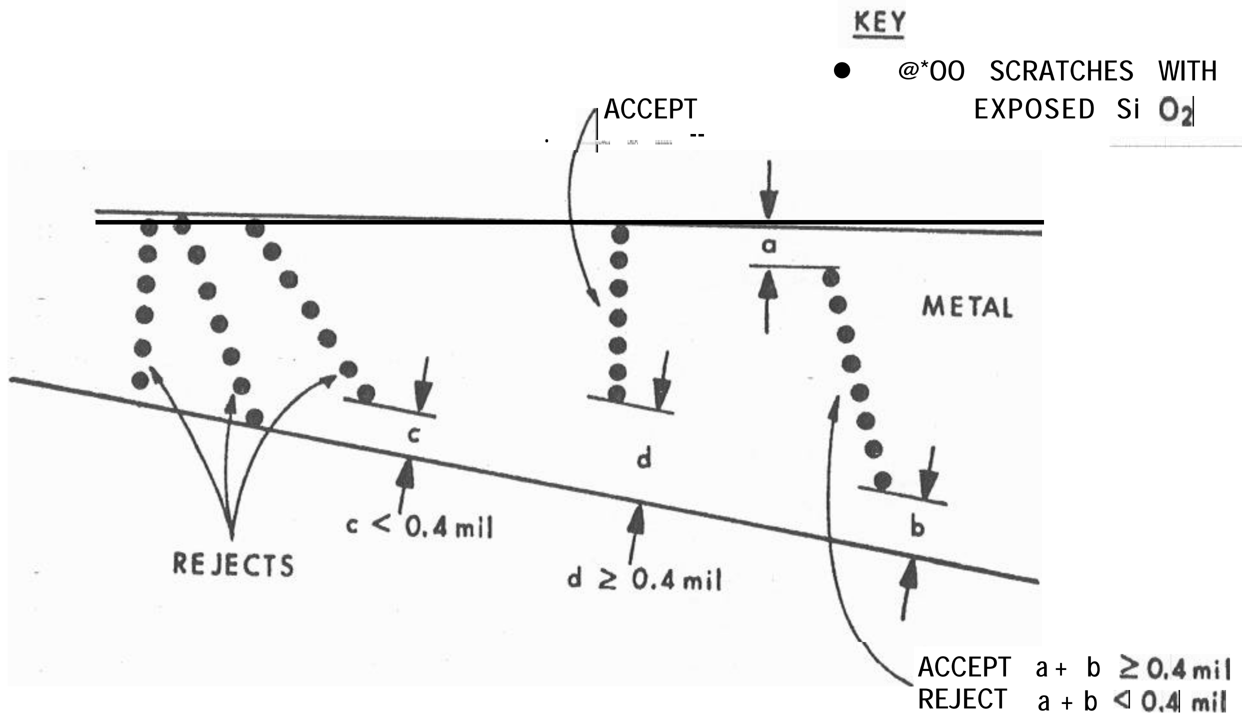
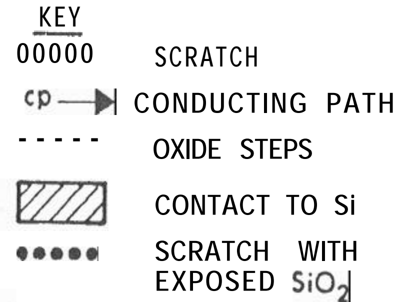


Fig. 1. Examples of acceptable and rejectable devices for scratches. Note that only those scratches which expose silicon dioxide somewhere along the scratch shall cause rejection.



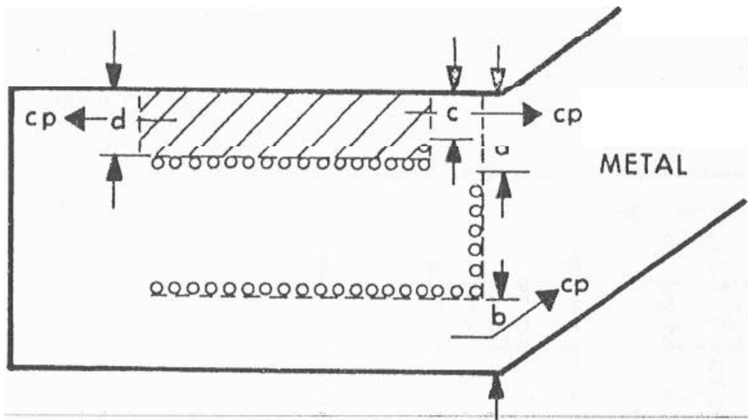


Fig. 2a. ACCEPT, a + b AND c + d ≥ 0.6 mil.
REJECT, a + b OR c + d < 0.6 mil.

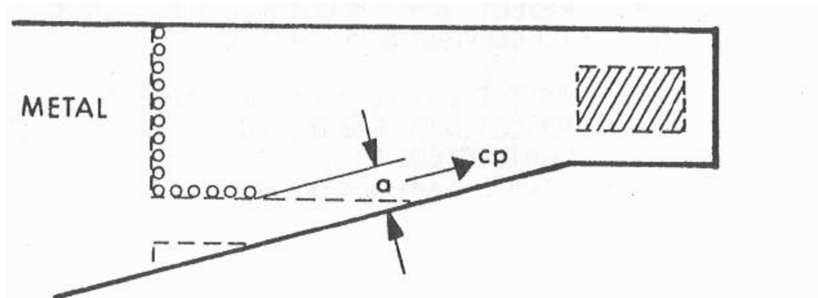


Fig. 2b. ACCEPT, a ≥ 0.6 mil.
REJECT, a < 0.6 mil.

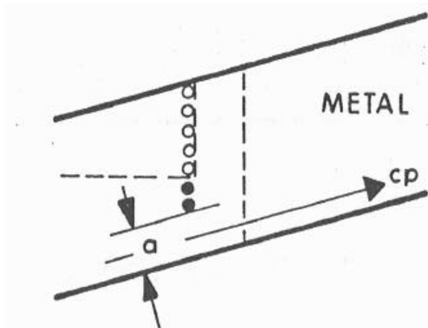


Fig. 2c. ACCEPT, a ≥ 0.4 mil.
REJECT, a < 0.4 mil.

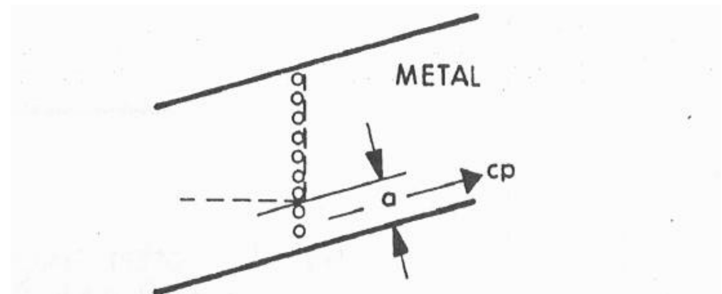


Fig. 2d. ACCEPT, a ≥ 0.4 mil.
REJECT, a < 0.4 mil.

Fig. 2. Examples of acceptable and rejectable devices for scratches at or along oxide steps.

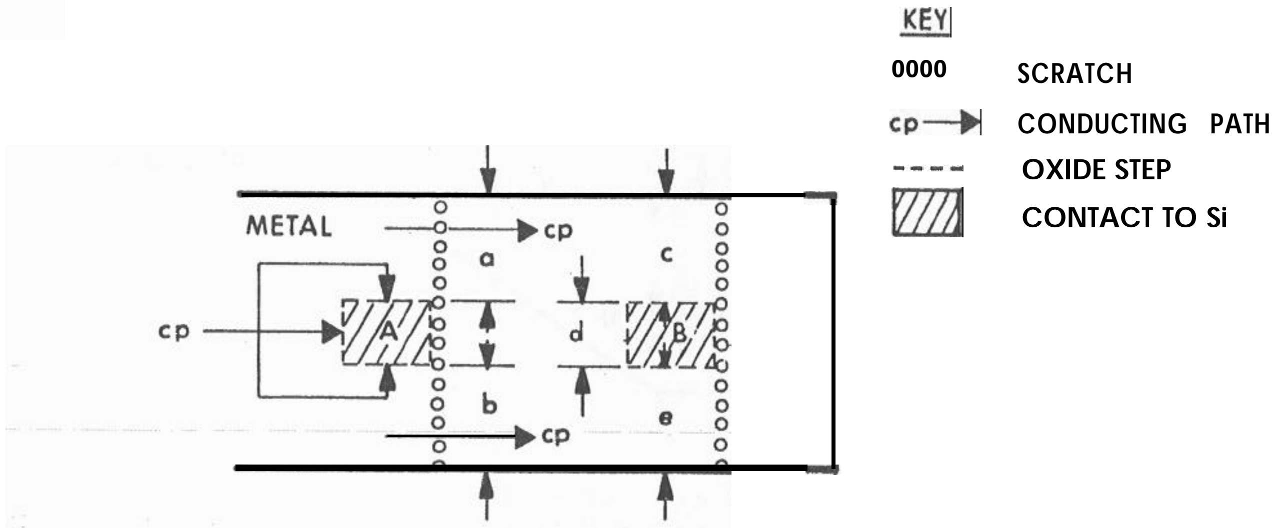


Fig. 2e. ACCEPT, a + b $\geq$ 0.4 mil.
REJECT, a + b $<$ 0.4 mil SINCE THE CONDUCTING PATH TO CONTACT B IS AFFECTED.

ACCEPT, c+d +e $\geq$ 0.6 mil SINCE THE CONDUCTING PATH TO CONTACT B $\geq$ 0.6 mil AND NO OTHER CONTACT IS AFFECTED.
REJECT, c+d+ e $<$ 0.6 mil.

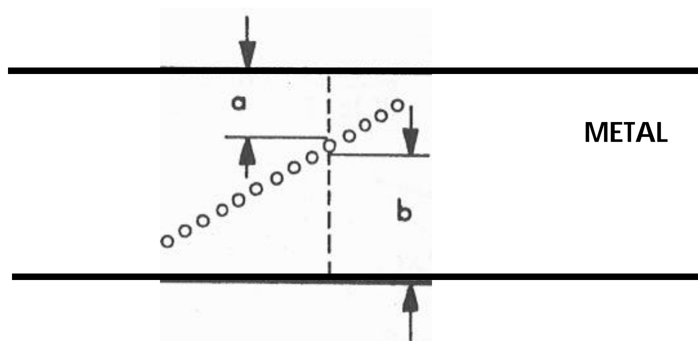
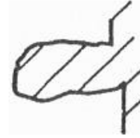


Fig. 2f. ACCEPT SINCE THE SCRATCH DOES NOT EXPOSE SiO_2 AND a + b $\geq$ 0.6 mil.
REJECT, a + b $<$ 0.6 mil.

Fig. 2 cont. Examples of acceptable and r-ejectable devices for scratches at or along oxide steps.



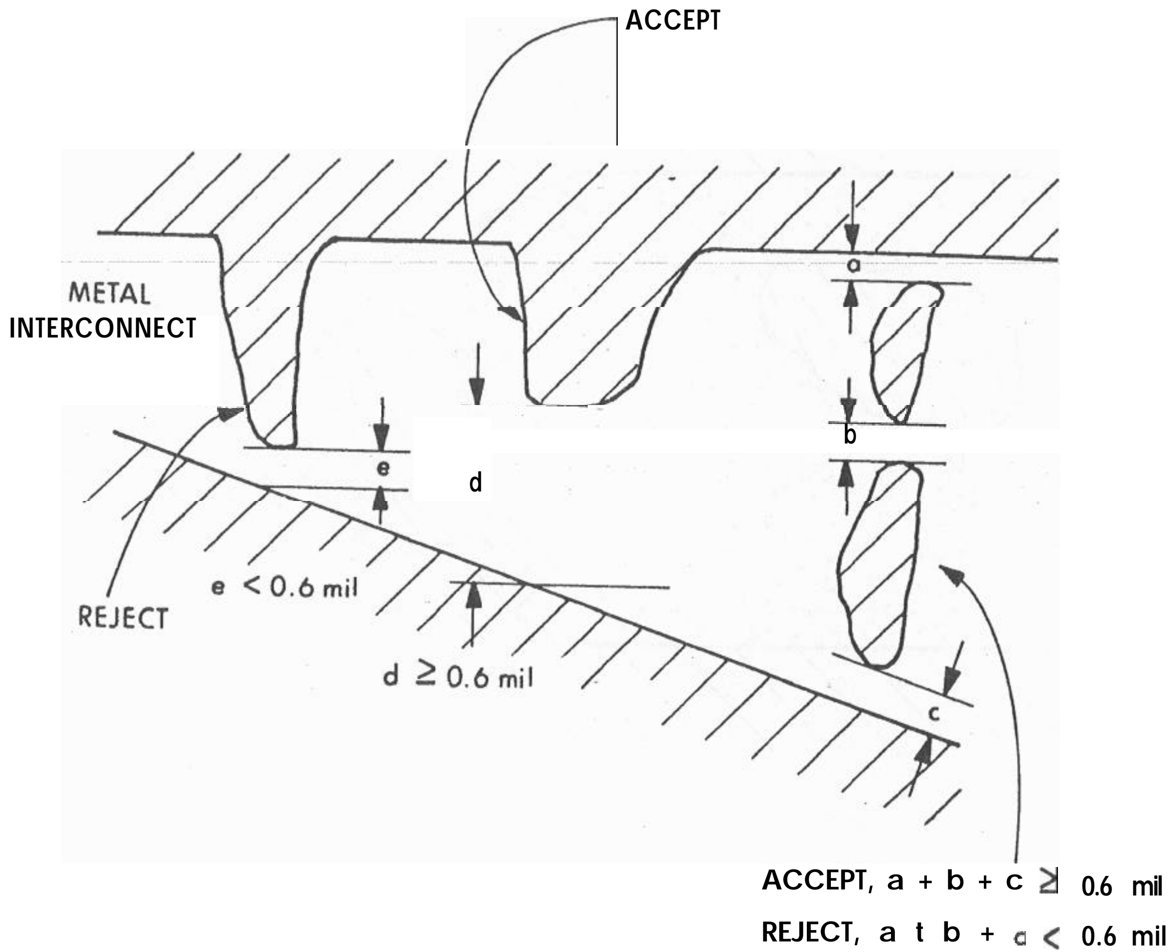
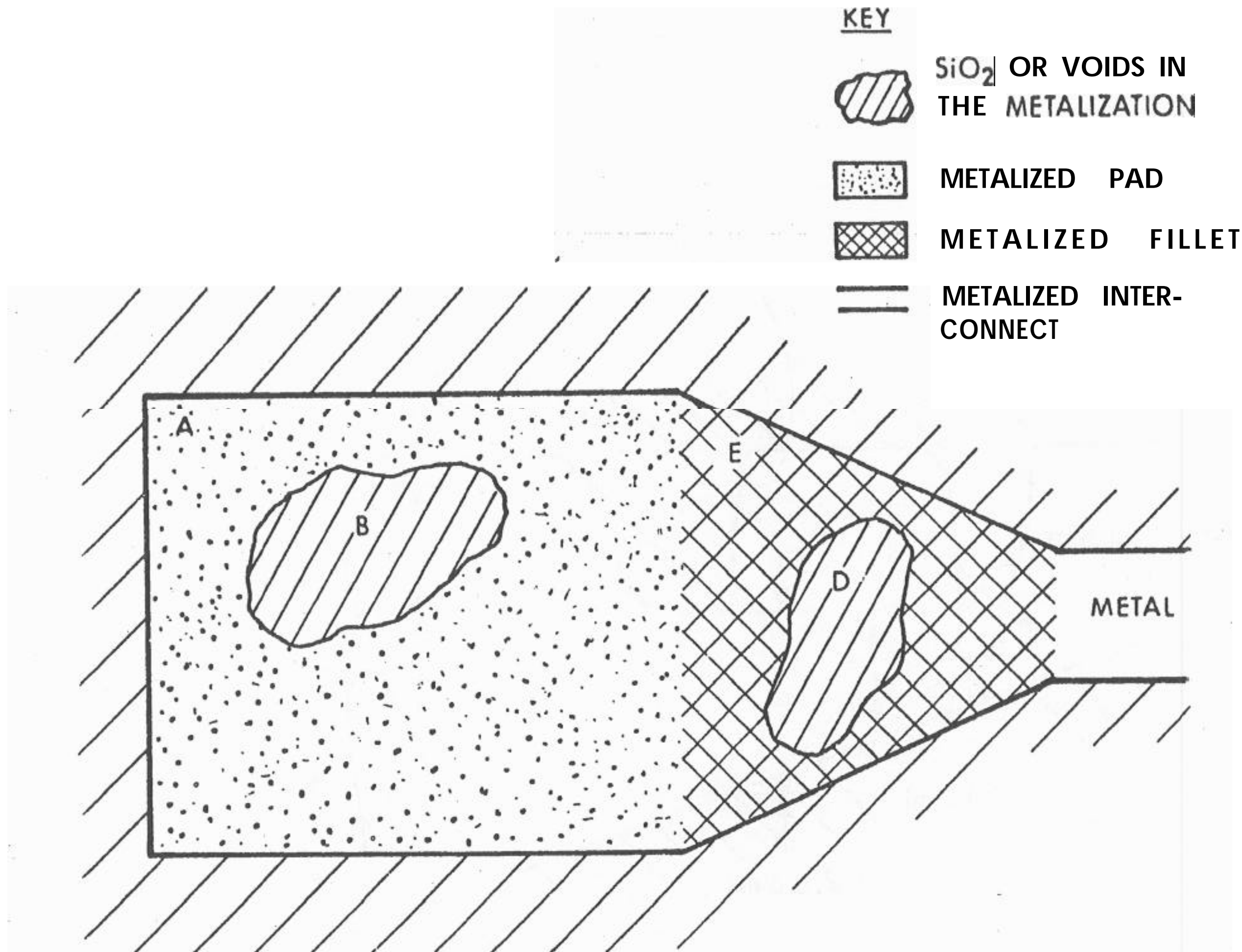


Fig. 3. Examples of acceptable and rejectable devices for voids in tho metal interconnect. Note that the conditions for accept or reject are the same 3s for scratches (Fig. 1) except that the minimum acceptable distance is larger.



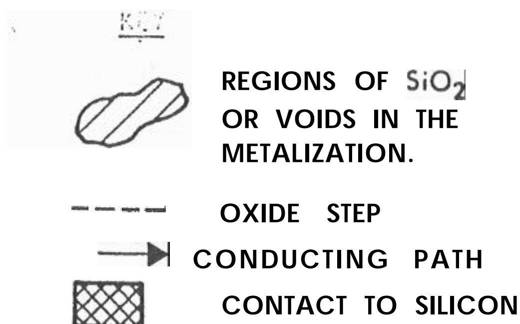
ACCEPT IF AREA B < 1/2 AREA A AND IF THE REQUIREMENTS OF PARAGRAPH 3.7b, c, d ARE MET.

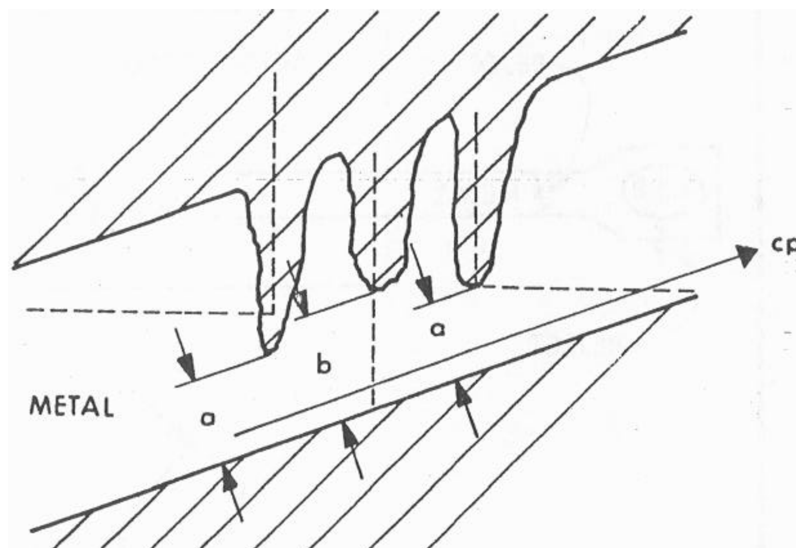
REJECT IF AREA B ≥ 1/2 AREA A.

ACCEPT IF AREA D < 1/2 AREA E.

REJECT IF AREA D ≥ 1/2 AREA E.

Fig. 4. Examples of acceptable and rejectable devices for voids in the metal pad and fillet.





ACCEPT, $a \geq 0.6$ mil.
OR $b \geq 0.75$ mil.

REJECT, $a < 0.6$ mil.
OR $b < 0.75$ mil.

Fig. 5. Examples of acceptable and rejectable devices for voids at an oxide step. Note that the conditions for accept or reject are the same as for scratches at oxide steps (Fig. 2) except that the minimum acceptable distance is larger. For more examples of voids at oxide steps refer to Fig. 2, substituting the appropriate numbers.

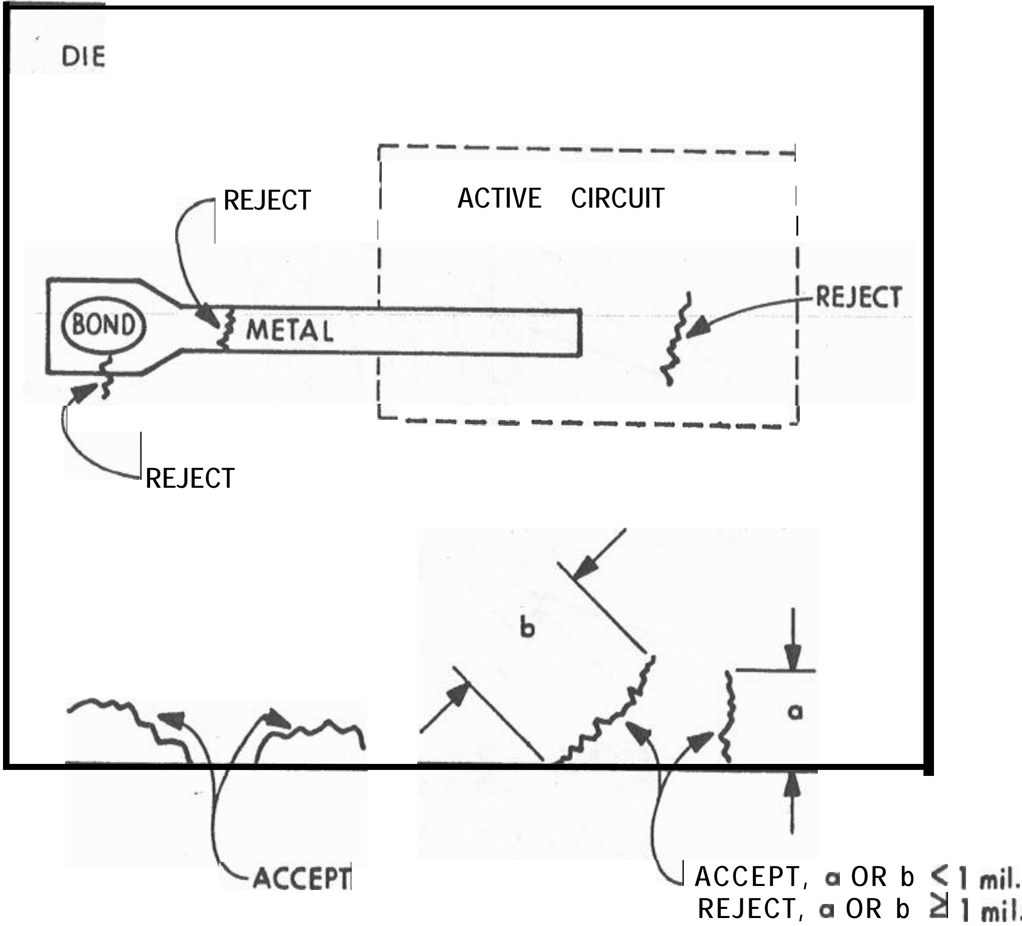


Fig. 6. Examples of acceptable or rejectable devices for cracks in the die.

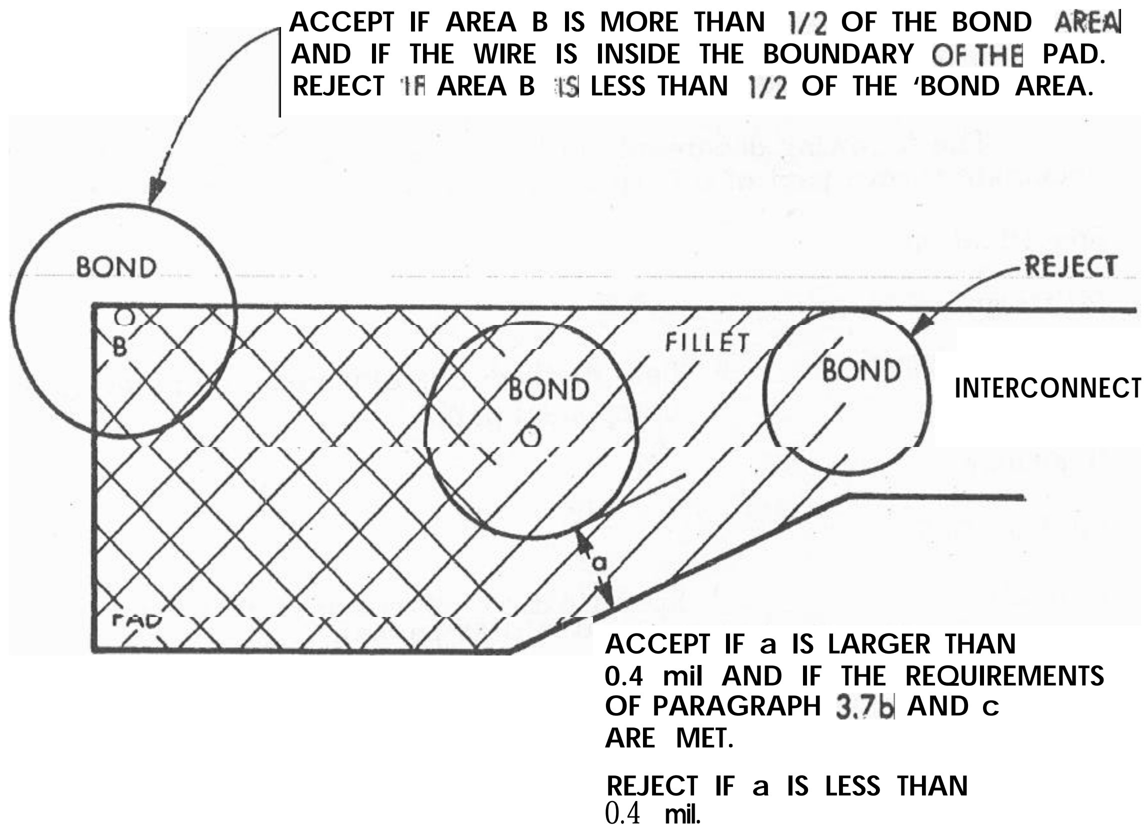


Fig. 7. Examples of acceptable and rejectable devices for bond placement. Pad, fillet, and interconnect areas are to be negotiated.

APPENDIX C

Apollo G & N Specification
ND 1002246

LEAK TEST PROCEDURES FOR NOR GATES

1. SCOPE

1.1 PURPOSE

This specification establishes the procedures for leak testing of Nor gates in a flat package and the rejection criteria for the leak tested flat packages.

2. APPLICABLE DOCUMENTS

2.1 EFFECTIVE ISSUES

The following documents of the issue in effect on the date of this document form a part of this specification to the extent specified herein.

Specifications

Military

MIL-STD-202C	Test methods for electronic and electrical component parts.

Drawings

Apollo G&N

1006321	Specification control drawing for dual nor gates (flat-packs),

3. REQUIREMENTS

3.1 GENERAL

The three leak tests specified herein are required to detect all nor gate flat pack leakers up to 5 x 10^{-8} cc/sec. The leak tests shall be performed in the following order.

3.2 HELIUM OR RADIFLO LEAK TESTS

3.2.1

The helium or radiflo leak tests shall be performed in accordance with MIL-STD-202C method 112, condition C, to the limits specified in 1006321.

3.3 NITROGEN BOMB

3.3.1 Materials

3.3.1.1 Isopropyl Alcohol, Reagent Grade

3.3.2. Apparatus

3.3.2.1 Pressure Vessel

A pressurevessel capable of storing flat packages and capable of maintaining 150 psi of nitrogen for 20 hours shall be used. The vessel must be constructed such that the packages can be removed from the vessel under pressure to the alcohol bath within a time period of no longer than three minutes,

3.3.2.2 Alcohol Bath Container

A container of approximately 4 inch diameter and 1/ 2 inch depth shall be used.

3.3.2.3 Binocular Microscope

A binocular microscope capable of magnification of 7 to 10 X shall be used.

3.3.3 Procedure

Flat packages shall be subjected to a nitrogen gas pressure of 150 psi for 10 to 20 hours. The flat packages will then be removed from the pressure vessel and placed in an alcohol bath such that the top of the package is under a 3/8 to 1/ 2 inch depth of alcohol and the alcohol bath container shall be under a binocular microscope of 7 to 10 X magnification. The time interval from beginning of depressurization to examination of the packages under the microscope shall be no longer, than three minutes The flat packages shall then be examined through the binocular microscope in groups of no more than 25 per person observing and no package body shall rest on another package body. The examination procedure shall consist of the following:

> The entire group of 25 packages shall be examined for a continuous period of fifteen minutes.

The criteria of a failure are the following:

> Observation of a continuous or intermittent stream of bubbles emanating from package leak producing areas during any examination period.

Note: Some packages will immediately emit a stream of bubbles then stop bubbling. Others will emit an intermittent stream of bubbles while others will not emit a stream of bubbles until a time period of minutes has elapsed,

3.4 HOT GLYCERINE BUBBLE TEST

The hot glycerine bubble test shall. be performed, testing units in accordance with MIL-STD- 202C method 112, condition A, with the following exceptions:

1. Glycerine shall be used instead of mineral oil.

2. The failure criteria shall be the observation of a growing bubble emerging from a sealed area, instead of observation of a continuous stream of bubbles emanating from the specimen, The observation of a growing bubble constitutes a leaker of greater than 10^{-5} cc/sec. Note that small non-growing bubbles may immediately appear upon insertion of the specimen into the glycerine due to trapped air in external package voids .

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