

APOLLO

GUIDANCE AND NAVIGATION

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A CASE HISTORY OF THE AGC INTEGRATED LOGIC CIRCUITS

Eldon C. Hall
December 1965

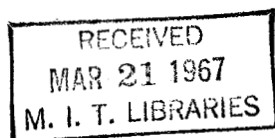
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E-1880

A CASE HISTORY OF THE AGC INTEGRATED LOGIC CIRCUIT

ABSTRACT

A case history of the integrated circuit used for the logic in the Apollo Guidance Circuit is given. Achieving the required goals of low weight, volume, and power coupled with extreme high reliability necessitated the use of one single, simple integrated circuit for all logic functions. A brief description of the evolution of the computer design is given along with a general discussion of some of the engineering and design problems which arise with the use of a standardized semiconductor monolithic integrated circuit.

The flight qualification procedure is described. After the qualified suppliers list has been formed, each lot shipped from any qualified supplier is exposed to a screen and burn-in procedure followed by failure analysis of generated failures. The lot is accepted or rejected on the basis of the number of failures generated and the types of failure modes generated. The reliability history of the NOR Gate is given showing differences among vendors, showing differences among lots shipped from a single vendor, and updated field failure rates.

by Eldon C. Hall
December 1965

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SECTION I

INTRODUCTION

Military and space objectives require the very latest in technological development coupled with reliability goals that require successful operation for several years. A compromise must often be made between the use of new technology and high reliability objectives. With judicious planning this compromise can be instituted effectively. For example, integrated circuits using planar technology have made new objectives possible by reducing the size and weight of a system while introducing an important future reliability gain.

The inherent reliability gains must be implemented in the design stages of the computer. Hence the decision to use one simple single logic element for the logic in the Apollo Guidance Computer. This resulted in high volume procurement of the integrated circuit from multiple sources, so that the needed high reliability could be developed and proven within a short period of time.

The standardization approach, which is particularly adaptable to digital computers, has been demonstrated with the Polaris flight computer and extended with integrated circuits to the Apollo Guidance Computer. Both computers were designed to use a three input NOR Gate as the only logic element. All logic functions are generated by interconnecting the three input NOR Gate with no additional logic blocks, resistors, or capacitors. At first glance, it appears that using only one type of logic block greatly increases the number of blocks required for the computer. But, by judiciously selecting and organizing the logic functions it is quickly apparent that few additional blocks are necessary. The few additional units required are greatly counter balanced by the increased reliability gain during both the manufacturing of components and fabrication of the components into modules.

The logic element utilized in the Apollo Guidance Computer is the three input NOR Gate as shown in Fig. 1. At the time that the decision was made to use integrated circuits, the NOR Gate, as shown, was the only device available in large quantities. The simplicity of the circuit allowed several manufacturers to produce interchangeable devices so that reasonable competition was assured. Because of recent process development in integrated circuits, the NOR Gate has been able to remain competitive on the basis of speed, power and noise immunity. This circuit is used at 3V and 15mw, but is rated at 8V and 100mw. Unpowered temperature rating is 150°C. The basic simplicity of the three input gate aids an effective screening process. All transistors and resistors can be tested to insure product uniformity. The simplicity of the circuit also aids in the quick detection and diagnosing of insidious failures without extensive probing as required with more complicated circuits.

One additional integrated circuit used in the Apollo Guidance Computer is the memory sense amplifier. As seen in Fig. 2, the circuit is considerably more complex than the NOR Gate. The experience with this more complicated circuit has been comparable with the logic gate. However, since it is a low usage item there is available less information of historic interest, that is, reliability information such as failure rates and modes of failures. The balance of this report relates to history of the logic gate.

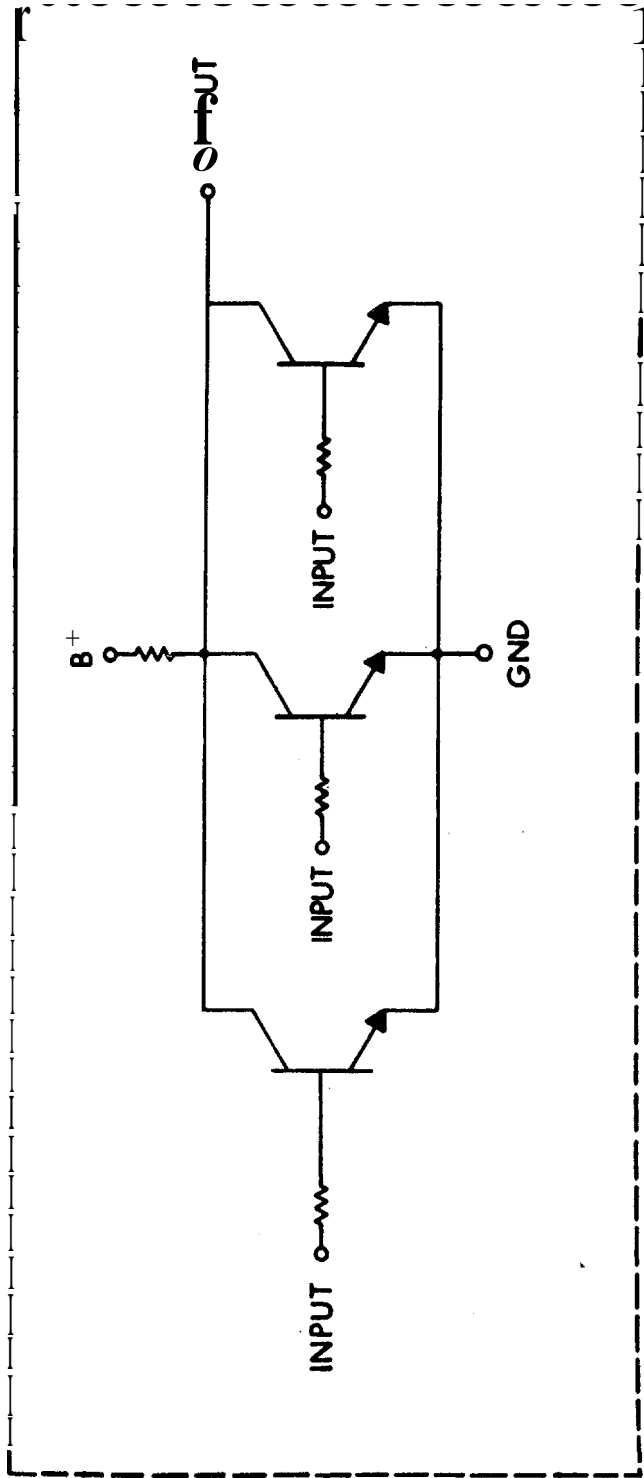


Figure 1

SENSE AMPLIFIER CIRCUIT

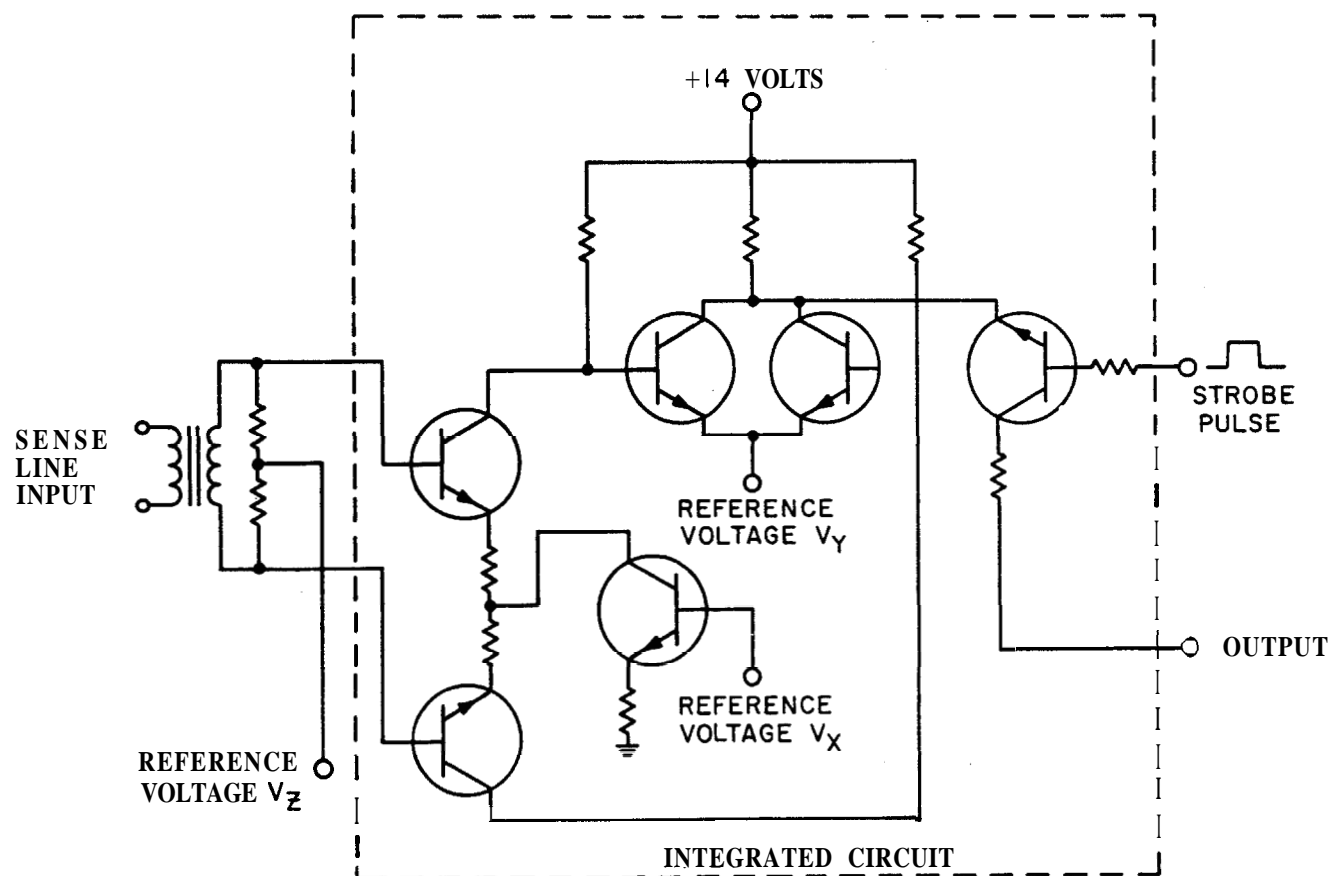


Figure 2

SECTION II

ENGINEERING ASPECTS OF THE APOLLO COMPUTER

Figure 3 pictures the Block II Apollo Guidance Computer. This version differs from the Block I Computer in that the memory, instruction and input output was increased. The Block II Computer also uses a dual gate in a flat package rather than the single gate in a TO-47 used in Block I. Figures 4 and 5 illustrate the packaging techniques used in the Block II computer. The Block II logic sticks are made using the flat package welded to multilayer interconnection boards. The modules are interconnected using a tray which is wired by machine wire wrap technique as shown in Fig. 6. Two identical Display and keyboards as shown in Fig. 7 provide the man machine interface with the computer. Table I is a general summary of the Block II computer characteristics.

Since the logic design of the computer was restricted to a single type of gate, a method to provide fan-in and fan-out expansion was provided as shown in Fig. 8. Also, methods that were used to provide interconnections between logic and memory circuits and connections to outside world are shown in Fig. 9. All high frequency information transfer between the computer and periferal equipment is accomplished with transformer coupled circuits as shown in the top view. The second row is the type of circuit used in the memory interfaces and for low frequency DC level type signals. The receiver is shown on the right. The bottom row provides low frequency DC level inputs.

Interesting and subtle problems arise with the use of integrated circuits. To illustrate, Fig. 10 (a) depicts a very desirable circuit that can be used to drive long cables for ground test equipment while requiring no power drain from the airborne equipment. Figure 10 (b) shows the same circuit but includes some of the parasitic diodes not usually represented in the integrated circuit. When point (x) rises above 2 volts, diode capacitor coupling occurs through the resistor substrate which activates the unused transistors. This coupling

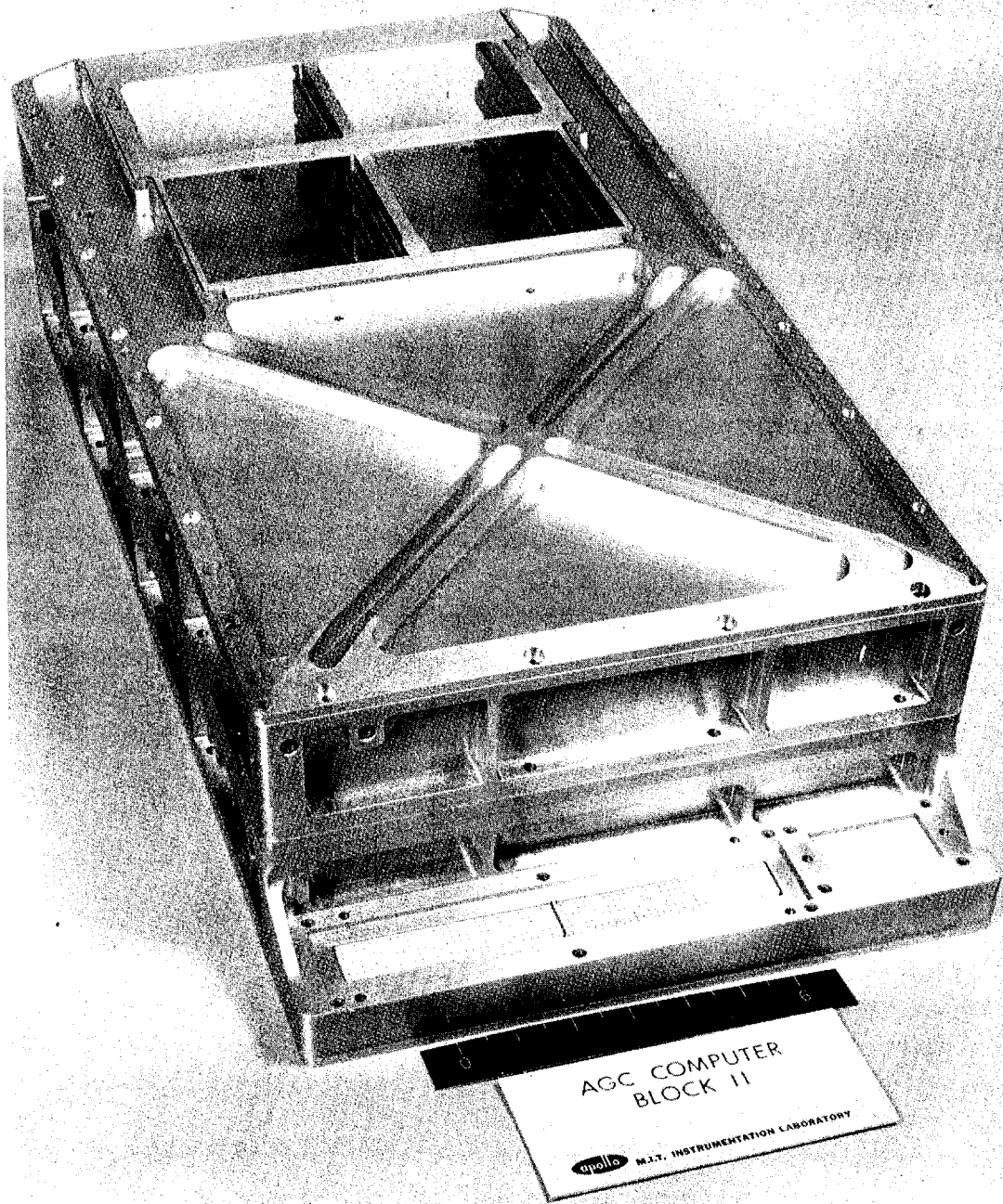
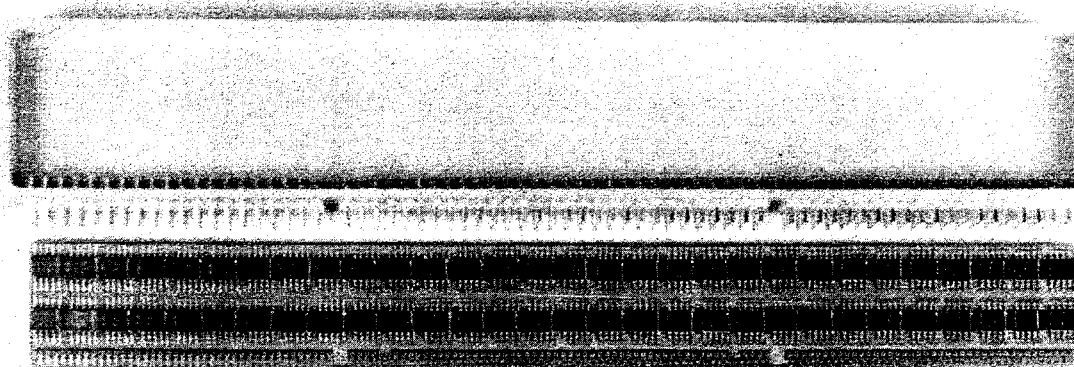
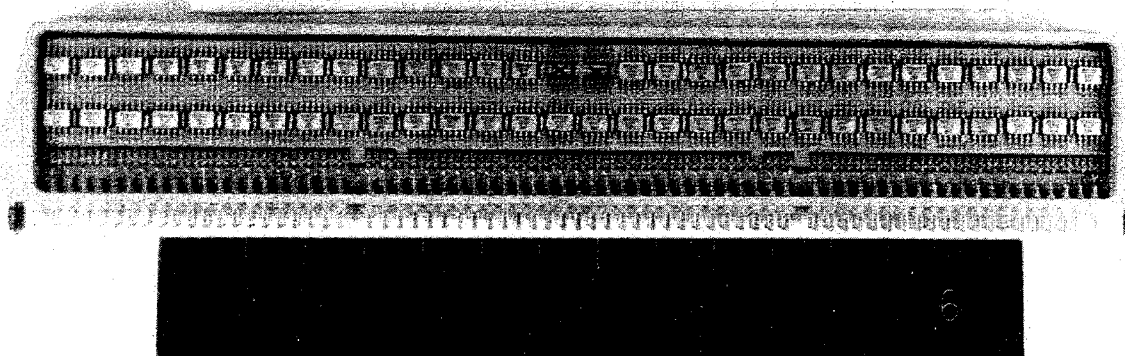


Figure 3



**MODULE MOUNTING FRAME AND
MULTILAYER BOARD
WITH MICROLOGIC ASSEMBLED
(PRIOR TO FINAL WELDING)**



**— FINAL ASSEMBLY —
(PRIOR TO ENCAPSULATION)
TYPICAL DIGITAL MODULE BLOCK II CDU**

Figure 4

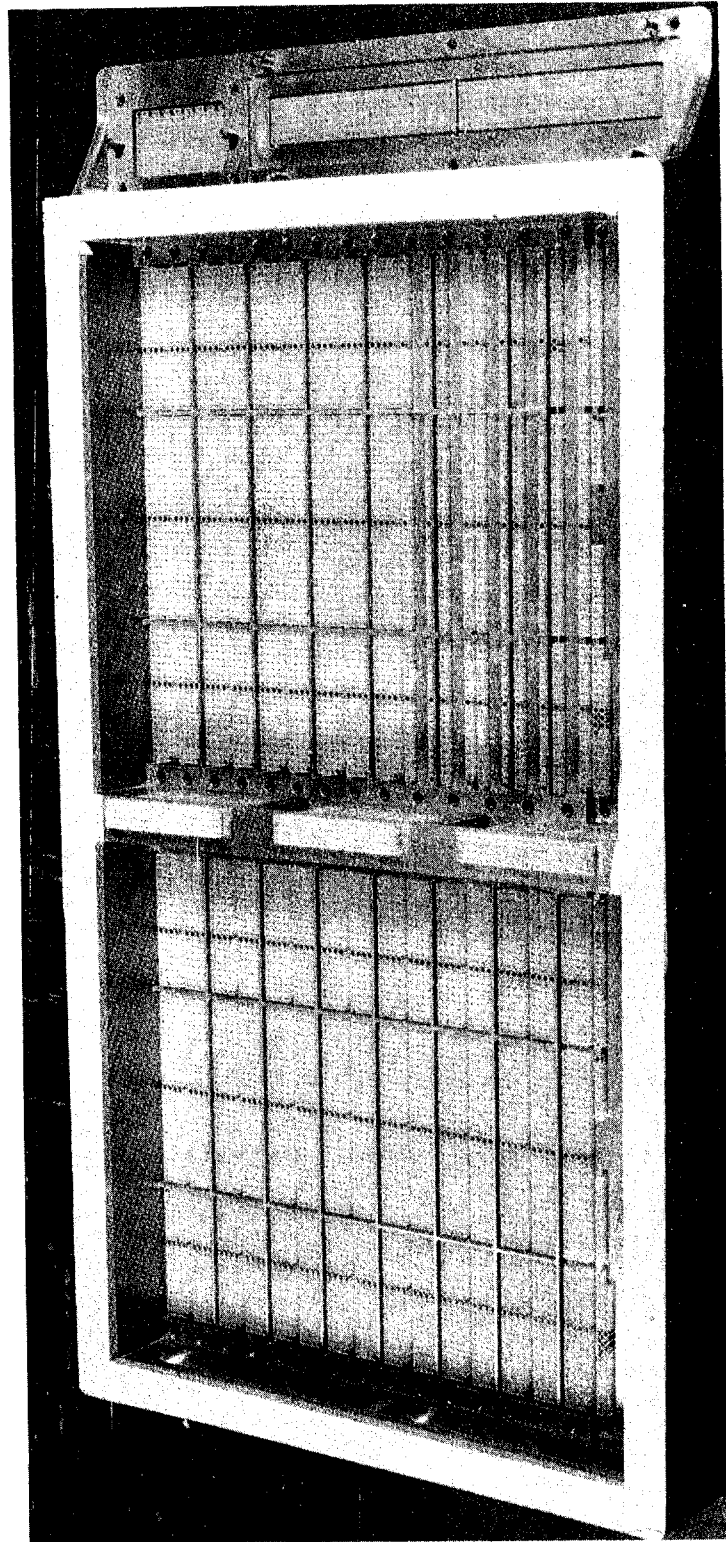


Figure 5

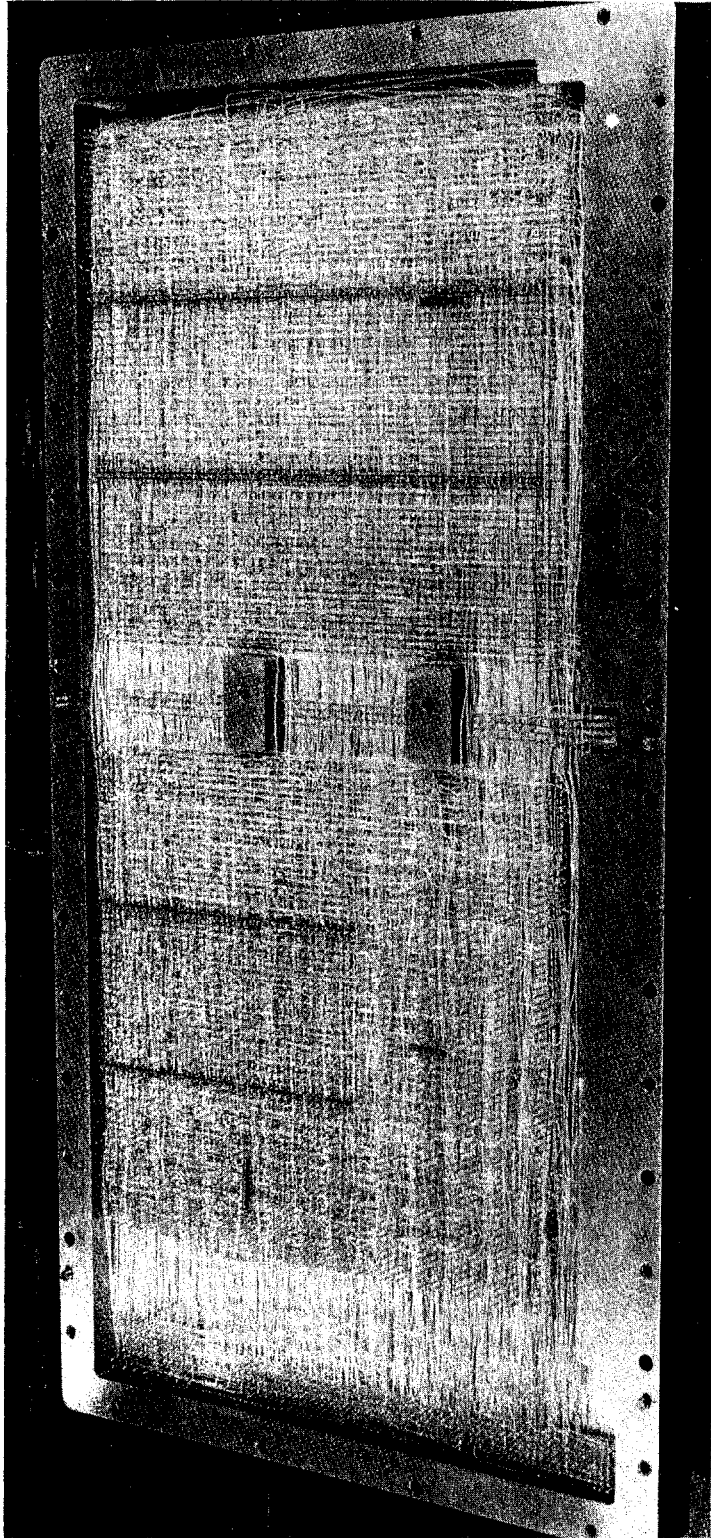


Figure 6

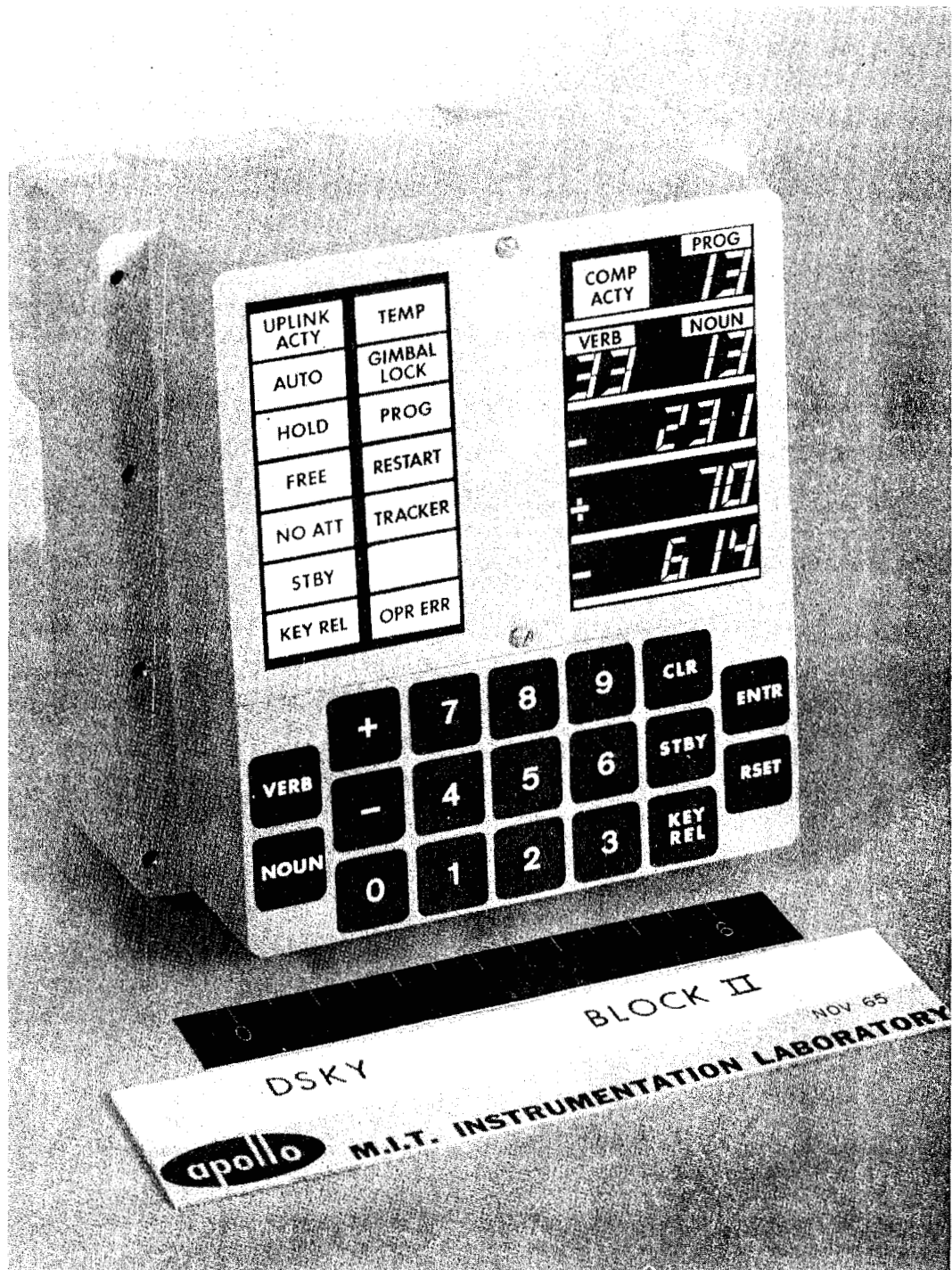


Figure 7

AGC CHARACTERISTICS

Word Length	15 Bits + 1 Parity
Number System	One's Complement
Memory Cycle Time	11.7 μ sec
Fixed Memory Registers	36,864 Words
Erasable Memory Register	2,048 Words
Number of Normal Instructions (Interrupt, Increment, etc.)	10
Interrupt Options	10
Addition Time	23.4 μ sec
Multiplication Time	46.8 μ sec
Double Precision Addition Time	35.1 μ sec
Double Precision Multiplication Subroutine Time	575 μ sec
increment Time	11.7 μ sec
Number of Counters	29
Power Consumption	100 Watts (AGC + DSKY's)
Weight	58 Pounds (Computer Only)
Size	1.0 Cubic Foot (Computer Only)

Table I.

LOGIC DESIGN

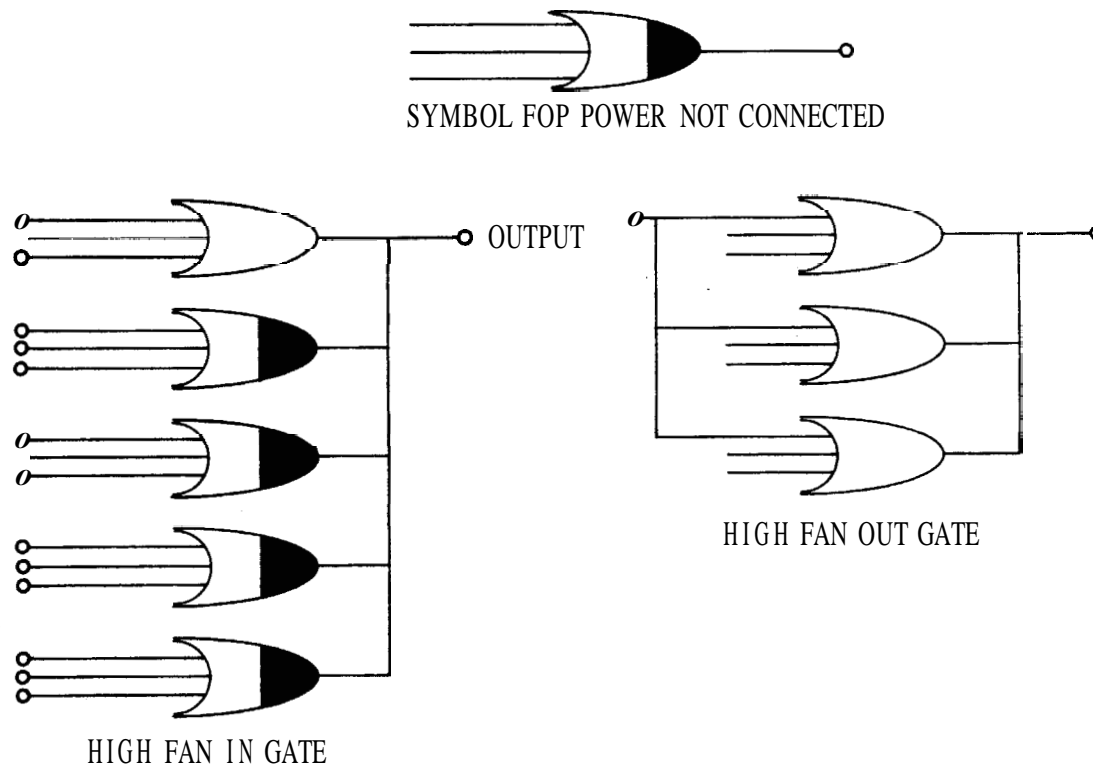
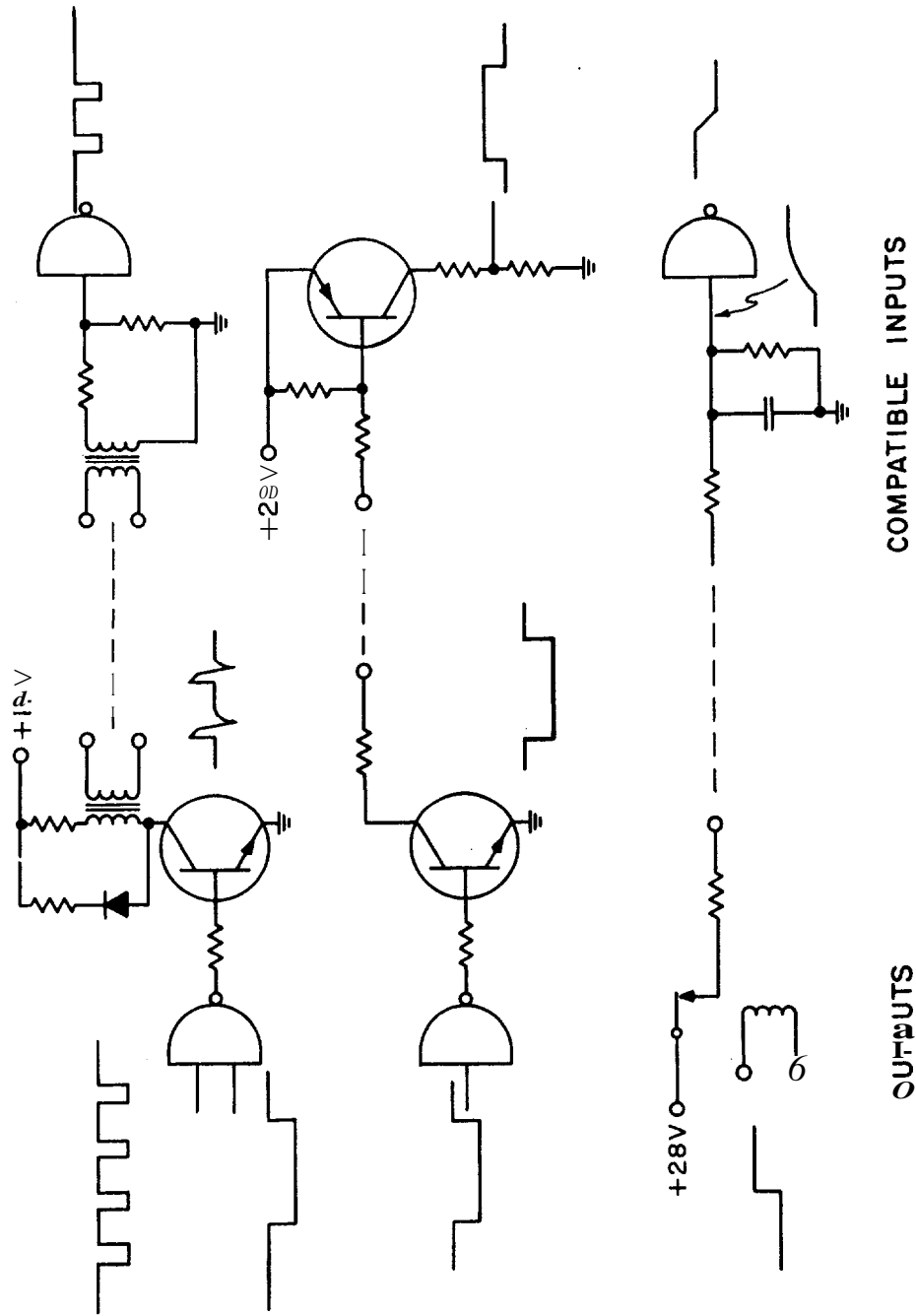


Figure 8

EXAMPLES OF AGC INTERFACE CIRCUITS



COMPATIBLE INPUTS

OUTPUTS

Figure 9

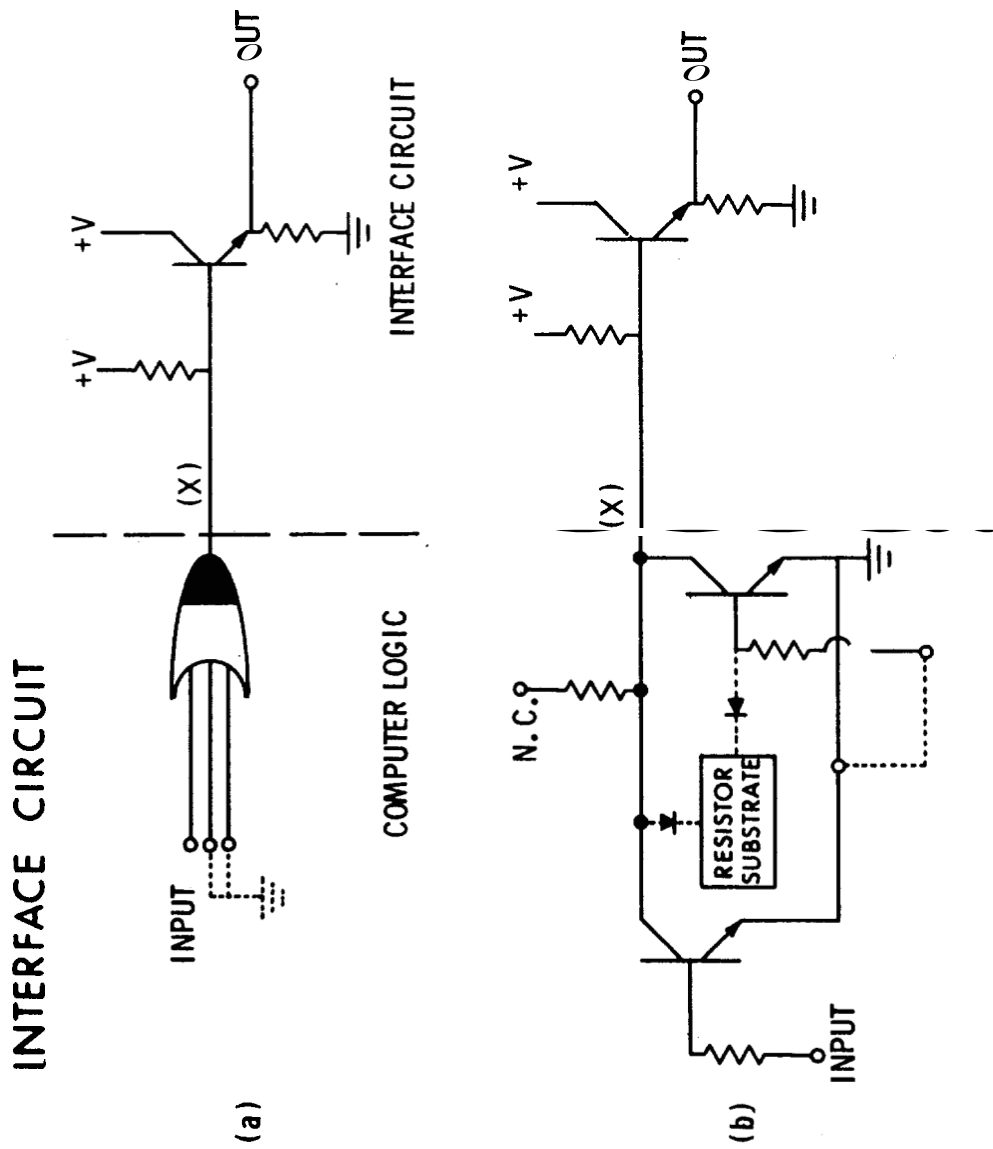


Figure 10

is a feedback path which slows up the pulse rise times. The rise time will be a function of the gain of the unused transistor and also a function of repetition rate of the drive which tends to turn the transistors off at high repetition rates. Connecting all unused inputs to the emitter (0V) will prevent or minimize the feedback thus speeding up the pulse response. Another interesting and much discussed problem is that of noise in logic circuits using integrated circuits. It is well known that all digital computers have noise problems and there are well known design techniques which when properly applied will minimize these problems. In the electrical design as well as the mechanical design there are trade offs that must be made in order to meet all of the ground rules placed on the computer designer. Noise is one of the major constraints that must be considered during the design. One must consider both self induced and externally induced noise. Although the cause is different for both types, the effect is usually the same and can be illustrated by Fig. 11. From this figure it is seen how switching currents in the circuit ground plane can cause voltage transients that will erroneously switch the transistors shown. These ground currents can also be induced from the outside either by conducted or radiated interference. To maximize the immunity of the computer the designer should,

1. Select circuits that have maximum immunity:
there is about a factor of 2 realizable between the worst and best integrated circuits.
2. Provide good ground planes and signal paths.
3. Provide proper shielding, grounding and filtering of the computer, and all interface wires.

Obviously one must compromise here also, otherwise the protection as well as the magnitude of the noise would continue to escalate. In the choice of the NOR Gate, the Apollo Computer may have sacrificed some noise immunity for simplicity and availability. Testing of the finished computer has shown that its susceptibility is much lower than the limits specified in MIL-1-26600 which is the specification for electromagnetic compatibility. In fact, in order to locate areas of weakness,

NOISE PROBLEM

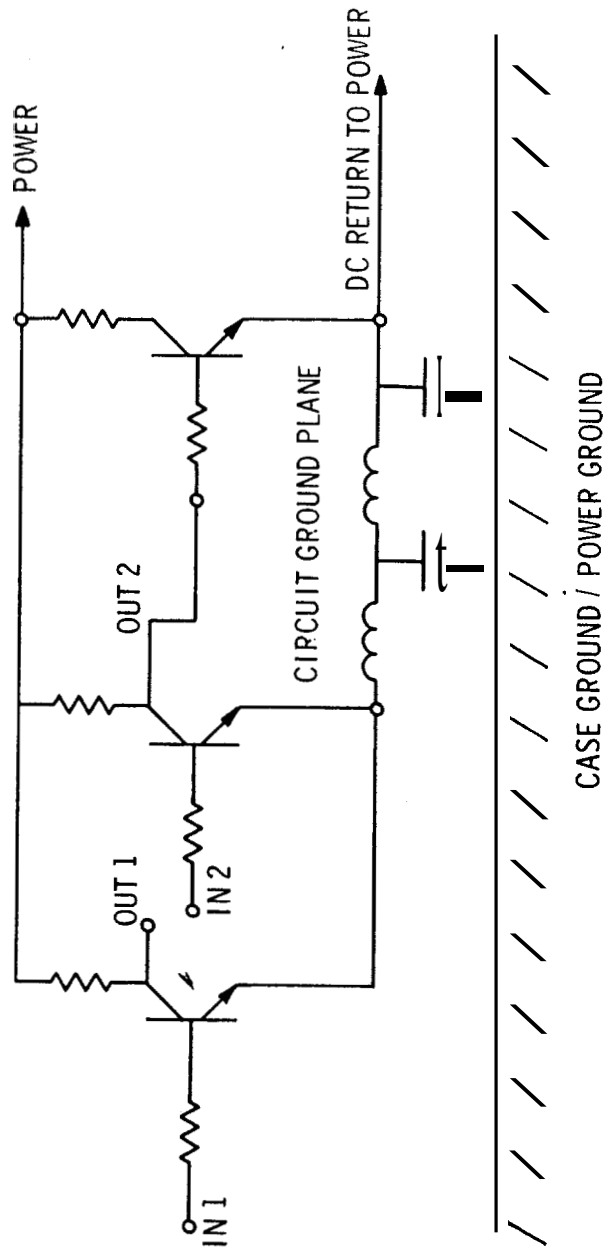


Figure 11

spark discharges have been used during testing. The normal radiation susceptibility tests do not generate levels high enough to induce computer failure. In fact, MIL-1-26600 is weak in other areas when applied to digital computers. For example, a power transient between a power input line and case is notorious for inducing troubles and locating areas of weakness, although this test is not a requirement of the MIL spec. The Apollo computer has been subjected to and passed these more stringent tests.

SECTION III

RELIABILITY

Because of the high reliability application of the Apollo Guidance Computer, the reliability assurance of the integrated circuits will be discussed. The procedures have been previously reported in detail, but will be summarized here.

It became immediately obvious that small-sample stress testing could not guarantee that each purchased lot would meet the Apollo integrated circuit failure rate requirements. The MIL-S-19500D statistical sampling procedure was both not applicable nor practical. Furthermore, as long as all failure modes were not completely screenable, one-hundred percent screening alone was not sufficient to attain the required high reliability goals. A study of the various failure modes of integrated circuits created the dilemma whereby some of the failure modes were easily screened by standard screening techniques and others only occasionally detected. No assurance could be made with any reasonable confidence that the devices with these troublesome defects had been removed from the lot. To overcome this problem, lot acceptance criteria were established which would identify with high confidence those lots in which insidious failure modes were not prevalent and screening had been adequate. Providing an effective failure mode detection system, the procedure for lot acceptance is based on one-hundred percent nondestructive tests and sample destructive testing. All the failures generated from the testing are completely analyzed. The failures are then classified by groups and compared to the acceptance criteria. It must be emphasized that the lot is accepted or rejected not only because of the number of failures but also on whether the failure modes generated were nonscreenable or insidious and long time dependent.

The Apollo Guidance and Navigation Specification, ND 1002248, is the central document on which each procured lot qualification is based. This document specifies the procedures required for lot acceptance resulting in flight qualified parts. In particular, ND 1002248, specifies the details of:

1. The operational and environmental stress test procedures and sequence commonly referred to as the screen and burn-in procedure. The screen and burn-in procedure was designed to detect failure modes which could occur during the normal stress and environmental application of the device.
2. The electrical parameter tests to be performed during the screen and burn-in procedure. The tests as defined were determined during the engineering evaluation and were chosen to detect failures and assure proper computer operation.
3. Definitions of failures. Failures have been defined as catastrophic, several categories of non-catastrophic, induced, and inspection failures.
4. Allocation of failures. The conditions are defined for removal from the screen and burn-in procedure of failures which are to be forwarded to failure analysis.
5. Classes of failure modes. Failure modes are classified according to screenability and detectability.
6. Maximum acceptable number of failures per class of failure mode for all 100% electrical parameter test stations.
7. Maximum acceptable number of failures for non-electrical tests and all sample electrical parameter tests.

8. The report required for each flight qualified lot. The report must contain the complete history of the lot with the specific data and analysis required for flight qualification.
9. Data and failed parts storage. In order to assure traceability and future analysis should field failures occur, the conditions of data and failed parts storage are given.
10. Contractual requirements to implement lot qualification.

To assist the understanding of the lot acceptance procedures, a general discussion of the semiconductor part vendor selection and flight qualification procedures will be given as performed for the Apollo Guidance and Navigation Computer.

The process begins with an assessment of the vendor's ability to supply devices, the institution of component standardization in designs, and the preliminary study of device failure modes. A block diagram of this preliminary evaluation which precludes any production procurement is given in Fig. 12. The qualification procurements which supply parts for the qualification testing and engineering evaluations established the manufacturer's device processing. One of the indirect results of the initial procurements is the early detection of new failure modes. The conclusions of the failure analyses are then fed back to the manufacturer who in turn attempts corrective action. This cyclic procedure is continued until the most obvious problems have been eliminated. Additionally, the early detected failure modes coupled with past experience are utilized to design the qualification testing.

The formalized qualification testing begins when the vendors have supplied devices representative of their finalized manufacturing process. It is extremely important that all qualification and engineering testing be performed on devices fabricated from the identical process used to supply computer production devices. The qualification tests subject the

PART AND VENDOR SELECTION

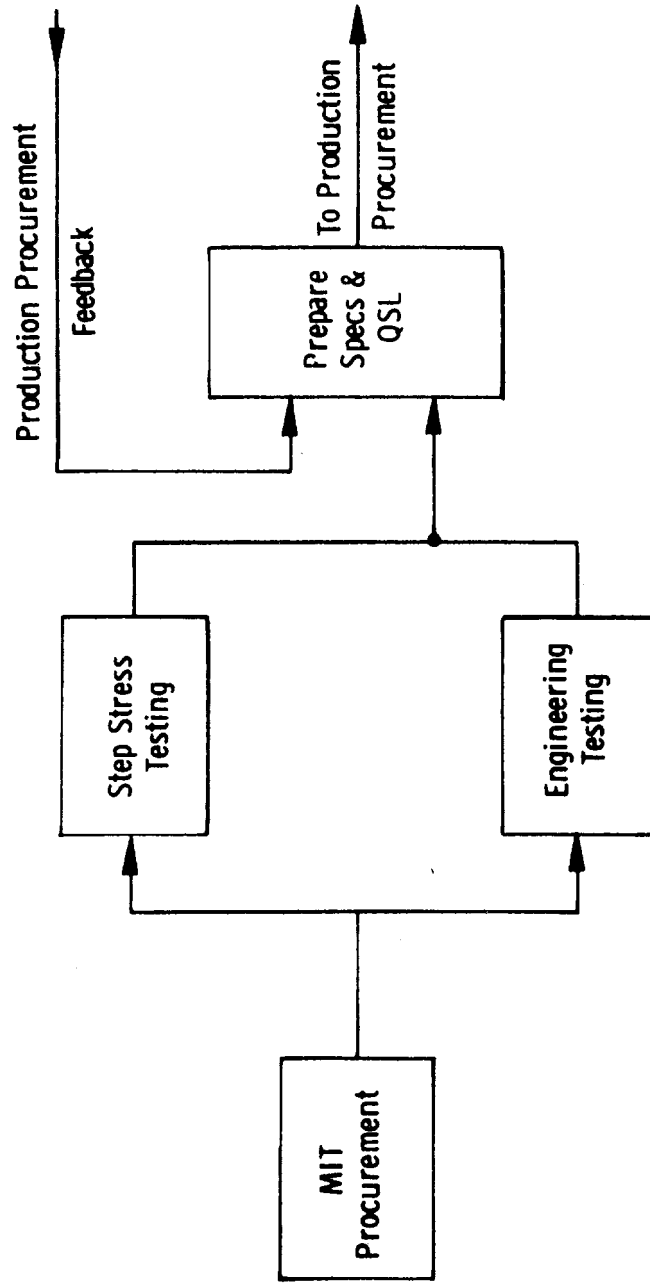


Figure 12

devices from various vendors to the extremes of and, to a limited extent, beyond usage conditions in an attempt to detect failure modes which could occur in normal applications.

The engineering evaluations are performed simultaneously with the qualification procedures to determine device speed, fanout capability, noise immunity, and operating temperature range. From this evaluation, the optimum computer design is developed. It is at this time that tests are conducted to determine the electrical parameters which will insure proper device operation in every usage mode and to establish the logical design rules for the computer.

The qualification and engineering evaluations determine those vendors who are capable of supplying the semiconductor part and who do not exhibit any gross reliability problems. The qualification tests alone are insufficient to determine the ability of a vendor to control his process, but large volume production procurement data fed back from screen and burn-in supplies extensive vendor history.

Utilizing the data generated during the engineering evaluations and qualification tests, the specification control document (SCD) is prepared. The SCD is the document to which production parts are bought. Based on the qualification by vendors, the qualified suppliers list (QSL) is formed which specifies the vendors from whom the production parts shall be procured.

Once the SCD and QSL have been released, production procurement may begin. Figure 13 pictures the general flow of parts and data as required for flight qualification. The devices procured by lots proceed through the screen and burn-in (S&BI) test sequence.

Upon completion of screen and burn-in, the lot is stored until failure analysis is completed. All failed units are catalogued, analyzed, and classified to complete the lot assessment, followed by a written report. If the lot passed, all the devices that passed all tests can be identified as a flight qualified part with a new part number and

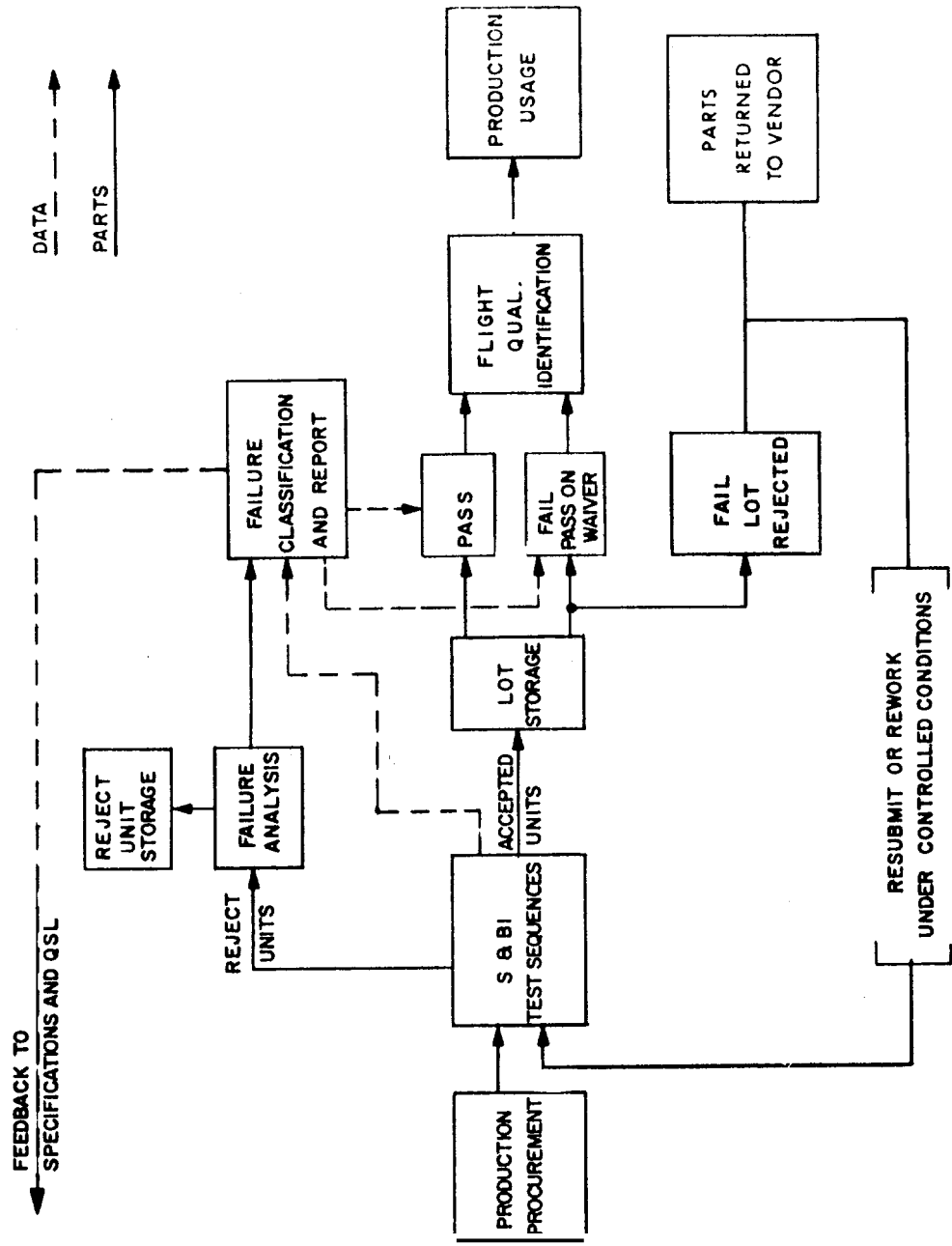


Figure 13

sent for production usage. Only the semiconductor part with the flight qualification part number can be used in flight qualified computer assemblies. From failure analysis, rejected parts proceed to reject storage where they will be available for future study if required. In the event that the lot failed because of circumstances not completely defined through failure classification, the lot can be flight qualified by waiver. The waiver must be authorized by NASA and will accompany the computer. In certain limited cases, parts from a failed lot may be resubmitted for rescreening.

The accumulated data from the screen and burn-in procedure (Fig. 14) and failure analysis are utilized to further evaluate the vendor production capability and his device quality and reliability. This in turn affects a vendor's continued status as a qualified supplier.

S & BI SEQUENCE

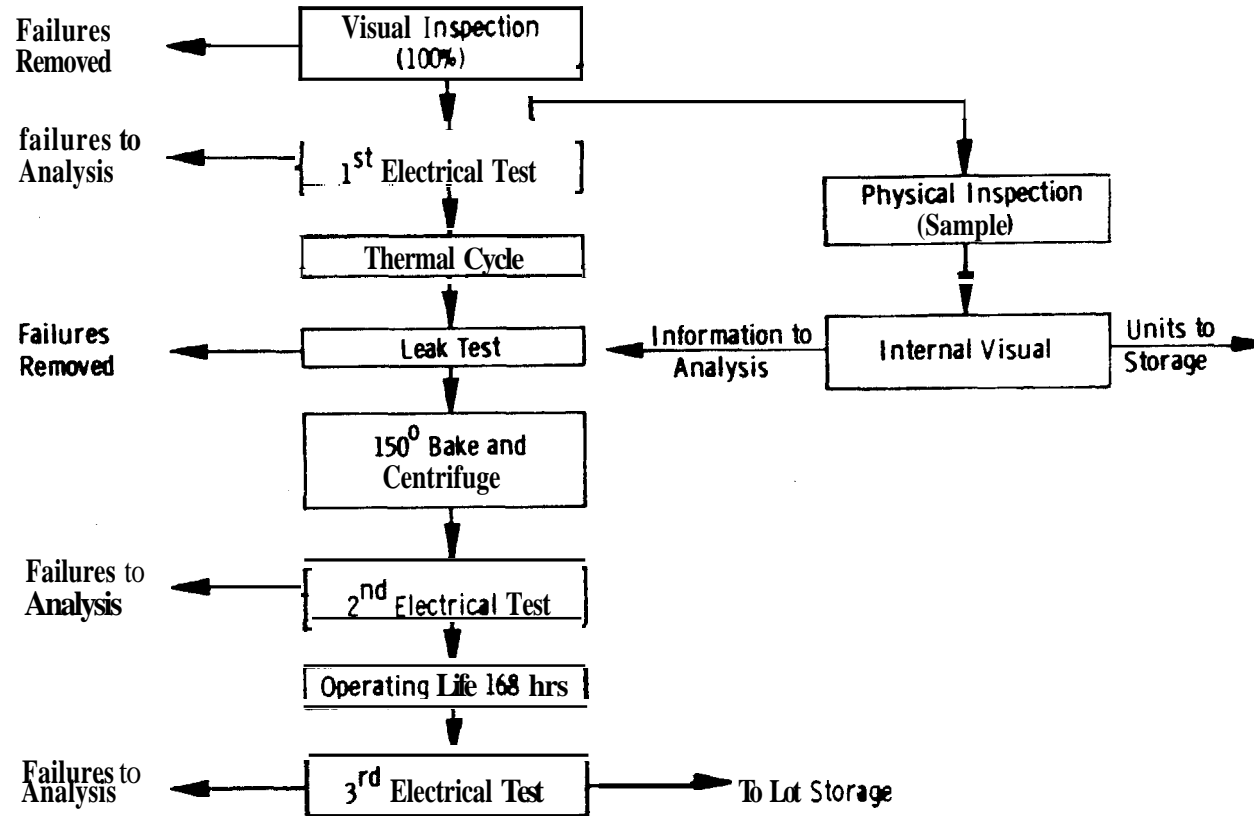


Figure 14

SECTION IV

RELIABILITY HISTORY AND DATA

The reliability history of the NOR Gate will exemplify some of the difficulties encountered and successes achieved in building a digital computer utilizing integrated circuits.

Table II is a summary of the reliability data for the NOR Gate accumulated up to October 1964. This data has been previously discussed in detail² but is presented here to show the extreme differences among manufacturers. The electrical failure definitions during screen and burn-in were any inoperable devices or any device exceeding the electrical specifications. The percentages include approximately 0.05 to 0.1% combined induced failures and testing errors. The initial qualification results are also included in Table II where the failure definition was an inoperable device. The extreme differences among the manufacturers is also reflected in the failure modes generated during both the initial qualification and screen and burn-in. For the data in Table II Manufacturer A rarely exhibited the nonscreenable, and/or long-time dependent failure modes while both Manufacturers B and C consistently did. The inoperable failures generated at computer use conditions for Manufacturers B and C were of the nonscreenable, long-time dependent failure modes.

It is interesting to note that the same devices used to generate the data of Vendor A of Table II have since exhibited a field failure rate of $0.0015\%/10^3$ hours at 90% confidence as of 30 September 1965 with one operational failure. The same devices of Vendors B and C have not improved their failure rates because additional failures have occurred.

The more subtle differences in quality and reliability may be observed in variations of lots shipped from one manufacturer. The data of Fig. 15 indicates the numerical variations

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VENDOR	PRE QUALIFICATION % FAILURES	SCREEN & BURN-IN % FAILURES		FAILURE RATES AT USE CONDITIONS 90% CONFIDENCE
		TOTAL	2nd & 3rd ELECTRICAL	
A	5	1.8	0.3	0.005%/10 ³ hrs (0 FAILURES)
B	26	3.8	1.7	0.3%/10 ³ hrs (2 FAILURES)
C	58	5.0	2.5	1.8%/10 ³ hrs (26 FAILURES)

SEPT 65 : VENDOR A — 0.0015%/10³ (1 FAILURE)
 VENDOR B & C — NO IMPROVEMENT

Table II.

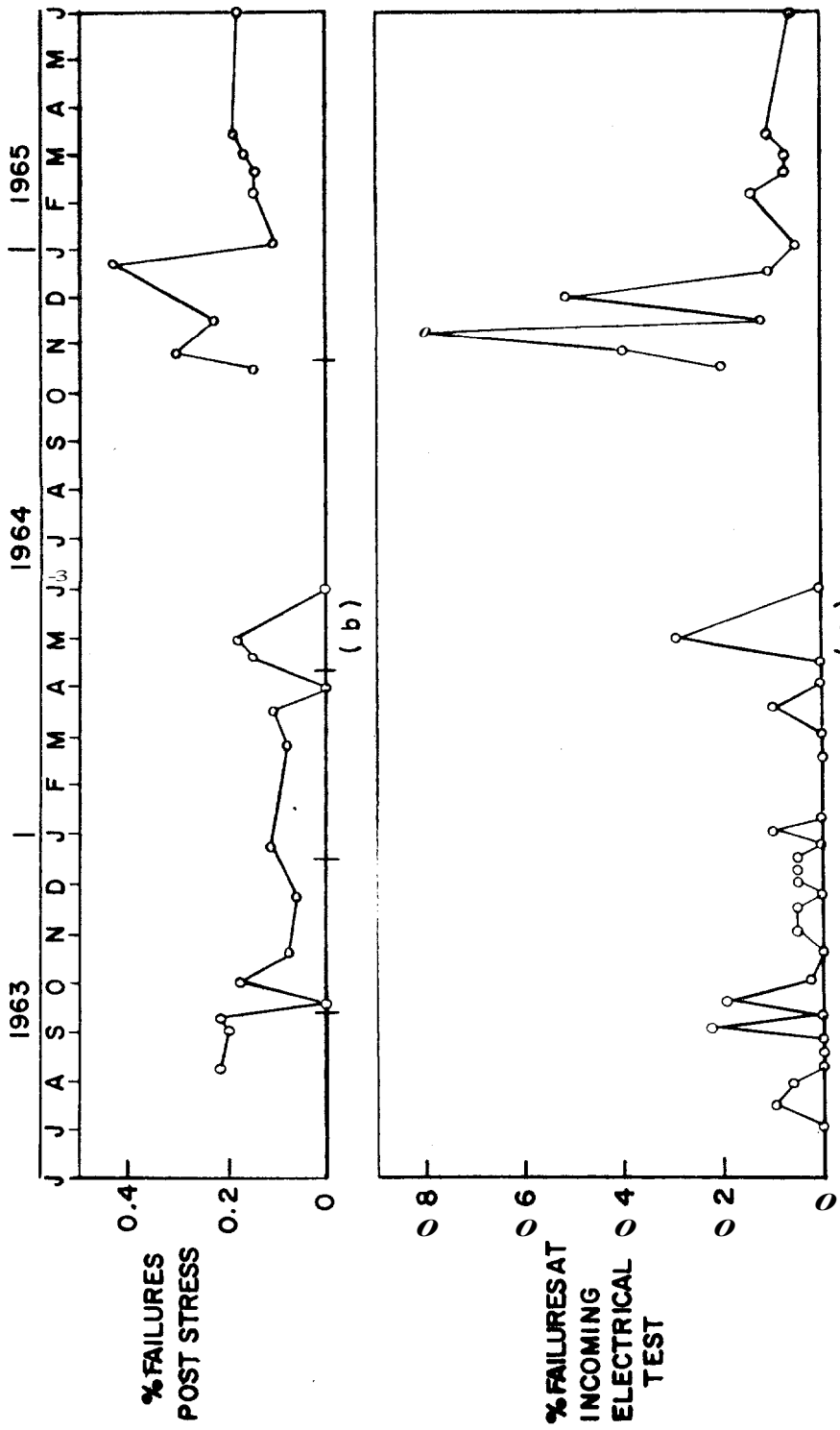


Figure 15

for the NOR Gate from one qualified manufacturer. Here, only the inoperable failures are plotted and induced failures and testing errors have been eliminated from the data. These NOR Gates were exposed to the screen and burn-in procedure as shown in Fig. 14. Each point in Fig. 15 represents a shipment lot of 2000 to 5000 NOR Gates. Figure 15 (a) shows the percent catastrophic failures at the incoming electrical tests. Figure 15 (b) shows the percent catastrophic failures which were generated after stressing with incoming catastrophic failures removed. There are fewer points plotted in Fig. 15 (b) than in Fig. 15 (a), since some lots not used for flight hardware were not exposed to screen and burn-in. There was no buying of the three input NOR Gate between June and October 1964, so that the line producing the integrated circuit was temporarily discontinued. As a result when the production line was reinstated, several lots after October 1964 indicated a new region of instability. At that time rapid feedback to the manufacturer from the customers resulted in subsequent decrease of catastrophic failures during the screen and burn-in procedure.

SECTION V

SUMMARY

Controversy **still** exists with respect to the decision made in the design *of* the Apollo Guidance Computer. In particular standardization of logic gates is claimed to have many disadvantages. But, as a result of standardization the NOR Gates *of* the Apollo Computer has been able to establish the reliability with operating failure rates lower than ever before realized.

To date, fourteen Block I computers have been built and are in field use for flight simulation, spacecraft integration test, and various qualification tests. These computers have accumulated 38,442.0 hours of operating time as of 30 September 1965. The first prototype computer was operating in July 1963 with the Raytheon built flight computer operating in January 1964.

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