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Implementation of Area & Power Optimized VLSI Circuits Using Logic Techniques

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Abstract: *To achieve the reduction of power consumption, optimizations are required at various levels of the design steps such as algorithm, architecture, logic and circuit & process techniques. This paper considers the two logic level approaches for low power digital design. Optimization techniques are carried to reduce switching activity power of individual logic-gates. we can reduce the power by using either circuit level optimization or logical level optimization. In this paper, the circuit level optimization process is followed to reduce the area and power. In the first approach, Modified gate diffusion input (GDI) logic is used in the proposed parallel asynchronous self time adder (PASTA) technique. Similarly, the structure of XOR gate and half adder is reduced to achieve the low area and low power. In second approach, Multi value logic based digital circuit is designed by increasing the representation domain from the two level (N=2) switching algebra to N > 2 levels. The main advantage of this approach is to compensate the inefficiency of existing integrated circuits that are used to implement the universal set of MVL gates. From the results, the proposed GDL logic based Adder offers less number of transistors (area) and low power consumption than the existing technique. And proposed MVL technique allows designing MVL digital circuit that is set to obtain the values from the binary circuits. Also this technique offers low power and small wiring delay, when compared to binary and three value logic. The simulation process is carried out by tanner toolv14.11 to check the functionality of the PASTA & MVL circuits.*

Keywords: *PASTA, Modified GDI logic, Optimized XOR and half adder, MVL, Tanner toolv14.11.*

I. Introduction

A. Proposed Modified Gdi Logic

In day today life, the Systems on Chip (SoC) product are necessary. Millions of chip integrated into one single chip is called as SoC. These millions of chip are integrated into single chip by shrinking the transistor size in each and every chip. Therefore this CMOS technique can apply in SoC product [3]. Carry Select Adder (CSLA) is primarily used to minimize the chip size and for reducing the propagation delay. The parallel asynchronous self time adder (PASTA) is working based on iterative coding. So the number of unwanted activation of clock cycle is removed in this adder to achieve the high speed and low power. This type of adder will be designed in this paper in two ways [10].

The Gate Diffusion Input (GDI) technique is proposed in 2002 to reduce the area and power of VLSI digital circuits. The GDI logic was initially proposed for fabrication in twin-well and Silicon on Insulator (SOI) CMOS methods. It enabled the implementation of a broad range of difficult logic functions using simply two transistors. This scheme was appropriate for the design of regular digital circuits, with a much lower area than existing PTL and Static CMOS methods, whereas offering improved power characteristics. Equally to PTL implementations, the GDI circuits suffered from a decreased swing because of threshold drops. Conversely, a considerably shrinked the logic flexibility and transistor count of the basic GDI cell, gives major power reduction, in spite of the need for swing restoration circuits [1].

B. Proposed MVL Logic

The MVL is also known as multiple-valued, multi-valued or many-valued logic that traces its origins back to the Lukasiewicz logic and Post algebra. The proposed methodology in this work is based on a universal set of gates that is used to implement operators acting on the elements of a domain**.** The current trend in Integrated Circuits (IC) is to embed multiple systems onto a single IC, known as System on a Chip (SoCs) leading to, factors like, an increment in the quantity, the delay time, length, and complexity of the interconnections. The multiple-valued logic is a viable alternative to cope up with the issues due to interconnections, as they are said to decrease the number of the interconnections. This reduction in the area of the IC devoted to the interconnections has motivated many MVL proposals. Methodologies for the synthesis of MVL digital circuits comprise of the operators and their properties. Main drawbacks of such methodologies are: first, the lack of existing integrated circuits that implement the universal set of gates and, second minimization tools needed to design practical MVL digital circuits.

Design Of Adder Using Existing Cscmos Technique

Existing parallel asynchronous self time adder (PASTA) is designed using complementary static CMOS logic for half carry generation and half sum generation, 2:1 multiplexer and complete detection units (CDU) as shown in fig.1. Iterative phase is used to perform the addition operation. For example if we took a=1101, b=1111 & cin=0 means no carry propagation. It means that directly input a & b values are added and generated the sum and carry as outputs. If sel=0 means carry input cin=1, only cin=1 up to first iteration. After that sel=1 and input cin set as 0. From that if the selection line is zero means first path (a, b) values are gives to half adder and selection line is 1 means feedback path is enabled so cin and previous output are sent to half adder. We have to check all the carry values, not zero means this Iteration process is carried out up to all the carry values are set as zero. This kind of adder is called as parallel asynchronous self time adder [7].

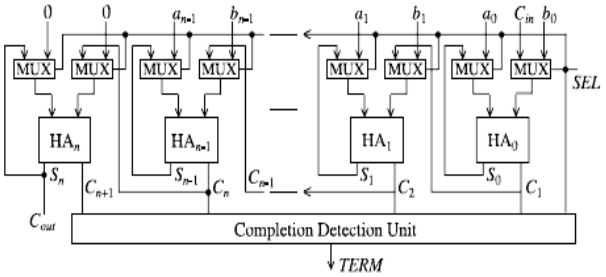


Fig.1 Conventional n-bit PASTA using static CMOS logic.

Structure of conventional half adder is shown in Fig.3. Conventional parallel asynchronous self time adder is reduced by using only half adder instead of full adder and iterative phase. Multiplexer having 2 main inputs (i0 and i1) and one control input (sel) to produce the only one output (x). Multiplexer circuits consists of 6 PMOS and 6 NMOS which is connected as shown in Fig.2 [12]. In the existing half adder circuits consists of 5 PMOS and 5 NMOS for sum generation and 3 PMOS and 3 NMOS for carry generation. Totally 16 transistors are required to design the existing half adder circuits using static CMOS technology. If the input x0 is 0 and x1 is one, PMOS_3 and NMOS_2 is on. So PMOS_3 value is zero, which enter into inverter, Hence the final half adder sum output is one. Similarly for carry generation for same inputs is checked, PMOS1 and PMOS2 is on which is connected to vdd so the output is 1. But it is connected to the inverter so final carry output is 0 when x0=0 and x1=1. Accordingly, all other inputs are processed to produce the correct output [6].

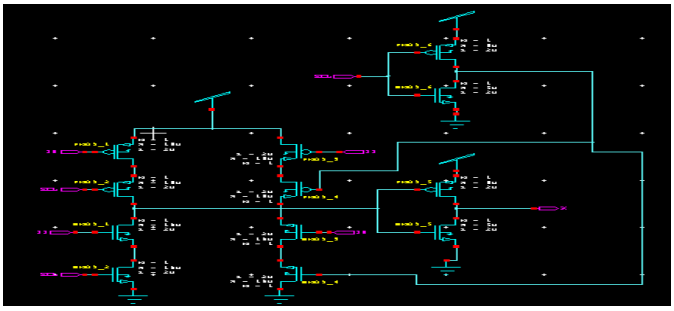


Fig.2 Schematic diagram of conventional multiplexer using Static CMOS technique.

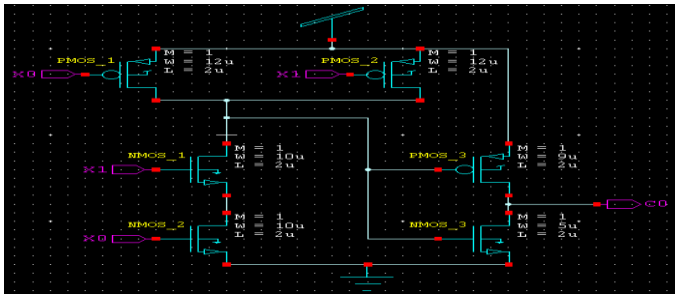


Fig.3 Schematic diagram of existing half adder using Static CMOS technique.

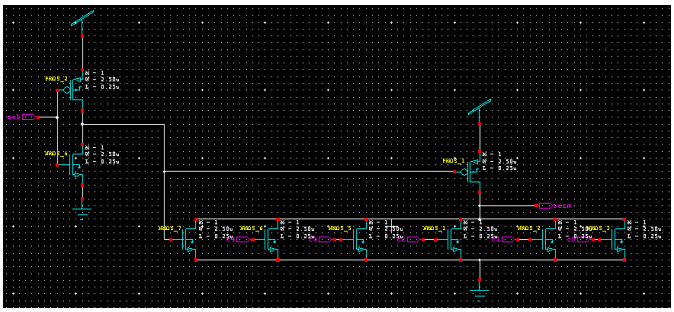


Fig.4 Circuit diagram of existing CDU using Static CMOS technique.

The conventional complete detection unit (CDU) gate is designed using static CMOS method as shown in Fig.4. The output of CDU is generated based on NOR operation. If the sel input and all the carry inputs are zero means the output of CDU is one [8]. Otherwise the output is zero. Further to decrease the power consumption and a number of transistors in the conventional PASTA, the optimum half adder structures are established in the proposed systems.

II. Proposed Pasta Using Modified GDI Logic

The proposed parallel self time adder is designed using optimized half adder structures and modified gate diffusion input (GDI) logic. The proposed half adder circuit is constructed using only 10 transistors instead of 16 transistors; Multiplexer is designed using 6 transistors instead of 12 transistors; Also the reduced NOR gate is applied in the proposed PASTA circuit. The enhanced half adder is proposed by using only 10 transistors based on GDI technology. All these components are integrated into existing parallel self time adder as shown in Fig.5. Comparison between existing PASTA with regular multiplexer, NOR gate and half adder structure and proposed PASTA with optimized multiplexer, NOR gate and half adder constructions is achieved to analyze these functionality, area utilization and power consumption.

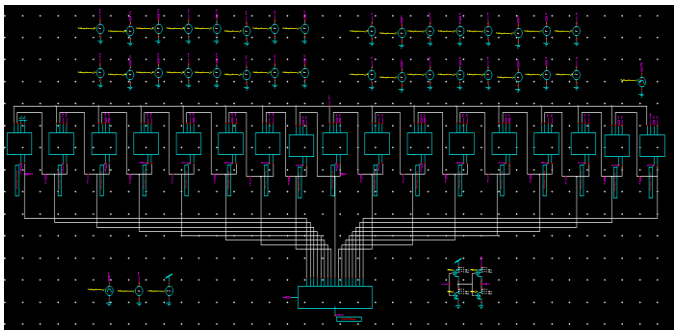


Fig.5 Schematic diagram of proposed 16-bit PASTA using GDI logic.

The circuit diagram of simplified half adder is shown in Fig.6. It requires only 10 transistors, instead of 16 transistors when we applying GDI logic. In this paper, the half adder is designed by using the NOR gate instead of XOR gate to reduce the number of transistors. Two NOR gates are used to generate the sum output and only one and gate are used to generate the carry output. Reuse technique are followed to reduce the half adder structure.

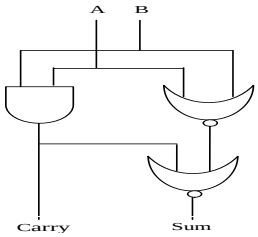
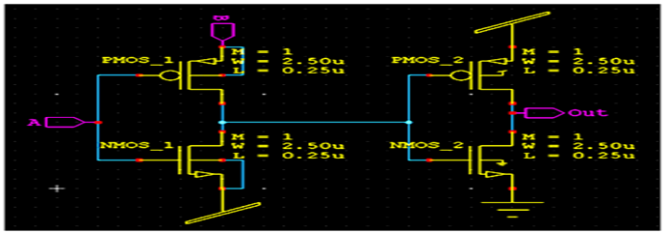
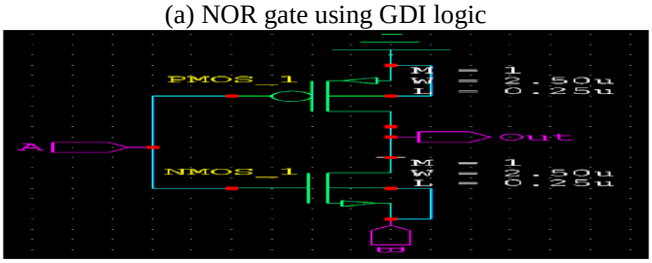


Fig.6 Structure of reduced half adder for proposed PASTA.



(a) NOR gate using GDI logic



b) AND gate using GDI logic

Fig.7 Structure of reduced NOR & AND gates for reduced half adder using GDI logic.

The reduced NOR gate using GDI logic is shown in Fig.7 (a). The PMOS_1 is on, when the inputs a=0 and b=0. But the source terminal of PMOS_1 is connected to the input b. So the intermediate output is b (zero). This output is given to the inverter. i.e the NOR gate output is one. If the inputs a=0 and b=1, PMOS_1 is on. But the PMOS_1 source terminal is connected to b so b (one) value is passed to the next stage inverter. Hence the NOR gate output is 0. Similarly all other inputs combination is given to make the NOR gate output. The reduced circuit of GDI logic based AND gate is shown in Fig.7 (b). The PMOS_1 is on, when the inputs a=0 and b=0. So the output of improved AND gate is zero. If the inputs a=0 and b=1, PMOS is on and NMOS is off, which is connected into gnd as source terminal. Hence the output of AND gate is 0. PMOS off and NMOS on, when the inputs a=1 and b=0. But the drain terminal of NMOS_1 is connected to the input b. So the modified AND gate output is zero. If the inputs a=1 and b=1, NMOS_1 is on. But the input b is connected as drain terminal of NMOS_1. So the output of modified GDI logic based AND gate is one.

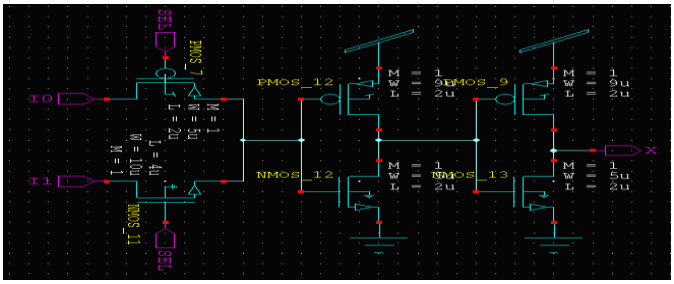
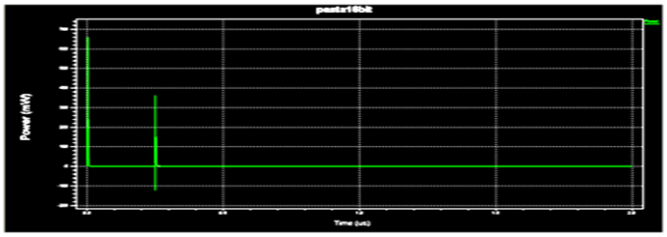


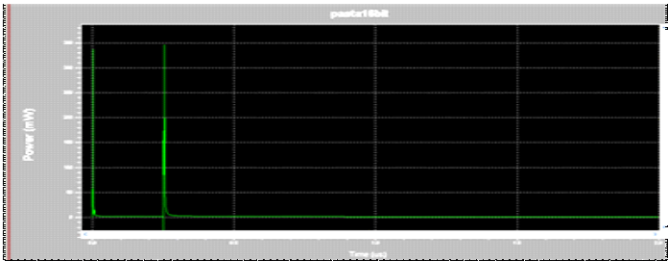
Fig.8 Structure of reduced MUX using GDI logic.

III. Results And Discussion

In this paper, the design of modified parallel asynchronous self time adder with optimized NOR gate, Multiplexer and half adder is presented for low power and low area applications. The modified parallel asynchronous self time adder and conventional parallel asynchronous self time adder are designed and implemented using Tanner14.11 to analyze the power and this adder functionality. The Table.1 illustrates the Maximum Power of modified parallel asynchronous self time adder over conventional parallel asynchronous self time adder using different CMOS technology.



Power of Existing 16-bit PASTA



Power of proposed 16-bit PASTA

Fig.9 Power output of existing and proposed PASTA

Table 1. Comparison of existing and modified parallel asynchronous self time adder

Adder Types	**Existing PASTA**	**Proposed PASTA**
	Max power (mW)	**Max power (mW)**
8-bit	446	211
16-bit	630	345

From the results, the proposed 8-bit PASTA offers 52.6% maximum power reduction than the conventional PASTA technique. The modified 16-bit PASTA provides 45% maximum power reduction when compared to the existing PASTA.

Table 2. Comparison between existing and proposed PASTA for area utilization.

Adder Types	Existing PASTA	Proposed PASTA
	Number of transistors	Number of transistors
4-bit	211	125
8-bit	375	215
16-bit	703	401
Half adder	16	10
Multiplexer	12	6

The table.2 describes the area utilization of different type of adder with different size; the proposed parallel asynchronous self time adder offers 41%, 43%, 42.9% area reduction for 4-bit, 8-bit and 16bit adders than the existing parallel asynchronous self time adder. To reduce the number of transistor, GDI logic is used in the proposed PASTA in the transistor level. Also logic level simplification is performed to reduce the number of gate.[13]

IV. Proposed Full Adder, Half Adder & Multiplexer Using Multi-Value Logic

The main aim of this paper is to reduce the power and wiring delay of the digital circuits based on multi-value logic. Less number of wires will used for designing a digital circuit. So the power consumption of the circuits is very low. Since it require half the number of digits to store any information than its binary equivalent; it is good for storage; the quaternary storage mechanism is less than twice as complex as the binary system. The truth table of MVL based half adder is shown in table.1.Similarly, the truth table of full adder is used to check the functionality of MVL based full adder with 16 input combinations.

Table.1 Truth table of half adder using MVL

A	**B**	**S**	**C**
0	0	0	0
0	1	1	0
0	2	2	0
0	3	3	0
1	0	1	0
1	1	2	0
1	2	3	0
1	3	0	1
2	0	2	0
2	1	3	0
2	2	0	1
2	3	1	1
3	0	3	0
3	1	0	1
3	2	1	1
3	3	2	1

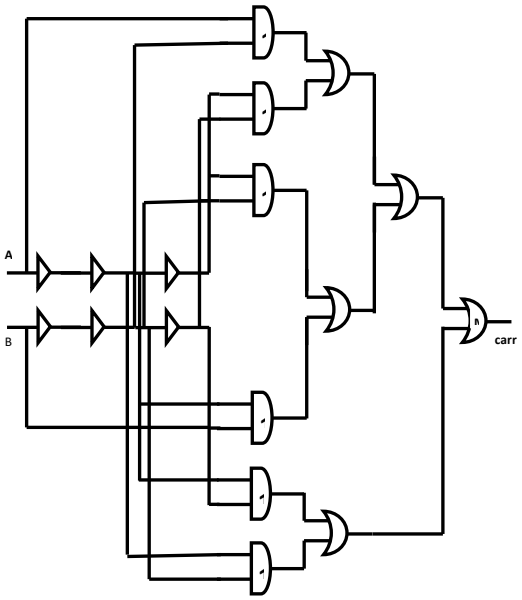


Fig.1 New circuit diagram of MVL logic based half adder for carry generation

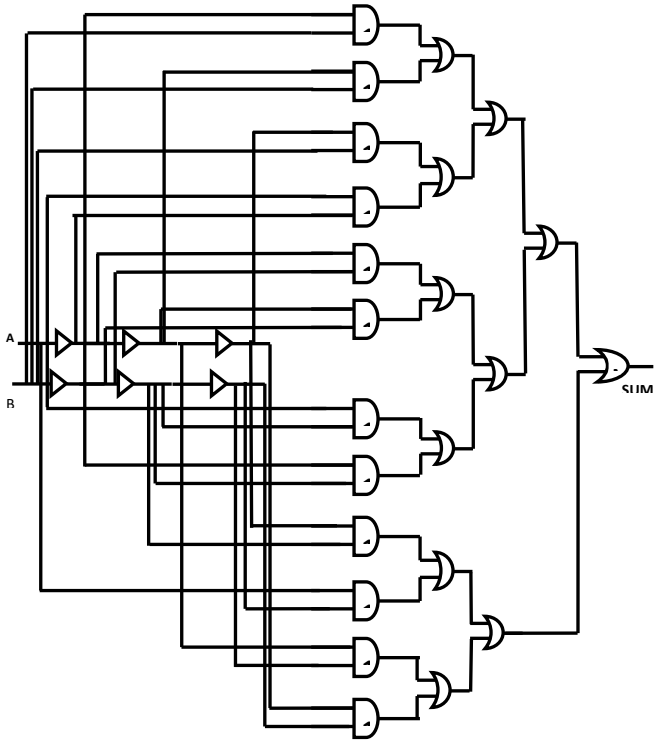


Fig.2 New circuit diagram of MVL logic based half adder for sum generation

Novel circuit diagram of MVL logic based half adder for carry and sum generations are shown in fig.1 and fig.2. Similarly, Three Inverters are used to design MVL logic based multiplexer, half adder and full adder circuits. It will works as

- **07 Inverter:**
  0-0.7v, Input=0, Output=1.
  Above 0.7 to 3.3V, Input =1 and Output =0.
- **14 Inverter:**
  0-1.4v, Input=0, Output=1.
  Above 1.4 to 3.3V, Input =1 and Output =0.
- **22 inverter:**

0-2.2v, Input=0, Output=1.
Above 2.2 to 3.3V, Input =1 and Output =0.

For eAND1, inputs X & Y =1 => output=>1, otherwise 0.
For eAND2, inputs X & Y =2 => output=>2, otherwise 0.
For eAND3, inputs X & Y =3 => output=>3, otherwise 0.

In the successor input=>0 means corresponding output =>1, input=>1 means corresponding output =>2, input=>2 means corresponding output =>3 and input=>3 means corresponding output =>0.

Similarly, MAX gate (M) is used to select the maximum value from the two or more numbers. Two half adder are used to design the one full adder by using a new half adder circuit.

V. Results & Discussion

In this paper, a new half adder, full adder is designed for optimized adder and multipliers circuits. The multi-value logic based half adder and full adder is mainly used to reduce the wiring delay and power by giving the more than three inputs into one input line. Also 250nm and 65nm CMOS circuits are designed by reducing the supply voltage and width and length of the PMOS and NMOS. So the wiring delay is reduced, which leads to the low power consumption. Improved Multi-value logic is worked based on some logical reduction in the circuit level. Logical reduction is done by using some digital theorem. The simulation is performed in Tanner Toolv14.11. The schematic circuit of half adder is shown in fig.3 and fig.4 for sum and carries generation.

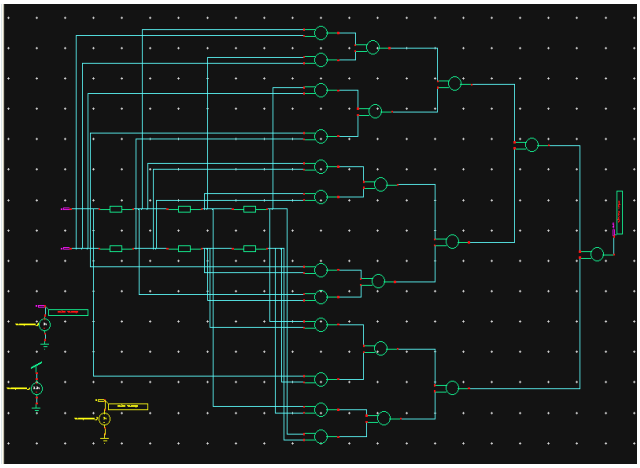


Fig .3 Schematic diagram of MVL logic based half adder for sum generation

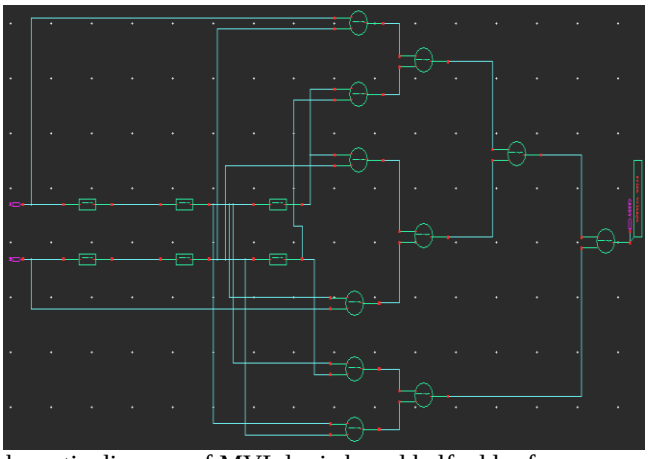


Fig.4 Schematic diagram of MVL logic based half adder for carry generation

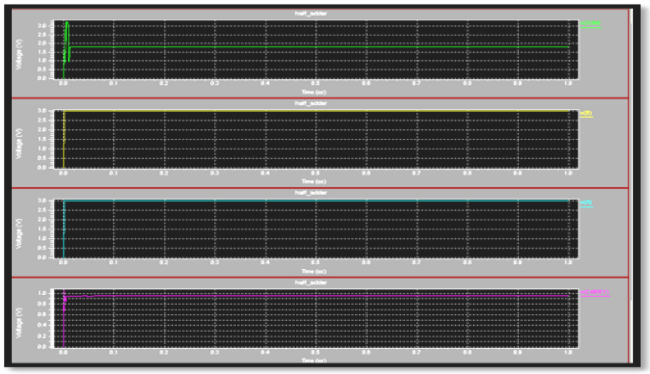


Fig.5 Simulation output of MVL half adder

The simulation output of half adder is shown in fig.5. The output is checked by using the truth table of half adder as in table.1. When the input a=3 and b=3, the corresponding output sum is 2.1V and carry is 1.4 v that is 2 and 1. Similarly all other input are processed to generate the exact output of MVL half adder.

Table.2 Comparison of power consumption for full adder, half adder and MUX using 250nm

Results for 250nm	Full adder	Half adder	MUX
Maximum Power	1.15w	556mw	339mw
Average Power	36mw	15mw	5.03mw

Table.3 Power consumption for full adder, half adder and MUX using 65nm

Results for 65nm	Full adder	Half adder	MUX
Maximum Power	178.5mw	91.6mw	56.7mw
Average Power	4.66mw	2.77mw	1.68mw

The power consumption of full adder, half adder and multiplexer by using 250nm and 65nm are presented in table.2 and table.3. The MVL logic based 65nm full adder, half adder and multiplexer circuits offers low maximum power and average power than the existing 250nm based full adder, half adder and multiplexer circuits.

Table.4 Comparison between existing and proposed MVL circuits

Circuit	Existing Delay (ns)	Proposed Delay (ns)
MUX	10.232	8.875
Half adder	11.93	9.67
Full adder	1.87	1.51

The comparisons for existing and the proposed delay circuits is represented in Table 4.There is a reduced delay offered by multiplexer circuits, full adder, half adder for an MVL logic which is based on its size 65nm than those in terms of time scaled in nanoseconds for an existing delay. As per the observations in current work, the multiplexer proposed (based on MLV) is said to offer a delay reduction of 13.2% which is comparatively efficient based on existing multiplexer circuits. And not just its impact on multiplexer is effective, but the half adder and full adder circuits tend to exhibit a delay reduction of 18-19.5% than the existing adder circuits. A special tool, T-spice tanner is used to obtain the results, by initiating the .measure command. And thereby, the performance in measure of speed of the proposed MVL circuits tend to produce a high output.[14]

VI. Conclusion

In this paper, Two approaches are discussed one is the design of reduced multiplexer and half adder is proposed using Gate diffusion Input (GDI) logic. The proposed half adder needs only 10 transistors instead of 16 transistors; multiplexer needs 6 transistors instead of 12 transistors. This gate, mux and half adder have been integrated in the Modified PASTA with GDI logic without buffer in the end of the half adder. In the proposed GDI PASTA Adder, voltage drop is reduced in the modified GDI logic based half adder than the ordinary GDI logic. The simulation result shows that the proposed CSLA consumes low power and requires less number of transistors than the conventional CSLA. In the second approach, the proposed MVL gates allow designing of any MV Logic digital circuit taking advantage of the knowledge coming from the binary circuits by extending it to the MVL digital circuit synthesis. Further work will be performed in order to improve electronic gates characteristics such as frequency, delay, fan-in, and fan-out. Future work is also related to the design and implementation of minimization MVL states and gates.

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