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Overview and Future Challenge of Ferroelectric Random Access Memory Technologies

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We have developed a low-temperature formation technique for ferroelectrics (<500 °C), which is crucial for the ferroelectric random access memory (FeRAM) to be embedded in a leading-edge complementary metal oxide semiconductor (CMOS). A 53-nm-thick $Bi_4Ti_3O_{12}$ film was successfully formed by metalorganic chemical vapor deposition at 450 °C and subsequent annealing at 500 °C. It was found that perovskite grains preferentially orient along the (110) and (111) directions and that the fabricated $Bi_4Ti_3O_{12}$ capacitors show a remnant polarization ($2P_r$) of as large as 25.7 μC/cm^2. In addition, we have adopted a nondestructive readout operation (NDRO) technique to extend read cycle endurance, in which the switched polarization at reading is automatically rewritten by readout voltage removal. We have demonstrated stable readout characteristics at more than 10^{11} cycles for 0.18 μm NDRO FeRAMs. [DOI: 10.1143/JJAP.46.2157]

KEYWORDS: ferroelectric random access memory, security, power consumption, design productivity, $SrBi_2Ta_2O_9$, $Bi_4Ti_3O_{12}$, nondestructive readout operation

1. Introduction

The implementation of ferroelectric random access memory (FeRAM) technology can enhance the performance and functionality of system-on-a-chips (SoCs). Among various ferroelectrics, bismuth-layered perovskite materials, such as $SrBi_2Ta_2O_9$ (SBT), can particularly provide SoCs with high-read/write-speed, low-voltage and fatigue-free memory performance characteristics.[1] However, until now, FeRAM technology has been two or three generations behind leading-edge complementary metal oxide semiconductor (CMOS) technology. In addition, the read cycle endurance of FeRAMs, typically less than 10^{12} cycles, is not sufficient for SoCs. Therefore, we require a drastic technology transition in FeRAM materials, processing and readout scheme to catch up with the leading-edge CMOS technology.

In this paper, we discuss FeRAM solutions for secure data storage, low-power consumption and a high design productivity, which are vital issues of the leading-edge CMOS technology.[2–4] For the security issue, the structural robustness of a stacked ferroelectric capacitor can stand off malicious attacks using microprobes. For the power crisis, standby power can be completely removed in power-managed systems by incorporating nonvolatile flip-flops with ferroelectric capacitors. For the design productivity issue, reconfigurable hardware, which can change its function on the basis of the configuration data in ferroelectric capacitors, can greatly reduce the number of LSIs to be designed. To clarify the issues for realizing such FeRAM solutions, we first overview the current status of process technology. Then our latest results of the low-temperature formation of ferroelectrics are described. Furthermore, we describe a nondestructive readout operation (NDRO) scheme that can effectively extend read cycle endurance and demonstrate a stable readout operation at more than 10^{11} cycles for a 0.18 μm NDRO FeRAM.

2. FeRAM Solutions for Leading-Edge CMOS

2.1 *Secure data storage*

An electronic wallet has recently allowed us to shop without cash. In the electronic wallet, personal information is encrypted by an encryption circuit and stored in a nonvolatile memory. To avoid thefts of the information during data transfer through wire connections, the nonvolatile memory is already embedded in LSIs with the encryption circuits. The strength of security is heavily dependent on the nonvolatile memory contained in the device. An embedded FeRAM can provide secure systems compared with an electrically erasable programmable read-only-memory (EEPROM) device, in which the stored data can be read by connecting microprobes to the source and drain electrodes [Fig. 1(a)].[5] As ferroelectric capacitors are stacked on pass transistors,[6] microprobing on the electrodes of the pass transistors would destroy the data stored in the ferroelectric capacitors [Fig. 1(b)]. Even if probing is possible through a particular method, the amount of polarization charge is too small to distinguish a difference between datum "0" and "1" due to the parasitic capacitance on the probe. Therefore, the accumulation of the polarization charge by applying repeated pulses is necessary to improve signal-to-noise ratio. However, when a pulse sequence is applied to ferroelectrics for reading data, the stored polarization is destroyed. Accordingly, the structural robustness of FeRAM provides secure data storage.

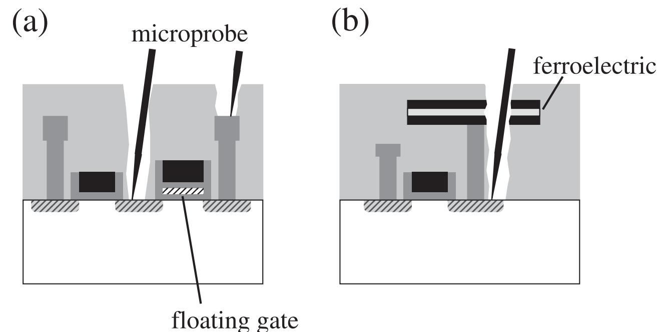

Fig. 1. Cross-sectional drawings of (a) EEPROM and (b) FeRAM cells.

2.2 *Low-power consumption*

As the semiconductor technology moves toward the 65

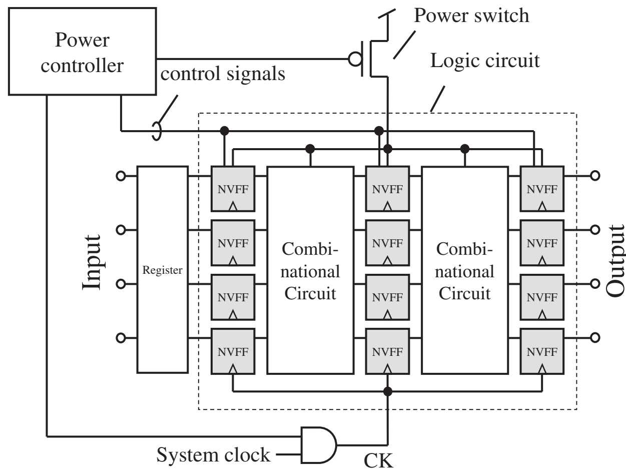

Fig. 2. System diagram of power-managed circuit with NVFFs.

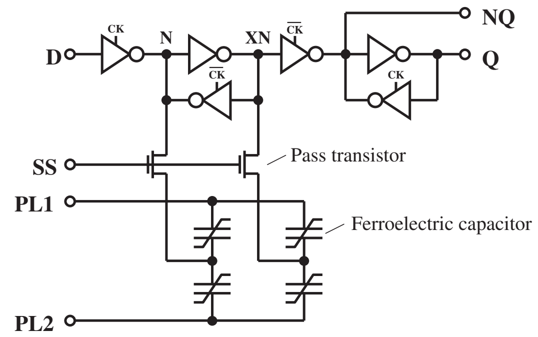

Fig. 3. Circuit schematic of NVFF with ferroelectric capacitors.

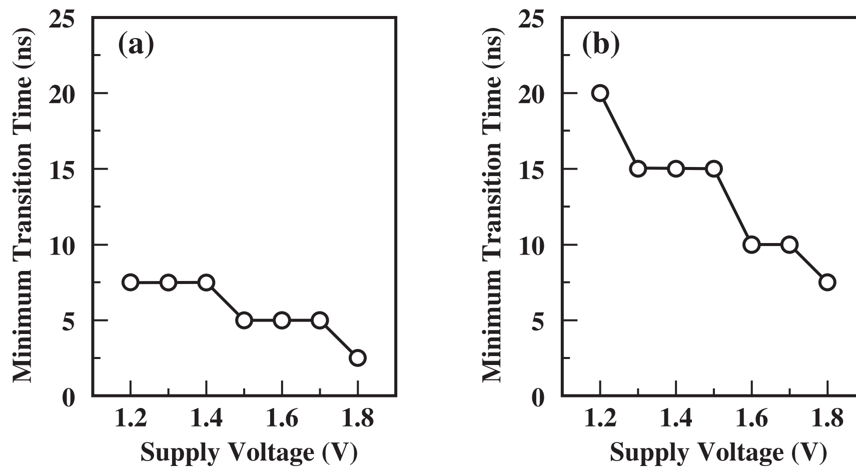

Fig. 4. Minimum transition times as function of supply voltages for getting (a) into and (b) out shutdown mode.

and 45 nm nodes, leakage currents through gate oxide films and subthreshold leakage currents on MOS transistors become so large that the standby power consumed in SoCs due to wasteful leakage current becomes larger than the active power required for operation.[3)] By replacing the static random access memories (SRAMs) incorporated in SoCs by FeRAMs, the power supply voltage applied to the memories can be removed during standby. As SRAMs occupy a large area in an SoC, standby power can be effectively reduced by the replacement.

The remaining standby power consumed in logic segments can be reduced by introducing power-managed circuits, which turn the power off when the circuits have no task to perform. The power-managed circuits consist of combinational circuit elements, nonvolatile flip-flops (NVFFs) and a power switch (Fig. 2). In the NVFFs, ferroelectric capacitors are connected to the data latch nodes in flip-flop circuits (Fig. 3) to hold data without power supply. Prior to the state transition to a shutdown mode, the data at nodes N and XN in the NVFFs are acquired in the pairs of ferroelectric capacitors by applying voltage pulses to PL1 and PL2. During the shutdown period, the supply voltage V_{DD} is completely removed by turning the power switch off. To reactivate the NVFFs, the refuge data are recalled from the pairs of ferroelectric capacitors to the data latch nodes N and XN by applying a voltage pulse to PL1 and keeping PL2 grounded. Then, the voltage difference across the two nodes is amplified by cross-coupled inverters. As fast transitions for getting into and out of the shutdown mode enable frequent power-off of the power-managed circuits, a fast write/read operation of the NVFFs can effectively reduce the standby power of the circuits. In addition, the size of registers that hold input data during the recall operation can be reduced.

To evaluate the operational speed of the NVFFs, we have integrated the NVFFs into a 0.18 μm CMOS logic with four-level metals using $SrBi_2Ta_2O_9$ (SBT) capacitors.[7)] Figure 4 shows the transition times of the NVFFs taken to get (a) into and (b) out of the shutdown state as a function of V_{DD}. The transitions for getting into and out of the shutdown period have been completed within 2.5 and 7.5 ns, respectively, at 1.8 V. These transitions are ten times faster than those of the NVFFs using $Pb_{1-x}Zr_xTiO_3$ (PZT) capacitors reported thus far.[8,9)] It is considered that the fast transitions are attributed to the low dielectric permittivity of SBT ($\varepsilon_r \sim 300$) compared with that of PZT ($\varepsilon_r \sim 700$). Accordingly, the NVFFs with SBT capacitors can effectively reduce the standby power of power-managed systems with frequent transitions.

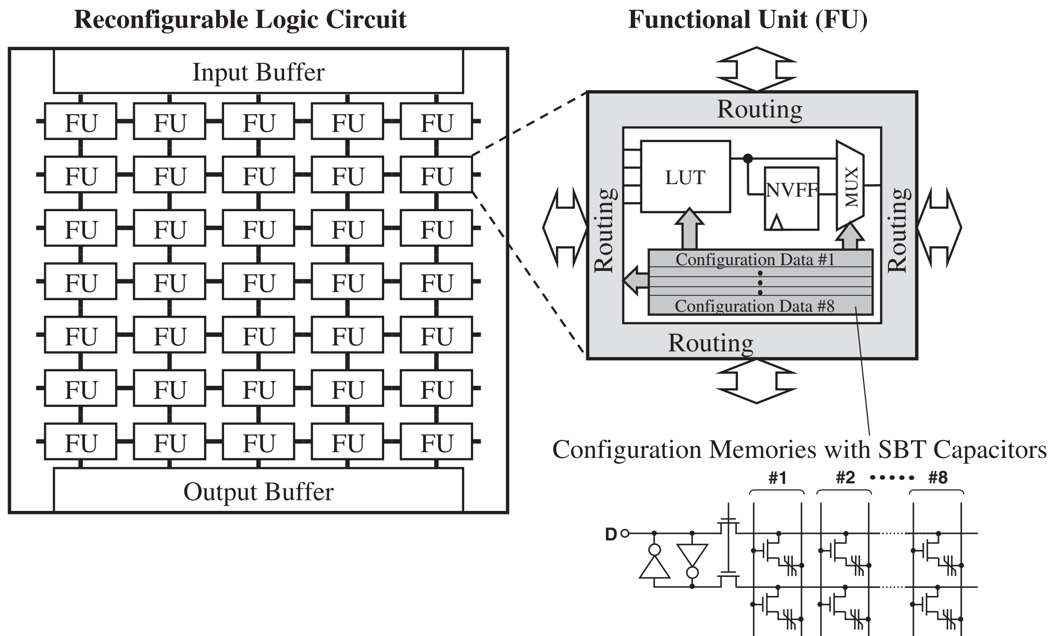

Fig. 5. Circuit diagram of reconfigurable logic circuit incorporating configuration memories with ferroelectric capacitors in each functional unit.

2.3 Hardware convergence

As the semiconductor technology progresses, more functions are implemented in SoCs. However, a high integration of functions leads to a decline in design productivity.[4] To overcome design complexity, dynamic reconfigurable circuits that exhibit structural flexibility, such as software, and operate at a high speed, such as hardware, have attracted considerable attention recently.[10] Masui *et al.* reported a dynamic reconfigurable circuit, which incorporates ferroelectric SRAM cells.[11] They demonstrated data encryption by dynamically changing its function on the basis of the configuration data stored in the ferroelectric SRAM cells. However, the ferroelectric SRAM cell consisting of six transistors and four ferroelectric capacitors is too large to be used as a high-density configuration memory device.

To improve the density of configuration memories, we have implemented ferroelectric memory cells composed of two SBT capacitors and two pass transistors in a reconfigurable circuit by 0.18 μm FeRAM technology.[6] Figure 5 shows a block diagram of the fabricated reconfigurable circuit consisting of a 16×32 functional unit (FU) array and routing interconnects (RIs). The reconfigurable circuit can perform one of the eight different functions, such as encryption, decryption, and communication protocols, on the basis of the configuration data stored in the ferroelectric memories. Figure 6 shows two different configuration instances, (a) a key entry function followed by (b) a data encryption function. As the ferroelectric memories are directly connected to a lookup table (LUT), a multiplexer (MUX), and the RIs, the context of the reconfigurable circuit can be altered within 1 μs. Furthermore, when the key entry function is executed, the NVFFs incorporated into the FU hold the key. Thus, key entry operations at every encryption operation can be eliminated and opportunities for the theft of the key can be reduced.

Although the logic density of current reconfigurable circuits is too low to be applied in high-end applications, various functions converge with the reconfigurable circuits when the FeRAM technology catches up with the leading-edge CMOS technology.

3. Process Technology

To clarify the issues for realizing the FeRAM solutions described above, we first overview the current status of process technology. Traditionally, the process compatibility of the FeRAM technology allows successful implementation of a FeRAM in CMOS devices without any circuit design modifications (Fig. 7). At the 0.6 μm node, planar capacitor technology was used with a spin-coating technique. At the 0.18 μm node, a planar capacitor surrounded by a hydrogen barrier is stacked on a pass transistor, which withstands hydrogen attacks during a CMOS back-end process.[6] The memory cell size is then dominated by the capacitor area. As the planar capacitor is not allowed for much tighter density transistors at the 130 nm node, a three-dimensional (3D) capacitor structure is required to reduce a footprint. Then, a metalorganic chemical vapor deposition (MOCVD) technique is required to form a 3D ferroelectric film on a topographic electrode. At the 65 nm node and beyond, ferroelectric films have to be formed at temperatures lower than 500 °C, because process temperatures higher than 500 °C cause an anomalous increase in the sheet resistance of nickel–silicide (NiSi) layers for ultrashallow junctions.[12] However, when an SBT film is annealed at temperatures lower than 650 °C, an undesired phase, which is a fluorite phase, appears and results in nonperovskite.[13] Therefore, a somewhat drastic technology transition is required in FeRAM materials and processing to catch up with the leading-edge CMOS technology.

To reduce the process temperature, $Bi_4Ti_3O_{12}$ (BIT) is preferred rather than SBT, because the presence of the fluorite phase in BIT has not been reported thus far. A 53-

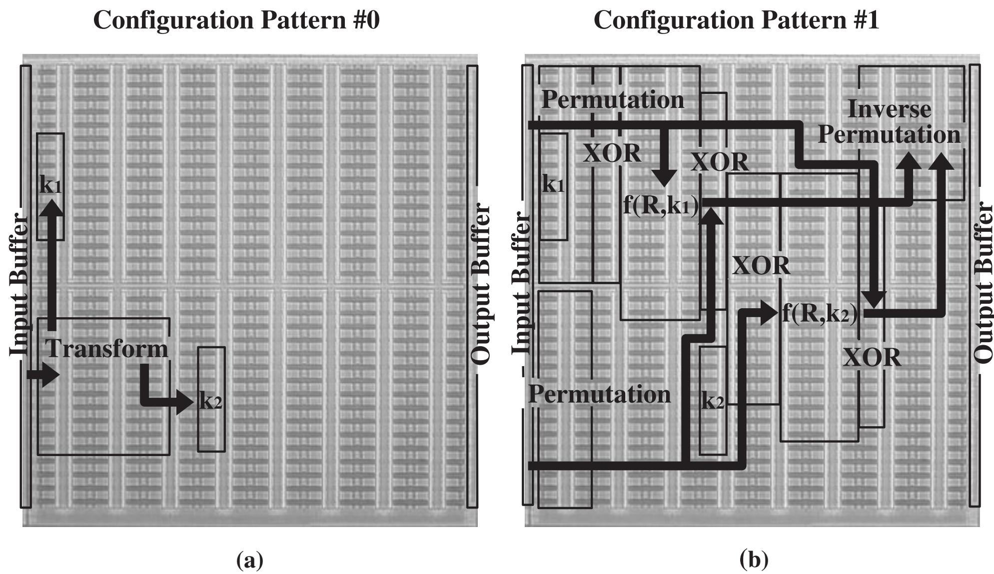

Fig. 6. Configuration patterns for (a) key entry and (b) data encryption functions.

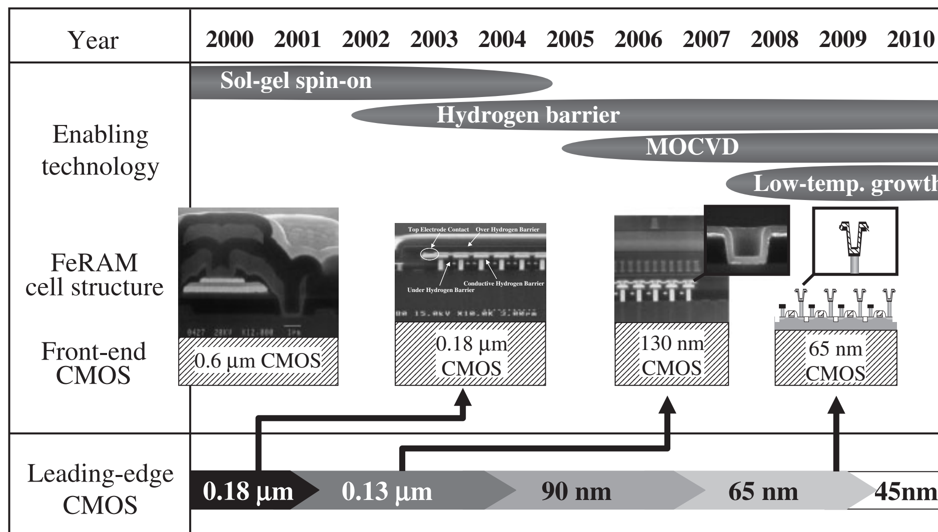

Fig. 7. Technology trend of embedded FeRAM.

nm-thick BIT film was deposited on a Pt-covered substrate at 450 °C by MOCVD and annealed at 500 °C for 1 min in atmospheric oxygen by RTA. For structural characterization, the BIT film was analyzed by electron backscatter diffraction (EBSD) and the EBSD patterns assigned to the perovskite phase were observed on the entire surface of the BIT film. The crystal orientation map calculated from the EBSD patterns showed that perovskite grains preferentially orient along the (110) and (111) directions, as shown in Fig. 8.

For electrical characterization, Pt electrodes were deposited on the BIT film via a shadow mask. The P–V hysteresis curve of the BIT capacitor shows $2P_r$ of 25.7 µC/cm^2 (Fig. 9). This $2P_r$ is higher than those previously reported for (117)- or (00l)-oriented BIT films.[14,15] We speculate that the (110)- and (111)-oriented grains contribute to $2P_r$ efficiently, because the polarization component normal to the electrode of the (110)- or (111)-oriented grains is much higher than that of the (117)- or (00l)-oriented grains.

4. Read Cycle Endurance

As we discussed above, the FeRAM technology can provide solutions for SoCs. The read cycle endurance of FeRAMs, typically less than 10^{12}, is sufficient for the solutions of secure data storage and low-power consumption, in which the readout interval is longer than 1 µs. However, the number of read cycles is too small to realize hardware convergence using dynamic reconfigurable circuits, in which configuration data are read at every clock cycle for the most frequent case. Therefore, the read cycle endurance has to be improved to realize hardware convergence with FeRAMs. Before an explanation of our approach to extend the readout cycle endurance, we overview the issue.

Typically, FeRAM cell consists of a pass transistor and a ferroelectric capacitor [Fig. 10(a)], in which a binary polarization state is stored. At readout operation, the stored polarization is switched. Thus, a subsequent rewrite operation is required to restore the switched polarization.[16] As

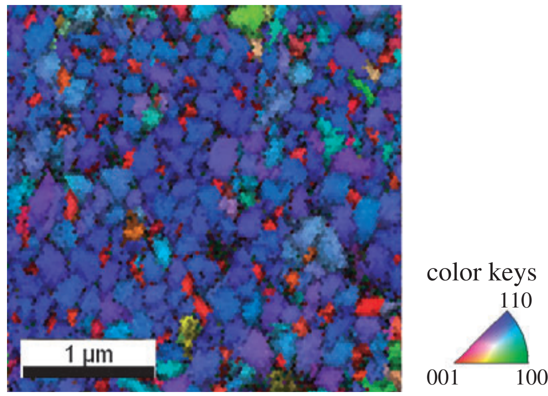

Fig. 8. Crystal orientation map of BIT film.

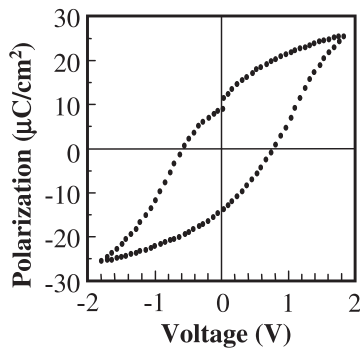

Fig. 9. P–V hysteresis curve of BIT capacitor.

the readout operation is repeated, polarization switching causes ferroelectric fatigue. To read the polarization without switching, a ferroelectric gate transistor has been investigated [Fig. 10(b)], in which a ferroelectric material is used as a gate insulator. As the stored polarization changes the channel conductance, the stored datum can be read out by drain–source current sensing. Since no bias is applied to the ferroelectric during the readout operation, polarization switching has never occurred. For realizing the ferroelectric gate transistor, several device structures have been proposed.[17–19] However, this approach may extinguish the advantage of conventional FeRAMs that can be embedded in CMOS wafers without process modifications, because the fabrication of the ferroelectric gate structure on CMOS wafers has not been sufficiently investigated.

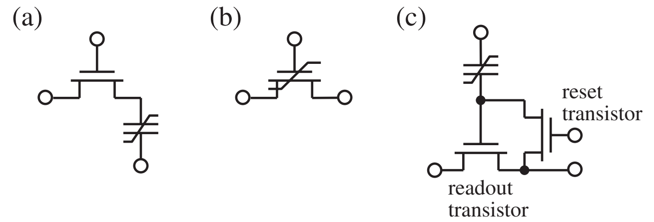

Fig. 10. Memory cell architectures for (a) 1T1C structure and (b) MFS (c) NDRO cells.

We have proposed an NDRO technique, which can be developed using an existing FeRAM process and can realize a long retention time, over ten years.[20,21] In the developed NDRO technique, a ferroelectric gate transistor is fabricated by connecting a gate electrode of a readout transistor and a ferroelectric capacitor [Fig. 10(c)]. The binary datum "1" or "0" is programmed on the ferroelectric capacitor on the basis of the voltage applied to both capacitor electrodes whether a voltage at the top electrode is high or low. After the programming operation, both capacitor electrodes are grounded by turning a reset transistor on. In this scheme, the polarization can be fully saturated and no bias is applied to the ferroelectric capacitor during the storage period. Therefore, this NDRO technique provides a long retention characteristic, which can be expected to be equivalent to the existing FeRAMs, over ten years.

An explanation of a NDRO scheme with a motion of the polarization on a hysteresis curve is given in Fig. 11 for datum "0", on which a load line of the gate capacitor of the readout transistor is overlaid. At a readout operation [Fig. 11(a)], the reset transistor is turned off and a small readout voltage, V_{RD}, is applied to the top electrode so as to transfer polarization charges from the ferroelectric capacitor to the gate electrode of the readout transistor, causing a slight polarization switching. Then, the stored datum is

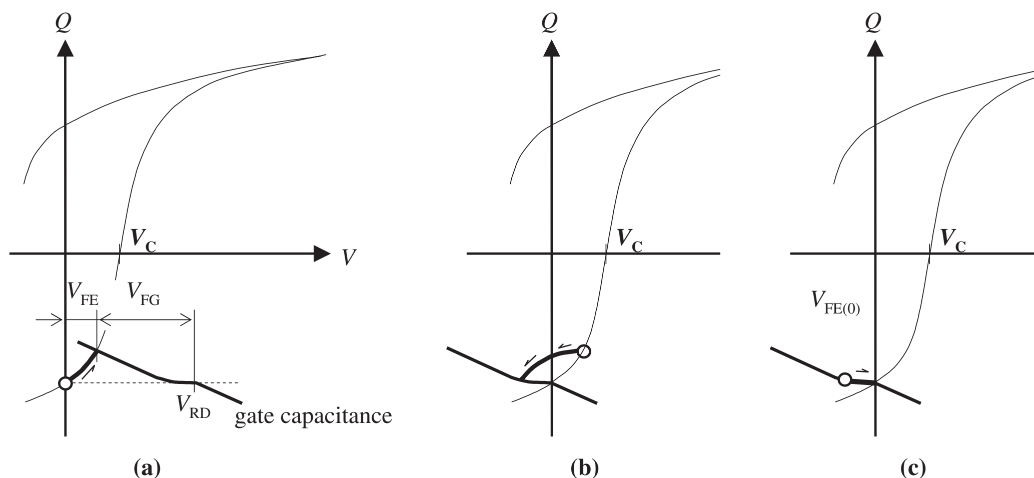

Fig. 11. Portion of Q–V hysteresis curve overlaid with gate capacitance at (a) readout operation, (b) V_{RD} removal and (c) reset operation.

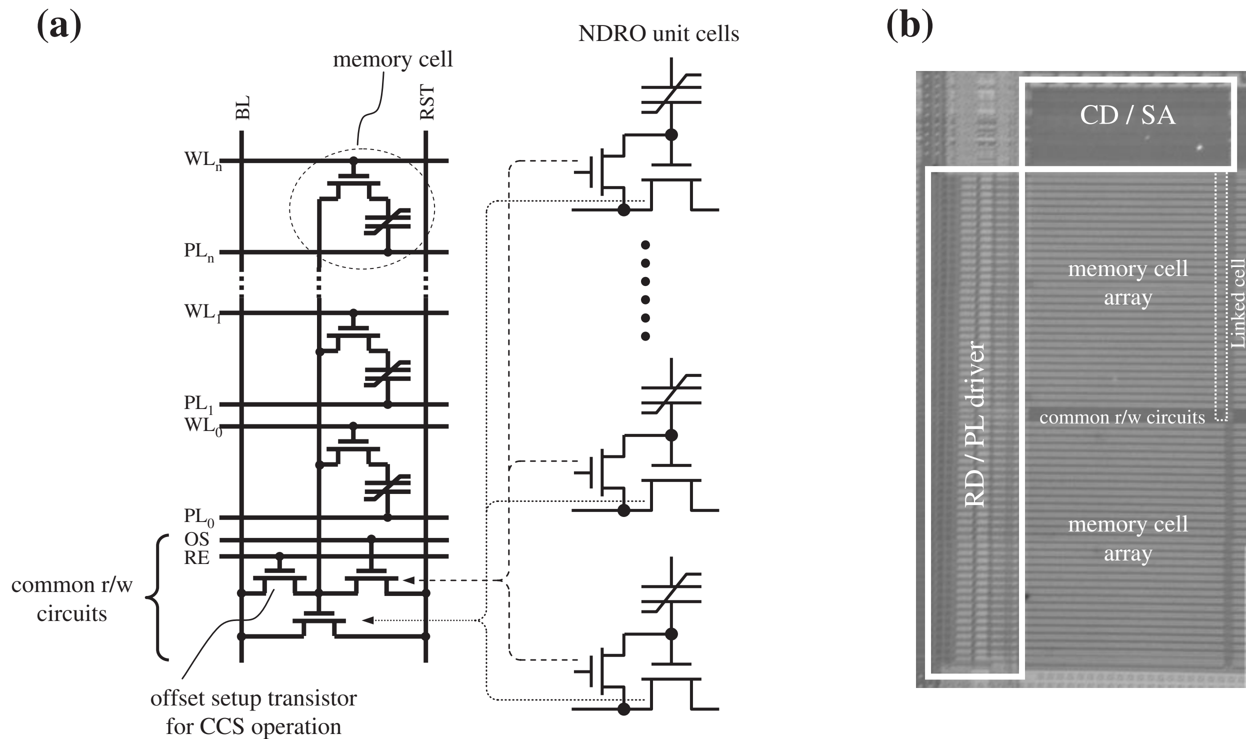

Fig. 12. (a) Link cell architecture and (b) a memory block of a NDRO FeRAM.

readout by drain–source current sensing. After reading, the top electrode is grounded, keeping the reset transistor off. In this operation, the polarization progresses toward a position with the same polarization value as the original value but a negative voltage [Fig. 11(b)]. This polarization motion is attributed to the bent shape of the load line (charges do not accumulate on the gate capacitor below a threshold voltage). Finally, the residual voltage is removed by turning the reset transistor on [Fig. 11(c)]. However, such a low-voltage operation reduces the amount of signal charges as a tradeoff against the increased read endurance.

To sense the small amount of charges, a memory cell consisting of two unit cells on which complementary data are programmed is used. Furthermore, to correct the process variations in threshold voltage of neighboring readout transistors, we have developed a charge-compensation-sensing (CCS) scheme, which is described elsewhere.[21)]

The unit cell using both NDRO and CCS techniques requires more elements than conventional FeRAMs. To reduce circuit elements, we have developed a linked cell architecture consisting of plural memory cells and a common read/write (r/w) circuit including a readout transistor, a reset transistor and an offset setup transistor for CCSs [Fig. 12(a)]. We have fabricated a 0.18 μm NDRO FeRAM with the link cell [Fig. 12(b)]. The NDRO FeRAM reveals that the NDRO scheme is efficient even after 10^{11} cycles of readout operation (Fig. 13). We expect that this stable readout will continue up to 10^{16} cycles.

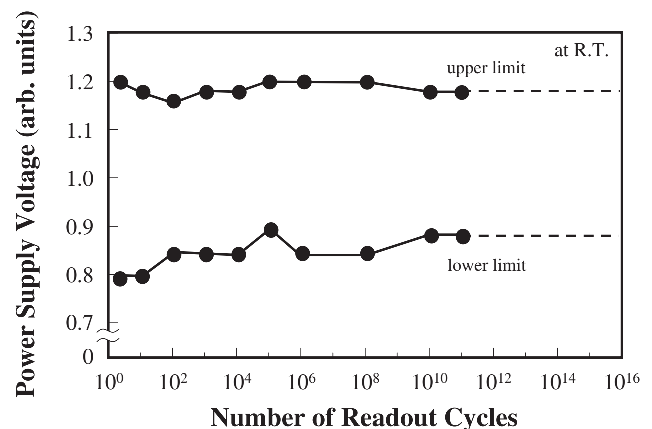

Fig. 13. Operational power supply voltage range as function of number of readout cycles.

5. Conclusions

Ferroelectric random access memory (FeRAM) technologies can provide SoCs with secure data storage, low-power consumption and a high design productivity. To incorporate the FeRAM technology into the leading-edge CMOS technology, we have developed a low-temperature formation technique for ferroelectrics. A bismuth titanate film deposited by metalorganic chemical vapor deposition and subsequently annealed at 500 °C reveals that perovskite grains preferentially orient along the (110) and (111) directions. A $Bi_4Ti_3O_{12}$ capacitor shows a remnant polarization ($2P_r$) of 25.7 μC/cm^2. In addition, to extend read cycle endurance, which is not sufficient for SoCs, we have developed a nondestructive readout operation (NDRO) technique, in which the switched polarization at reading is automatically rewritten by the removal of readout voltage. We have demonstrated stable readout operations even after 10^{11} cycles of a 0.18 μm NDRO FeRAM. The implementation of the FeRAM technology with the low-temperature formation and NDRO techniques is expected to be attractive for future SoCs.

1) C. A. Paz de Araujo, J. D. Cuchiaro, L. D. McMillan, M. C. Scott, and J. F. Scott: Nature **374** (1995) 627.
2) A. J. Menezes, P. C. van Oorschot, and S. A. Vanstone: *Handbook of Applied Cryptography* (CRC Press, Boca Raton, 1996) Chap. 1.
3) Y. Taur: IBM J. Res. Dev. **46** (2002) 213.
4) The International Technology Roadmap for Semiconductors (http://public.itrs.net/, 2005) Chap. Design.
5) O. Kömmerling and M. G. Kuhn: Proc. USENIX Workshop Smartcard Technology, 1999, p. 9.
6) Y. Nagano, T. Mikawa, T. Kutsunai, S. Natsume, T. Tatsunari, T. Ito, A. Noma, T. Nasu, S. Hayashi, H. Hirano, Y. Gohou, Y. Judai, and E. Fujii: IEEE Trans. Semicond. Manuf. **18** (2005) 49.
7) S. Koyama, Y. Kato, T. Yamada, and Y. Shimada: IEICE Trans. Electron. **E89-C** (2006) 1368.
8) T. Ninomiya, S. Masui, M. Oura, K. Mukaida, and T. Teramoto: Tech. Rep. IEICE SDM2002-268 (2003) p. 25 [in Japanese].
9) T. Miwa, J. Yamada, H. Koike, T. Nakura, T. Kobayashi, N. Kasai, and H. Toyoshima: Symp. VLSI Technology Dig. Tech. Pap., 2001, p. 129.
10) M. Motomura: presented at Microprocessor Forum, 2002.
11) S. Masui, T. Ninomiya, M. Oura, W. Yokozeki, K. Mukaida, and S. Kawashima: Symp. VLSI Technology Dig. Tech. Pap., 2001, p. 200.
12) Md. R. Anisur, T. Osipowicz, D. Z. Chi, and W. D. Wang: J. Electron. Mater. **34** (2005) 1110.
13) T. Osaka, A. Sakakibara, T. Seki, S. Ono, I. Koiwa, and A. Hashimoto: Jpn. J. Appl. Phys. **37** (1998) 597.
14) T. Kijima, M. Ushikubo, and H. Matsunaga: Jpn. J. Appl. Phys. **38** (1999) 127.
15) M. Yamada, N. Iizawa, T. Yamaguchi, W. Sakamoto, K. Kikuta, T. Yogo, T. Hayashi, and S. Hirano: Jpn. J. Appl. Phys. **42** (2003) 5222.
16) S. Kawashima and H. Nakano: IEEE J. Solid-State Circuits **37** (2002) 592.
17) C. L. Sun, S. Y. Chen, C. C. Liao, and A. Chin: Appl. Phys. Lett. **85** (2004) 4726.
18) S.-M. Yoon, E. Tokumitsu, and H. Ishiwara: Jpn. J. Appl. Phys. **39** (2000) 2119.
19) S. Sakai and R. Ilangovan: IEEE Electron Device Lett. **25** (2004) 369.
20) Y. Shimada, Y. Kato, T. Yamada, K. Tanaka, T. Otsuki, Z. Chen, M. Lim, V. Joshi, L. McMillan, and C. A. Paz de Araujo: Integrated Ferroelectr. **40** (2001) 41.
21) Y. Kato, T. Yamada, and Y. Shimada: IEEE Trans. Electron Devices **52** (2005) 2616.