A Novel Programmable Waveform Generator for Ultrasound Therapy Machine using FPGA

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Abstract: - The current ultrasound therapy machines are implementing continuous waveform, which in fact, is not an optimum technique for therapy treatment process. Apparently, pulse waveform appearing as a more effectively way of signal generation in terms of its power consumption, low cost hardware and short timing used. In order to overcome these drawbacks of conventional therapy machines, we proposed a programmable pulse generator for pulse waveform production with high frequency more than 1MHz through Cyclone 2 Field Programmable Gate Array (FPGA) development board. The generator is developed with maximum controllable 10 number of burst and clock frequency 50MHz. Register Transfer Level designs with Very-High-Speed Integrated Circuit Hardware Description Language (VHDL) coding are also implemented throughout this project. Pin assignment was used to assign the pin connection in FPGA for linkage of input and output data of FPGA. The result of generated waveforms were observed using oscilloscope. Based on the findings, the developed programmable FPGA is able to produce high frequency signal effectively and accurately.

Key-Words: - Ultrasound, field programmable gate array (FPGA), pulse generator, waveform, therapy

1 Introduction

The conventional waveform generator in ultrasound therapy machines are built with embedded hardware and due to that, problem of high maintenance cost for hardware might arise. Besides, treatment with pluses waveform at high frequency sound waves are also requires operator with special training, skills and experiences in order to operate the machine precisely. Fault operating of the machine might lead to overheating problem on the injured part of patient. In addition, the present waveform generator is not environmental friendly as the power consumption for this type of generator is essentially high. Consequently, it is contributed to greenhouse effect directly and waste of power resource might be another issue for long term upshot.

A pulse signal generator can either be an internal circuit or a piece of electronic test equipment used to generate pulses. Simple pulse generators usually allow control of the pulse repetition rate (frequency), pulse width, and delay with respect to an internal or external trigger and the high and low voltage levels of the pulses. More-sophisticated pulse generators may allow control over the rise time and fall time of the pulses. Besides, pulse generators may also applying digital techniques, analogue techniques, or a combination of both techniques to form the output pulses. For example, the pulse repetition rate and duration may be digitally controlled while the pulse amplitude, rise and fall of times may be determined by analogue circuitry in the output stage of a pulse generator. Within correct adjustment, pulse generators can produce a 50% duty cycle square wave. There are generally single-channel providing one frequency, delay, width and output. To produce multiple pulses, these simple pulse generators would have to be ganged in series or in parallel [1].

Based on the literatures, there were various types of methods in generating the particular waveform of pulse signal using Pulse Width Modulator (PWM).

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Sund S. Kim et al. have proposed a method using the combination of logic component such as register, comparator, counter, multiplexer, Flip-Flop and basic logic component. Their finding shows PWM is able to control the pulse width through the adjustments of duty cycle. Nevertheless, the drawbacks of their real time hardware implementation network controller with DSP and FPGA is only able to regulate the single width burst and produce continuous signal waveform [2]. Muthuramalingam et al. also reported their design using Universal Synchronous Receiver Transmitter (UART) to interface obtained data set based on Gaussian distribution. Read Access Memory (RAM) was used to store the received data from registers, counter and flip-flops. Then the produced pulse signals by FPGA are depends on the input signal control by the set of stored data. In other words, if there was no input data set to the FPGA, no pulse signal will be generated [3]. Besides, O. Cadenas et al. have presented method for pulse-width modulation based on DC-DC Converter for electric propulsion. The H bridge topography which consists of four IGBT transistors is driven by the module TL494 to function as switching. The filter circuit and operation amplifier are used to filter out the noise and amplify the output pulse signal [4].

In this paper, we present a computerized method to develop the pulse signal generator by using FPGA where the final resultant output are adjustable burst width and time delay between two pulse signal. The characteristic of the generated pulse signal waveform for burst width should be ranged within 1 second-1 until 10 second-1, and the maximum number of generated burst is up to 10 burst. The delay of burst and time should be changeable by the user accordingly.

The rest of this paper is organized as follows. In section 2, we describe the materials and method in details. The results of present method are shown in Section 3, and finally we draw some discussion and conclusion in Section 4 and 5 respectively.

2 Materials and Methods

The FPGA used in this project is Cyclone 2 FPGA Model EP2C20F484C7. Base on the characteristic of pulse signal, the burst width for one burst is range within 1 second-1 to 10 second-1. The time delay between two burst should be adjustable up to 40 ns at least and the maximum number of generated burst is 10 burst. Besides, among the High Description Language (HDL) coding, Very-High-Speed Integrated Circuit Hardware Description Language (VHDL) is chosen instead of Verilog coding. RTL design method is also required to plan the block diagram as the draft for codes writing. Last but not least, a Graphical User Interface (GUI) will be developed to allow user to key necessary data.

2.1 Quartus 2 Version 9.0

Quartus 2 is the software used to design the signal waveform which will be programmed in the Cyclone 2 FPGA for pulse signal production. The design of a system to integrate with FPGA consists four different steps, which including *algorithm of modelling, RTL modelling, RTL design and HDL coding*. The first stage of the design, *algorithm of modelling* is used to set the main function, and also determine the system stream by using finite state machine flow chart. Next, the *RTL modelling* is used to convert the algorithm of modelling into table form for type forecasting of logic components. These components will incorporate with the signal for output production at the next stage of design. For the *RTL design*, it is used to design the layout of the connection for combination of logic component. In addition, it is also used to set the output signal for each state to function the design system. Last but not least, the RTL design will be presented in VHDL coding form to program FPGA.

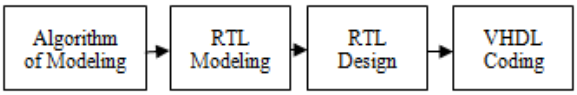

Fig. 1 The overall design system

2.1.1 Algorithm of Modelling

The goal of *algorithm of modelling* is to show the system flow for the output production, as shown in Figure 2. Firstly, the system will start with the initial state and its name to state 0 (S0). Next, it will be set to run the function “burst-1” and reach to state 1 (S1). The function of “burst-1” is to minus the number of burst that enters from the characteristic of signal in the developed Graphical User Interface (GUI). In order to continue move the program’s flow forward, it should passed through two different conditions, which are “in1=eq1” and “burst=0”. If “in1=eq1” and “burst=0” is in true mode, the system will set off to state 3 (S3). Else, it will be looped back to state S1. If “burst=0” is not in

true mode, then it will set off to state 2 (S2). In this state, if the "in2=eq2" is true mode, the program's flow it will go to state S1, otherwise it will be looped back to state S2 again. For the state S3, if "in3=eq3" is in true mode, the system will set off to "reset" function and return to initial state.

2.1.2 RTL Modelling

The system flow for the *RTL modelling* is the same as the previous stage. It is simply presented in the table form for continuing to set the control vector signal, which used to function the data path unit. Based on the table 1, we were able to forecast the logic components which will be used in the design later on. Such logic components are included counter and comparator. The counter is used to count the number for each clock cycle while the comparator can compare the input data value with the count value from the counter. If the input data value is equal to the count value, it will simulate positive response logic "1" to the control unit for triggering next state.

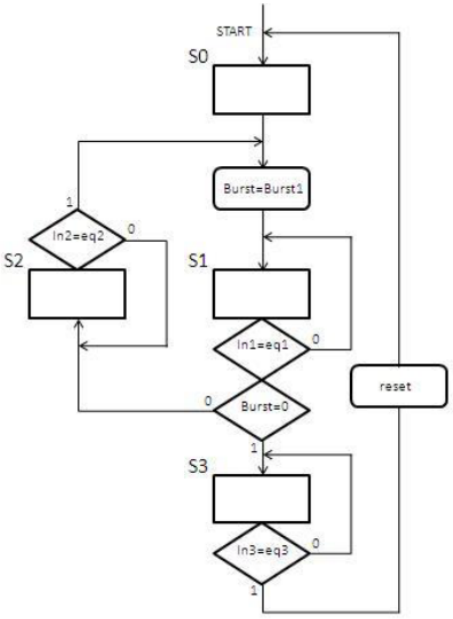

Fig. 2 The algorithm of modelling

Table 1 The RTL modelling of the present state and next state

S0	BURST<-BURST-1
	GOTO S1
S1: (IN1=EQ1)	GOTO S3
(BURST=0)	GOTO S1
(IN1=EQ1)*	GOTO S2
(BURST=0)*	
S2: (IN2=EQ2)	BURST<-BURST-1
(IN2=EQ2)*	GOTO S1
	GOTO S2
S3: (EQ3)	RESET
(IN3=EQ3)*	GOTO S0
	GOTO S3

2.1.3 RTL Design

A clock signal (*clk*) is synchronous supply to control unit and data path unit. The reset signal (*reset*) is used to disable the pulse signal generator to produce pulse when the reset signal is "1". The "burst" is the number of burst that the user wishes to generate and entered through the GUI. The signals "in1", "in2", and "in3" are the input data for the characteristic of signal which will be entered based on GUI.

The waveform is the output of the system which will be generated according to the user's setting. For

control unit, the signals are linked to other units such as clock signal, reset signal and feedback signal. The output of the control unit is called control vector signal. The feedback signal from the data path unit will triggered the control unit to perform next step in the system. The control vector or bus control (*rst, en1, en2, en3*) will manage the reset signal for counter switching. The first counter is used to count the burst width. The second counter is used to count the burst delay while third counter is use to count the time delay between two set of burst. Details of the description are illustrated in Figure 3.

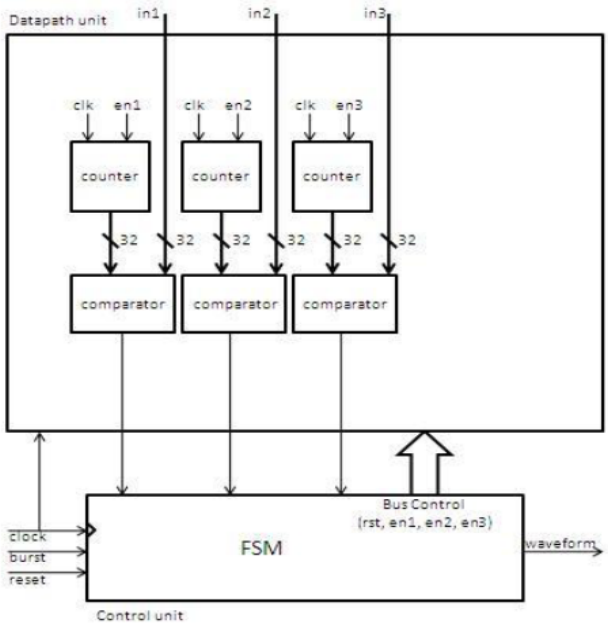

Fig. 3 The designed block diagram according to *algorithm of modelling*

Table 2 The signal that set in the control unit according to the feedback signal

RTN		SIGNAL ACTIVATE	[rst en1 en2 en3]
S0	BURST<-BURST-1	rst	1000
	GOTO S1		
S1: (IN1=EQ1)	GOTO S3	en1	0100
(BURST=0)	GOTO S1	en1	0100
(IN1=EQ1)*	GOTO S2	en1	0100
(BURST=0)*			
S2: (IN2=EQ2)	BURST<-BURST-1		
(IN2=EQ2)*	GOTO S1	en2	0010
	GOTO S2	en2	0010
S3: (IN3=EQ3)	RESET		
(IN3=EQ3)*	GOTO S0	en3	0001
	GOTO S3	en3	0001

When the system begin from the initial state (S0), the reset signal will set the entire counter to initial count value = 0. At state 1, whenever the feedback signal passed from the first comparator (*in1=eq1*) is "1", the system will set off to state 3. If the first comparator is "0", then the counter will keep on counting. If the number of burst is greater than two, the system will go to state 2 to initiate the second counter by giving signal enable 2 (*en2*). The state 3 will give signal enable 3 (*en3*) equal to "1" in order to initiate the third counter.

2.2 VHDL Coding Program using Quartus 2

By using the default timing analysis, the output shown in the vector waveform file is almost the same as the result obtained by using the

oscilloscope. Figure 4 illustrate the produced output waveform by the VHDL coding. It shows that the developed coding is generating the desired pulse signal waveform accurately.

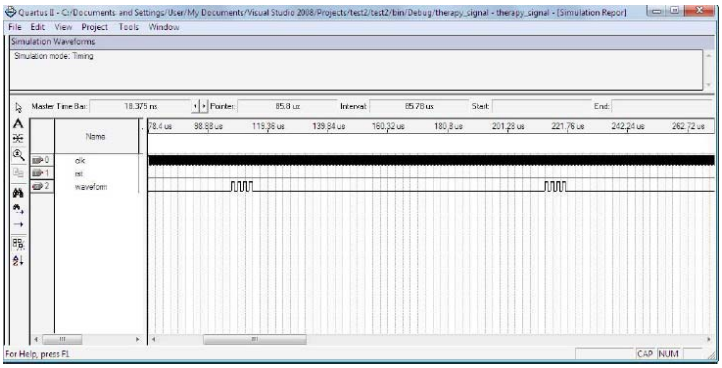

Fig. 4 Output signal generate by the VHDL coding

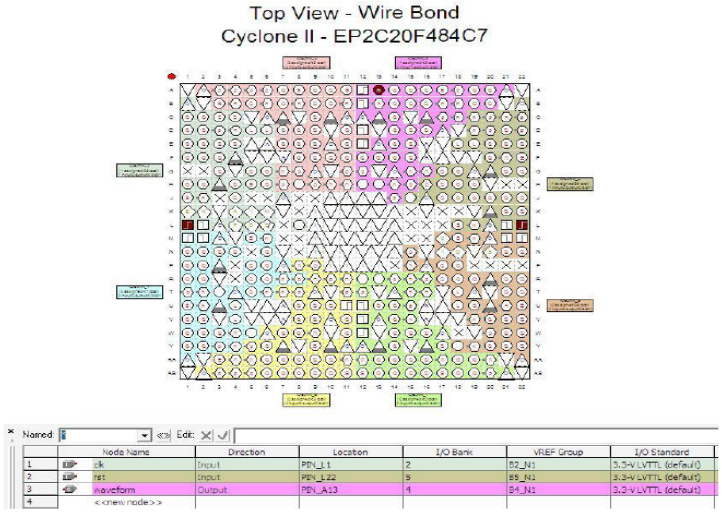

Fig. 5 Creating of pin assignment for the Cyclone 2 FPGA

Figure 5 shows the pin assignment of the Cyclone 2 FPGA model EP2C20F484C7. There are only 3 pin used in the present work to connect from the Cyclone 2 processor to the pin of input and output. The input pin such as PIN_L1 is an input of internal clock of frequency 50 MHz while the PIN_L22 is a switch button to reset or stop the system. The PIN_A13 act as output pin which is one of the PIO connector that will connect to the oscilloscope to view the output signal waveform.

3 Results

The method used to observe the produced pulse waveform can be done by measuring the burst width through the oscilloscope. The results of actual burst width measurement by using oscilloscope were recorded as shown in Table 3 and Table 4 accordingly.

Table 3 Actual burst width observe by using oscilloscope

Burst Width (s-1)	Voltage (v)	Burst width (ns)
1	3.48	1000±1
2	3.48	500±1
3	3.48	340±1
4	3.48	260±1

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5	3.48	200±1
6	3.48	160±1
7	3.48	140±1
8	3.48	120±1
9	3.48	111±1
10	3.48	100±1

Table 4 Total burst width that measure according to the number of burst

No. of Burst	Burst Width (ns)	Voltage (v)	Total Burst Width (ns)
1	1000	3.48	1000
2	1000	3.48	3000
3	1000	3.48	5000
4	1000	3.48	7000
5	1000	3.48	9000
6	1000	3.48	11000
7	1000	3.48	13000
8	1000	3.48	15000
9	1000	3.48	17000
10	1000	3.48	19000

As shown in Fig. 6, the number of pulse set in the graph is up to 10 burst. While the burst delay is 1000 ns, the burst width is 1000 ns. Also, the obtained finding shows the linear increments of number of burst are proportional to the total burst width. This indicates that the increasing number of burst is adding up the burst width for the pulse waveform linearly.

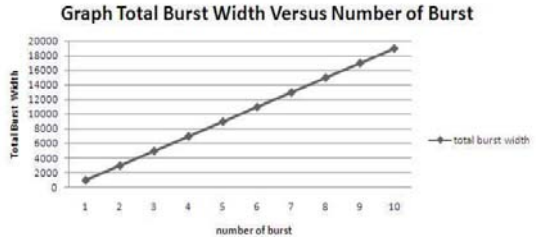

Fig. 6 Total burst width versus number of burst

4 Conclusion

As a conclusion, the pulse waveform generator using Cyclone 2 FPGA have been developed. The novelty of the developed program is the produced waveform signal can be adjusted or set by the user according to their needs through Graphical User Interface. Cyclone 2 FPGA is the most low cost and friendly user by the designer to develop the pulse waveform generator. The combination of logic component and represented by using VHDL coding is most efficient way to produce the adjustable pulse signal. Besides, Cyclone 2 FPGA can produce more high quality pulse signal with less affected noise that cause by the internal electronic component. Furthermore, the Cyclone two FPGA can be reprogrammable and used for other type of system design. Findings show that the developed system is able to provide consistent and more objective results.

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