Instruction Execution Times

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Introduction

This appendix contains several tables that provide the instruction execution times for DL105 Micro PLCs. Many of the execution times depend on the type of data used with the instruction. Registers may be classified into the following types:

- Data (word) Registers
- Bit Registers

V-Memory Data Registers

Some V-memory locations are considered data registers, such as timer or counter current values. Standard user V-memory is classified as a V-memory data register. Note that you can load a bit pattern into these types of registers, even though their primary use is for data registers. The following locations are data registers:

Data Registers	DL105
Timer Current Values	V0–V77
Counter Current Values	V1000–V1077
User Data Words	V2000–V2377 V4000–V4177

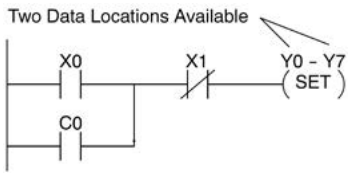
V-Memory Bit Registers

You may recall that some of the discrete points such as X, Y, C, etc. are automatically mapped into V-memory (see Appendix E). The following bit registers contain this data:

Data Registers	DL105
Input Points (X)	V40400–V40407
Output Points (Y)	V40500–V40507
Control Relays (C)	V40600–V40617
Timer Status Bits	V41100–V41103
Counter Status Bits	V41140–V41143
Stages	V41000–V41017

How to Read the Tables

Some instructions can have more than one parameter. For example, the SET instruction shown in the ladder program to the right can set a single point or a range of points.



In cases like these, execution times depend on the quantity and type of parameters. The execution time tables list execution times for both situations, as shown below:

SET	1st # → X, Y, C, S 2nd # → X, Y, C, S → (N pt)	17.4 µs 12.0 µs + 5.2 µs x N
RST	1st # → X, Y, C, S 2nd # → X, Y, C, S → (N pt)	19.5 µs 10.5 µs + 5.2 µs x N

Execution depends on the number of locations and types of data used

Instruction Execution Times

Boolean Instructions

Boolean Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Non Execute**
STR	X, Y, C, T, CT, S, SP	3.3 µs	3.3 µs
STRN	X, Y, C, T, CT, S, SP	3.9 µs	3.9 µs
OR	X, Y, C, T, CT, S, SP	2.7 µs	2.7 µs
ORN	X, Y, C, T, CT, S, SP	3.3 µs	3.3 µs
AND	X, Y, C, T, CT, S, SP	2.1 µs	2.1 µs
ANDN	X, Y, C, T, CT, S, SP	2.7 µs	2.7 µs
ANDSTR	None	1.2 µs	1.2 µs
ORSTR	None	1.2 µs	1.2 µs
OUT	X, Y, C	3.4 µs	3.4 µs
OROUT	X, Y, C	8.6 µs	8.6 µs
PD	X, Y, C	13.5 µs	13.5 µs
SET	1st # → X, Y, C, S 2nd # → X, Y, C, S → (N pt)	17.4 µs 12.0 µs + 5.4 µs x N	6.8 µs 6.8 µs
RST	1st # → T, CT 2nd # → T, CT → (N pt)	31.6 µs 17.0 µs + 14.6 µs x N	6.8 µs 6.8 µs
PAUSE	1wd # → Y 2wd # → Y → (N pt)	19.0 µs 15µs + 4µs x N	19.0 µs 15µs + 4µs x N
RST	1st # → X, Y, C, S 2nd # → X, Y, C, S → (N pt)	17.7 µs 10.5 µs + 5.2 µs x N	6.8 µs 6.8 µs

Comparative Boolean Instructions, Continued

Comparative Boolean Instructions				DL105	
Instruction	Legal Data Types			Execute	Non Execute
STRE	1st	→	2nd		
	V: Data Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	77µs 158µs 57µs	13.8 µs 13.8 µs 13.8 µs
	V: Bit Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	158µs 240µs 139µs	13.8 µs 13.8 µs 13.8 µs
STRNE	1st	→	2nd		
	V: Data Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	77µs 158µs 57µs	13.8 µs 13.8 µs 13.8 µs
	V: Bit Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	158µs 240µs 139µs	13.8 µs 13.8 µs 13.8 µs
ORE	1st	→	2nd		
	V: Data Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	75µs 158µs 55µs	12.0 µs 12.0 µs 12.0 µs
	V: Bit Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	158µs 239µs 137µs	12.0 µs 12.0 µs 12.0 µs
ORNE	1st	→	2nd		
	V: Data Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	75µs 158µs 55µs	12.0 µs 12.0 µs 12.0 µs
	V: Bit Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	158µs 239µs 137µs	12.0 µs 12.0 µs 12.0 µs
ANDE	1st	→	2nd		
	V: Data Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	75µs 158µs 55µs	12.0 µs 12.0 µs 12.0 µs
	V: Bit Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	158µs 239µs 137µs	12.0 µs 12.0 µs 12.0 µs
ANDNE	1st	→	2nd		
	V: Data Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	75µs 158µs 55µs	12.0 µs 12.0 µs 12.0 µs
	V: Bit Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	158µs 239µs 137µs	12.0 µs 12.0 µs 12.0 µs

Comparative Boolean Instructions, Continued

Comparative Boolean Instructions				DL105	
Instruction	Legal Data Types			Execute	Non Execute
STR	1st	→	2nd		
	T, CT.	→	V: Data Reg. V: Bit Reg. K: Constant	78µs 158µs 57µs	13.8 µs 13.8 µs 13.8 µs
	1st	→	2nd		
	V: Data Reg	→	V: Data Reg. V: Bit Reg. K: Constant	78µs 159µs 57µs	13.8 µs 13.8 µs 13.8 µs
	V: Bit Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	159µs 241µs 139µs	13.8 µs 13.8 µs 13.8 µs
STRN	1st	→	2nd		
	T, CT.	→	V: Data Reg. V: Bit Reg. K: Constant	78µs 158µs 57µs	13.8 µs 13.8 µs 13.8 µs
	1st	→	2nd		
	V: Data Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	78µs 159µs 57µs	13.8 µs 13.8 µs 13.8 µs
	V: Bit Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	159µs 241µs 139µs	13.8 µs 13.8 µs 13.8 µs
OR	1st	→	2nd		
	T, CT.	→	V: Data Reg. V: Bit Reg. K: Constant	75µs 158µs 55µs	12.0 µs 12.0 µs 12.0 µs
	1st	→	2nd		
	V: Data Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	75µs 158µs 55µs	12.0 µs 12.0 µs 12.0 µs
	V: Bit Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	158µs 240µs 137µs	12.0 µs 12.0 µs 12.0 µs
ORN	1st	→	2nd		
	T, CT.	→	V: Data Reg. V: Bit Reg. K: Constant	75µs 158µs 55µs	12.0 µs 12.0 µs 12.0 µs
	1st	→	2nd		
	V: Data Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	75µs 158µs 55µs	12.0 µs 12.0 µs 12.0 µs
	V: Bit Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	158µs 240µs 137µs	12.0 µs 12.0 µs 12.0 µs

Comparative Boolean Instructions, Continued

Comparative Boolean Instructions				DL105	
Instruction	Legal Data Types			Execute	Non Execute
AND	1st	→	2nd		
	T, CT.	→	V: Data Reg. V: Bit Reg. K: Constant	76µs 158µs 55µs	12.0 µs 12.0 µs 12.0 µs
	1st	→	2nd		
	V: Data Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	75µs 158µs 55µs	12.0 µs 12.0 µs 12.0 µs
	V: Bit Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	158µs 240µs 137µs	12.0 µs 12.0 µs 12.0 µs
ANDN	1st	→	2nd		
	T, CT.	→	V: Data Reg. V: Bit Reg. K: Constant	76µs 158µs 55µs	12.0 µs 12.0 µs 12.0 µs
	1st	→	2nd		
	V: Data Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	76µs 158µs 55µs	12.0 µs 12.0 µs 12.0 µs
	V: Bit Reg.	→	V: Data Reg. V: Bit Reg. K: Constant	158µs 240µs 137µs	12.0 µs 12.0 µs 12.0 µs

Immediate Instructions

Immdiate Instructions		DL105	
Instruction	Legal Data Types	Execute	Non Execute
STRI	X	27µs	9.8 µs
STRNI	X	26µs	8.6 µs
ORI	X	27µs	9.8 µs
ORNI	X	26µs	8.6 µs
ANDI	X	25µs	8.0 µs
ANDNI	X	24µs	6.8 µs
OROUTI	Y	45µs	45µs
SETI	1st # → Y 2nd # → Y → (N pt)	25.5 µs 5.5 µs + 20 x N	6.8 µs 6.8 µs
RSTI	1st # → Y 2nd # → Y → (N pt)	25.5 µs 5µs + 20.5 x N	6.8 µs 6.8 µs

Timer, Counter, Shift Register, EDRUM Instructions

Timer, Counter, Shift Register and Drum Instructions				DL105	
Instruction	**Legal Data Types**			**Execute**	**Non Execute**
TMR	1st	→	2nd		
	T	→	V: Data Reg. V: Bit Reg. K: Constant	75µs 158µs 66µs	31µs 31µs 31µs
TMRF	1st	→	2nd		
	T	→	V: Data Reg. V: Bit Reg. K: Constant	75µs 158µs 66µs	31µs 31µs 31µs
TMRA	1st	→	2nd		
	T	→	V: Data Reg. V: Bit Reg. K: Constant	94µs 304µs 95µs	56µs 264µs 45µs
TMRAF	1st	→	2nd		
	T	→	V: Data Reg. V: Bit Reg. K: Constant	98µs 304µs 95µs	54µs 264µs 49µs
CNT	1st	→	2nd		
	CT	→	V: Data Reg. V: Bit Reg. K: Constant	68µs 148µs 56µs	61µs 141µs 45µs
SGCNT	1st	→	2nd		
	CT	→	V: Data Reg. V: Bit Reg. K: Constant	57µs 140µs 46µs	64µs 148µs 53µs
UDC	1st	→	2nd		
	CT	→	V: Data Reg. V: Bit Reg. K: Constant	103µs 310µs 102µs	74µs 281µs 70µs
SR	C	→	(N points to shift)	30µs + 4.6 µs x N	17.2 µs
EDRUM	CT			320µs	221µs

Accumulator Data Instructions

Accumulator / Stack Load and Output Data Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Non Execute**
LD	V: Data Reg. V: Bit Reg. K: Constant	75µs 158µs 66µs	31µs 31µs 31µs
LDD	V: Data Reg. V: Bit Reg. K: Constant	75µs 158µs 66µs	31µs 31µs 31µs
LDF	1st → 2nd		
	X, Y, C, S → K: Constant T, CT, SP → (N pt)	30µs + 4.6 µs x N	10µs
LDA	O (Octal constant for address)	58µs	8.4 µs
OUT	V: Data Reg. V: Bit Reg. P: Indir (Data) P: Indir (Bit)	60µs 132µs 162µs 239µs	8.4 µs 8.4 µs 8.4 µs 8.4 µs
OUTD	V: Data Reg. V: Bit Reg. P: Indir (Data) P: Indir (Bit)	68µs 276µs 196µs 384µs	8.4 µs 8.4 µs 8.4 µs 8.4 µs
OUTF	1st → 2nd		
	X, Y, C, → K: Constant (N pt)	36µs + 7.6 µs x N	8µs
POP	None	55µs	17.2 µs

Logical Instructions

Logical (Accumulator) Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Non Execute**
AND	V: Data Reg. V: Bit Reg.	63µs 261µs	10.4 µs 10.4 µs
ANDD	K: Constant	53µs	8.4 µs
OR	V: Data Reg. V: Bit Reg.	59µs 257µs	10.4 µs 10.4 µs
ORD	K: Constant	49µs	8.4 µs
XOR	V: Data Reg. V: Bit Reg.	60µs 257µs	10.4 µs 10.4 µs
XORD	K: Constant	49µs	8.4 µs
CMP	V: Data Reg. V: Bit Reg.	59µs 259µs	10.4 µs 10.4 µs
CMPD	V: Data Reg. V: Bit Reg. K: Constant	63µs 257µs 54µs	8.4 µs 8.4 µs 8.4 µs

Math Instructions

Math Instructions (Accumulator)		DL105	
Instruction	**Legal Data Types**	**Execute**	**Non Execute**
ADD	V: Data Reg. V: Bit Reg.	198µs 397µs	10.6 µs 10.6 µs
ADDD	V: Data Reg. V: Bit Reg. K: Constant	198µs 397µs 188µs	8.4 µs 8.4 µs 8.4 µs
SUB	V: Data Reg. V: Bit Reg.	200µs 397µs	10.6 µs 10.6 µs
SUBD	V: Data Reg. V: Bit Reg. K: Constant	198µs 392µs 190µs	8.4 µs 8.4 µs 8.4 µs
MUL	V: Data Reg. V: Bit Reg. K: Constant	497µs 483µs 487µs	10.6 µs 10.6 µs 8.4 µs
DIV	V: Data Reg. V: Bit Reg. K: Constant	909µs 1108µs 899µs	10.6 µs 10.6 µs 8.4 µs
INCB	V: Data Reg. V: Bit Reg.	83µs 349µs	10.4 µs 10.4 µs
DECB	V: Data Reg. V: Bit Reg	82µs 351µs	10.4 µs 10.4 µs

Bit Instructions

Bit Instructions (Accumulator)		DL105	
Instruction	**Legal Data Types**	**Execute**	**Non Execute**
SHFR	V: Data Reg. (N bits) V: Bit Reg. (N bits) K: Constant (N bits)	44µs + 14.6 x N 243µs + 14.6 x N 34µs + 14.6 x N	10.4 µs 10.4 µs 8.4 µs
SHFL	V: Data Reg. (N bits) V: Bit Reg. (N bits) K: Constant (N bits)	44µs + 14.6 x N 243µs + 14.6 x N 34µs + 14.6 x N	10.4 µs 10.4 µs 8.4 µs
ENCO	None	62µs	7.2 µs
DECO	None	34µs	7.2 µs

Number Conversion Instructions

Number Conversion Instructions (Accumulator)		DL105	
Instruction	**Legal Data Types**	**Execute**	**Non Execute**
BIN	None	359µs	7.2 µs
BCD	None	403µs	7.2 µs
INV	None	27µs	5.0 µs

Table Instructions

Table Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Non Execute**
MOV	Move V: Data Reg. to V: Data Reg. Move V: Bit Reg. to V: Data Reg. Move V: Data Reg. to V: Bit Reg. Move V: Bit Reg. to V: Bit Reg. N= # of Words	450µs + 17 x N 430µs + 244 x N 460µs + 215 x N 490µs + 448 x N	6.2 µs 6.2 µs 6.2 µs 6.2 µs
MOVMC	Move V: Data Reg. to E^2. Move V: Bit Reg. to E^2 Move E^2 to V: Bit Reg. Move E^2 to V: Bit Reg. N= # of Words	— — 250µs + 201 x N —	— — 6.2 µs —
LDLBL	K	58µs	8.4 µs

CPU Control Instructions

CPU Control Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Non Execute**
NOP	None	0µs	0µs
END	None	27µs	27µs
STOP	None	16µs	5µs

Program Control Instructions

Program Control Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Non Execute**
MLS	K (1–7)	12µs	12µs
MLR	K (0–6) N= 1 to 7	13µs + 2.4 x N	13µs + 2.4 x N

Interrupt Instructions

Interrupt Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Non Execute**
ENI	None	9µs	5µs
DISI	None	8µs	5µs
INT	O0	0µs	0µs
IRT	None	1.6 µs	—

Message Instructions

Message Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Non Execute**
FAULT	V: Data Reg. (N bits) V: Bit Reg. (N bits) K: Constant (N bits)	171µs 253µs 2798µs	8.4 µs 8.4 µs 8.4 µs
DLBL	K	0µs	0µs
NCON	K	0µs	0µs
ACON	K	0µs	0µs

RLL*PLUS* Instructions

RLL*PLUS* Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Non Execute**
ISG	S	31µs	32µs
SG	S	31µs	32µs
JMP	S	14µs	8µs