
Silicon Nanowire FinFETs

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1. Introduction

Some of the fundamental problems of ultra-small MOSFETs beyond sub-10nm channel length are the electrostatic limits, source-to-drain tunnelling, carrier mobility degradation, process variations, and static leakage. The trend toward ultra-short gate length MOSFETs requires a more and more effective control of the channel by the gate leading to new device architecture. It appears that non-classical device architectures can extend the CMOS lifetime and provide solutions to continue scaling. In case of silicon-based CMOS technologies, planar MOSFETs are limited to scaling beyond 15 nm technology node. As simple scaling of silicon CMOS becomes increasingly complex and expensive, there is considerable interest in increasing performance by using strained channels which can improve carrier mobility and drive current in a device. Multi-gate MOSFETs based on the concept of volume inversion are widely recognized as one of the most promising solutions for meeting the ITRS roadmap requirements. A wide variety of multi-gate architectures, including Double-Gate (DG), Gate-All-Around (GAA), Pi-FET and Fin Field-Effect Transistors (FinFETs), rectangular or cylindrical nanowire MOSFETs has been proposed in the literature. In all cases, these structures exhibit a superior control of short channel effects resulting from an exceptional electrostatic coupling between the conduction channel and the surrounding gate electrode. The nanowire (NW) transistors can be seen as the ultimate integration of the innovative nanodevices and is one of the candidates which have gained significant attention from both the device and circuit developers because of its potential for building highly dense and high performance electronic circuits. Recent advances in nanoscale fabrication techniques have shown that semiconductor nanowires may become the candidate for next generation technologies. Si and Ge nanowire transistors are also important because of their compatibility with the CMOS technology.

Nanowires and FinFETs have attracted considerable attention due to their proven robustness against Short-Channel Effects (SCE) and relatively simple fabrication. Silicon nanowire

FinFET (SNWFT) is being considered as the candidate for CMOS scaling beyond the 32 nm node due to its high performance, excellent gate control and enhanced carrier transportation properties. Thin and multi-gate controlled body provide FinFETs a superior short-channel effect control, electrostatic shielding from the body bias, relaxing channel doping or pocket implants, commonly needed in planar technologies to avoid threshold voltage (V_{TH}) roll-off [1]. Adequate device V_{TH} is now being achieved by using gate stack engineering. Metal-Gates with High-k (HKMG) dielectric stacks provide the desired V_{TH} by work-function tuning as well as preserving low gate leakage [2]. Various process options are being attempted to affect carrier transport in a different manner. The use of metal gates as replacement for Poly-Si stacks eliminates the Poly-depletion effect, benefiting effective carrier mobility by reducing the transverse field [1]. Additionally, use of undoped channels improves low-field μ_{eff} due to the reduction in the substrate impurity scattering [3]. Mobility degradation due to Coulomb scattering in short-channel devices should further be reduced in the absence of pocket implants [4]. However, high-k dielectrics are known to degrade mobility as a result of a combination of Coulomb and phonon scattering mechanisms [5]. In order to account for inversion layer mobility degradation mechanisms for FinFET devices, a robust μ_{eff} extraction algorithm is necessary. The mobility extraction requires accurate measurement of both gate to channel capacitance and channel current, together with reliable estimations for the parasitic Source-Drain series resistance (R_{SD}) and the effective channel length [4]. Unfortunately, the capacitance of short-channel length devices in the presence of large gate leakage is no longer characterized trivially. In multi-gate architectures like the FinFET, the carrier transport occurs in different crystallographic planes. For standard substrates, the current flow occurs in the (100)/(110) for the top surface and (110)/(110) for the sidewalls. The transport in these crystal planes and directions are characterized by different mobility primarily due to the anisotropy of the effective masses.

The most promising among various Si multi-gate MOSFET architectures such as double-gate and tri-gate FinFETs, are nanowire FinFETs due to their superior electrostatic control through gate-all-around structure. Superior gate control, immunity of threshold voltage from substrate bias and excellent carrier transport properties along with more aggressive channel length scaling possibility have made GAA architecture with semiconductor nanowire channel a potential candidate for post-planar transistor design. Two approaches are generally used to fabricate Si NWs as well as other semiconductor NWs: bottom-up and top-down. In the first method, NWs are usually grown using a metallic catalyst on a separate substrate, usually through a Vapor-Liquid-Solid (VLS) growth mechanism. After a chemical or mechanical separation step, the NWs are harvested and transferred to another substrate [6]. In the top down-approach, the NWs are fabricated using a CMOS compatible technology, such as lithography-based patterning and etching [7]. Unlike the bottom-up approach where the NWs are randomly distributed, the top-down method enables accurate positioning of the NWs across the wafer and facilitates the ultra-large-scale-integration (ULSI) for high performance nano-electronic circuits. Moreover, due to processing difficulties related to the length of grown NWs, NW release and gate-etch process, most of the VLS grown NW transistors have omega-shaped gate (Ω -gate) geometry and are thus not full gate-all-around

[6]. Among all the promising post-CMOS non-conventional structures, the silicon nanowire transistor has the most unique advantage – it is based on silicon.

In a MOSFET, the carriers encounter various scattering mechanisms on their way towards the drain terminal. Carrier mobility is a well known benchmark to judge the intrinsic performance of a long channel MOSFET. The state-of-the art short channel devices do not operate in the fully ballistic regime (they are at roughly 60% of the ballistic limit) and mobility is related to velocity through effective mass and ballistic ratio. Therefore, understanding the carrier mobility is beneficial to design and engineer new devices for future CMOS generations. The presence of significant resistive and capacitive parasitics as well as lack of large capacitance due to the small size of the NW channel adds complexities to the extraction of the intrinsic NW device characteristics. Simplified assumptions or incomplete device charge simulations generally lead to inaccurate and unreasonable mobility extraction [9]. In the absence of a well-behaved top-down process (as compared to the bottom-up-fabricated NWs with smooth and near ideal sidewalls) results in significant mobility degradation for smaller NW sizes [8].

Noise is known as a fundamental problem in various fields such as telecommunication, nanoelectronics, and biological systems. The low-frequency noise, or $1/f$ noise, is the excess noise at low frequencies whose power spectral density (PSD) approximately depends inversely on the frequency and therefore escalates at low frequencies. The $1/f$ noise originating from the transistors is a major issue in analog circuit design. The $1/f$ noise is, for example, up converted to undesired phase noise in voltage controlled oscillator (VCO) circuits, which can limit the information capacity of communication systems.

In this chapter we shall present a detailed framework on gate-all-around nanowires and multi-gate FinFETs which will include process and device design and characterization, simulation, and low-frequency noise and tunnelling spectroscopy analyses. Carrier mobility extraction in nanowire and FinFETs using split-CV technique will be described. Channel orientation dependence of the electrical parameters such as current, low-frequency noise will be presented. Self-heating effects in nanowire transistors are also discussed. In Section 2, the growth and fabrication of silicon nanowire transistors and multi-gate FinFET devices will be covered. The detailed fabrication process steps for GAA nanowires as well as tri-gate FinFETs are discussed. 3D device simulation and electrical characterization will also be covered in this Section. Split CV measurement technique is employed for mobility calculation and detailed model equations are formulated for FinFET and nanowire structures. In Section 3, the low-frequency noise characteristics of the nanowire FinFETs will be taken up. Voltage dependence of flicker noise ($1/f$) and power spectral densities and corner frequencies will be discussed based on low-frequency noise measurements. Time-domain random telegraph signal (RTS) and existence of two-level or multi-level RTS noise in nanowire transistors will also be taken up. In section 4, the orientation dependence will be discussed and current-voltage characteristics are compared to show the effect of orientation on the drain current. The effect of channel orientation is also discussed for the nanowire FinFET noise spectral densities for (100) and (110) channel orientations. In section 5, the lattice structures of Si, SiO₂ in the nanowire FinFET are analyzed via inelastic electron tunneling spectroscopy (IETS). The

lattice dynamics and other molecular vibrations in silicon nanowire FinFETs are discussed using the IETS spectra.

2. Multi-gate FinFET and Nanowire Transistors

In order to control short channel effects in planar SOI MOSFETs and maintain reasonable electrostatics at a given gate length, L_G , a critical Si thickness, t_{Si} on the order of $L_G/3$ is required [10]. Multi-gate devices have been suggested to significantly relax the critical Si dimension in fully depleted SOI (FD-SOI) device architectures and process technology. For this purpose, planar double-gate, vertical double-gate (FinFET), triple-gate (Tri-gate), omega-shaped gate (Ω -gate), penta-gate, inverted T-channel FET, Φ -FET, and GAA nanowires have been proposed by various research groups over the past decade.

While most of these multi-gate technologies have been experimentally shown to benefit from excellent electrostatics and short-channel effects, they commonly suffer from a complicated fabrication process technology compared to planar bulk or SOI technology. Figure 1. shows the device schematic of

- a. double-gate FinFET
- b. tri-gate and
- c. GAA NW MOSFETs.

The critical Si dimensions to sustain acceptable electrostatics have been reported [11]. It can be seen that the criterion of Si film thickness may be relaxed for the nanowire MOSFET, which is naturally evolved from double-gate FinFET technology.

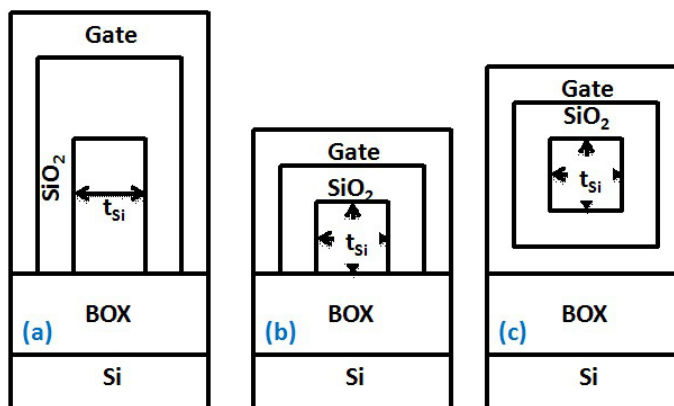


Figure 1. Schematics of device structures of (a) double-gate FinFET (b) tri-gate and (c) GAA NW MOSFETs.

2.1. 3D Quantum Simulation of Multi-Gate FinFETs

The simulation of tri-gate FinFET is performed using SILVACO ATLAS3D quantum simulator framework. The Bohm Quantum Potential (BQP) model is included to model the confinement effects in the simulation. Also, calibration of the BQP model against the 2D Schrödinger-Poisson simulation is done for describing the quantum effects in small geometry Si FinFET and nanowire transistors. To model the effects of quantum confinement, ATLAS allows the solution of Schrödinger's equation along with the fundamental device equations. The solution of Schrödinger's equation gives a quantized description of the density of states in the presence of quantum-mechanical confining potential variations. When the quantum confinement is in one dimension (along y-axis), the calculation of the quantum electron density relies upon a solution of a 1D Schrödinger equation solved for eigen-state energies $E_{iv}(x)$ and wave-functions $\Psi_{iv}(x, y)$ at each slice perpendicular to x-axis and for each electron valley (or hole band) v as described below:

$$-\frac{\hbar^2}{2} \frac{\partial}{\partial y} \left(\frac{1}{m_y^v(x, y)} \frac{\partial \Psi_{iv}}{\partial y} \right) + E_c(x, y) \Psi_{iv} = E_{iv} \Psi_{iv} \quad (1)$$

Here, $m_y^v(x, y)$ is a spatially dependent effective mass in y-direction for the v -th valley and $E_c(x, y)$ is a conduction band edge. The equation for holes is obtained by substituting hole effective masses instead of that of electrons and valence band edge $-E_v(x, y)$ instead of $E_c(x, y)$. ATLAS solves the one-dimensional Schrödinger's equation along a series of slices in the y direction relative to the device. The location of the slices in the y direction is developed in two ways. For rectangular ATLAS-defined meshes, the slices will automatically be taken along the existing mesh lines in the ATLAS mesh. If the mesh is non-rectangular or not an ATLAS defined mesh or both, a rectangular mesh must be specified. The potential derived from the solution of Poisson's equation is substituted back into Schrödinger's equation. This solution process (alternating between Schrödinger's and Poisson's equations) continues until convergence and a self-consistent solution of Schrödinger's and Poisson's equations is reached.

For the BQP model, there are two advantages over the density gradient method. First, it has better convergence properties in many situations. Secondly, one can calibrate it against results from the Schrödinger-Poisson equation under conditions of negligible current flow. The model introduces a position dependent Quantum Potential, Q , which is added to the Potential Energy of a given carrier type. This quantum potential is derived using the Bohm interpretation of quantum mechanics and takes the following form [12]

$$Q = -\frac{\hbar^2}{2} \frac{\gamma \Delta(M^{-1} \Delta(n^\alpha))}{n^\alpha} \quad (2)$$

where γ and α are two adjustable parameters, M^{-1} is the inverse effective mass tensor and n is the electron (or hole) density. The first part of the calibrating the BQP model against the Schrödinger-Poisson (S-P) Model, is to choose a suitable bias for the device. There should be

negligible current flow and quantum confinement effects that manifest at the chosen biases. The second part of the calibration is to set the appropriate BQP parameters. The third part of calibration is to choose the quantity to compare with S-P results. The BQP equation is coupled with Poisson's equation using the charge density terms:

$$n = N_c \exp\left(-\frac{E_c + qQ}{kT}\right), p = N_v \exp\left(-\frac{qQ - E_v}{kT}\right) \quad (3)$$

2.2. Tri-gate FinFETs

Typical p-type tri-gate FinFET is fabricated on 1000 Å SOI layer. The FinFET has a fin height of 30 nm. The fin width and fin length are varied from 60-90 nm and 60 nm to 100 μm, respectively. A 50 Å SiO₂ gate oxide is grown. Polysilicon gate was deposited of thickness 1500 Å, followed by pocket implantation and a 300 Å SiO₂ spacer deposition. A deep source/drain implant is followed. Silicidation is done for contact formation by 300 Å Ni/400 Å TiN depositions with RTA at 550-600°C for 1 minute. A 700 Å - 1 μm thick Al-pad is deposited for contact formation. The final device is annealed in forming gas at 420°C for 30 minutes.

3D Device Simulation

The 3D device structure simulated in ATLAS3D framework [13] of the tri-gate bulk Si-FinFET with fin height of 30 nm, fin width and fin length of 60 nm and 160 nm, is shown in Fig. 2. The simulation takes into account the quantum effects using the BQP model and the Schrödinger-Poisson solver. The tri-gate structure includes a poly-Si gate and a Si-Fin as a channel on the buried oxide (BOX). A gate oxide thickness of 5 nm is used for device simulation. The energy band diagram is shown in Fig. 3. depicting the conduction and valence band energies as a function of the distance along the Si-fin channel.

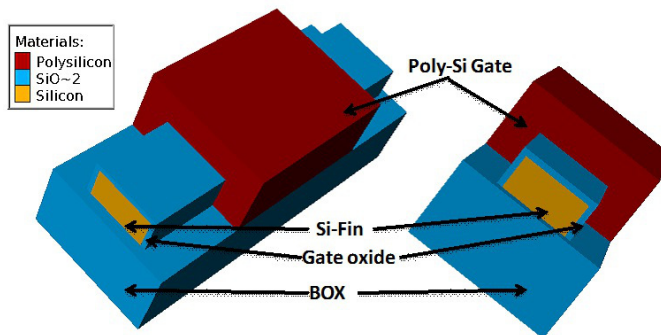


Figure 2. Simulated 3D device structure of a silicon tri-gate FinFET.

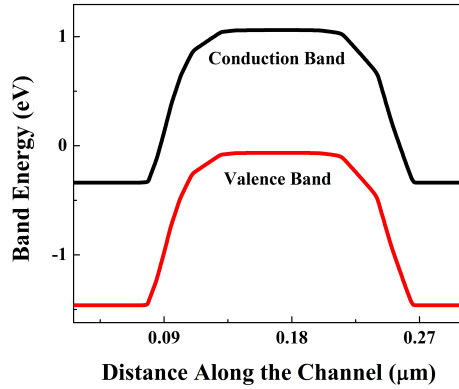


Figure 3. Energy band diagram of a tri-gate Si-FinFET.

Current-Voltage Characteristics

Figure 4. shows the measured I_D - V_{GS} characteristics of the p-type tri-gate FinFET. Typical device dimensions used for measurements are fin length of 160 nm, and width of 60 nm and oxide thickness of ~ 5 nm. The device displays excellent performance in terms of near ideal subthreshold slope (SS) (~ 82 mV/dec), and high I_{on}/I_{off} ratios ($\sim 10^6$). Figure 5. compares the measured I_D - V_{DS} with the TCAD simulation results which shows an excellent agreement showing the need of quantum 3D device simulation.

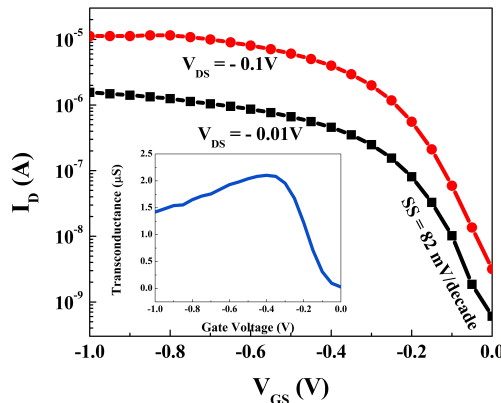


Figure 4. Typical measured I_D - V_{GS} characteristics of a tri-gate p-type Si-FinFET for two drain voltages; the inset shows the transconductance (g_m) plot as a function of gate voltage.

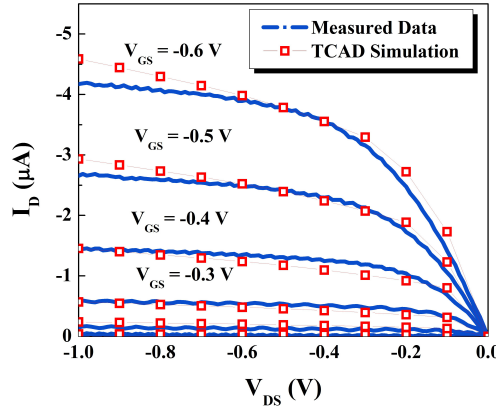


Figure 5. Comparison of I_D - V_{DS} characteristics of a tri-gate p-type Si-FinFET for results of both measured data and TCAD simulation.

2.3. Gate-All-Around Nanowire Transistors

GAA MOSFET is one of the most promising multi-gate structures to extend the scaling of the CMOS devices as it provides the best channel electrostatic control, which improves further with the shrinking of channel thickness. GAA MOSFETs have potential to offer enhanced carrier transport properties compared to planar devices, because of the high carrier mobility on sidewall planes. Careful design and fabrication are critical for GAA MOSFETs for obtaining better transport properties in such structures. The basic nanowire transistor fabrication process flow is illustrated in Fig. 6.

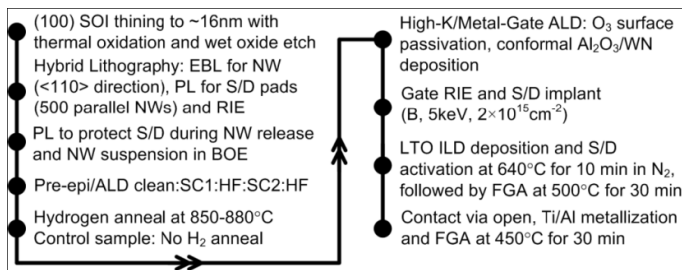


Figure 6. Typical nanowire fabrication process flow (After P. Hashemi, Gate-All-Around Silicon Nanowire MOSFETs: Top-down Fabrication and Transport Enhancement Techniques, PhD dissertation, Massachusetts Institute of Technology, 2010 [14]).

After definition of e-beam lithography (EBL) alignment marks, Si nanowires along <110> direction and S/D pads are defined by hybrid lithography. After reactive-ion etching (RIE) of

Si and stripping the resist, nanowires are locally released using a protective photo resist mask and a buffered-oxide etch bath. The suspended nanowires are then RCA cleaned and are subjected to hydrogen anneal process. Although thermally grown oxide benefits from excellent interface with Si nanowires, the facet dependence of the growth usually results in a non-uniform oxide thickness for various crystallographic planes. In addition, thermally grown oxide can induce a significant amount of stress in the nanowires which can alter their intrinsic carrier transport properties [15]. The ALD dielectric benefits from scalability to thinner effective-oxide-thicknesses (EOT) and its excellent conformality ensures that the entire perimeter of the Si nanowire is uniformly gated. The overlapped gate structures are designed for two reasons. First, it helps to minimize the S/D external resistance as the ion-implanted nanowires may exhibit very large series resistance. Second, it is technologically difficult to remove the metal gate stringers under the nanowires if the gate is under lapped. Moreover, any gate-first process to be used after vertical etching of the gate requires an isotropic etch of the gate metal stringers under the nanowires which also laterally etches the bottom gate and results in high extension resistance. After contact via opening and Ti/Al deposition and patterning, the fabrication is completed by a forming gas annealing at 450°C for 30 minutes.

The 3D device simulation is performed in ATLAS3D framework of SILVACO. The simulated device structure is shown in Fig. 7. depicting a cylindrical GAA FinFET structure with fin diameter ~10 nm and fin length of 100 nm with a surrounding gate oxide thickness of 10 nm. Gate electrode is defined with 70 nm overlap on source/drain. (100) SOI wafer (p-type, 10^{15} cm^{-3}) was the starting material with 200 nm Si on 150 nm buried oxide (BOX). The gate electrode deposition included 130 nm amorphous silicon (α -Si).

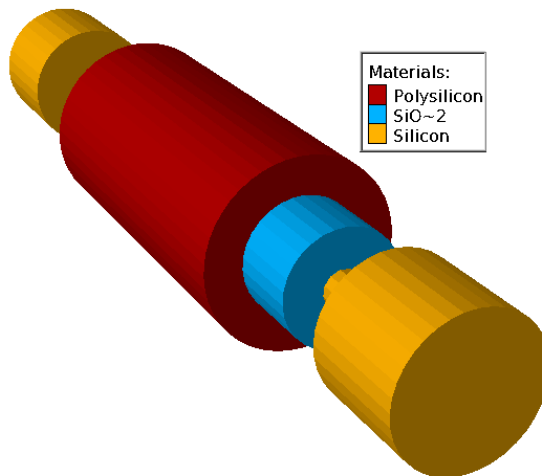


Figure 7. Simulated GAA nanowire FinFET structure.

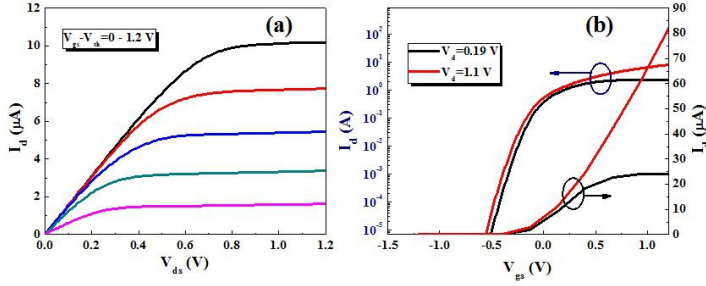


Figure 8. a): I_D - V_{DS} characteristics of a GAA Si-nanowire; (b): I_D - V_{GS} characteristics of a GAA Si-nanowire at two different drain voltages.

Figures 8 (a) and (b) show the typical I_D - V_{ds} and I_D - V_{gs} characteristics of a GAA n-FinFET, respectively. Typical device dimensions used for measurements are fin length of 100 nm, and diameter of 10 nm and oxide thickness of ~10 nm. The excellent subthreshold performance include a high subthreshold slope (SS) of ~90 mV/dec, and I_{on}/I_{off} ratios ~ 10^6 .

2.4. Carrier Mobility in FinFETs

Effective mobility extraction for the FinFET devices was based on an improved split C-V method, similar to planar device mobility extraction [4]. This technique relies on the accurate computation of the inversion charge (Q_i), as well as on the correct calculation of the channel conductance (g_c) along the different operation regimes. Effective channel mobility is defined as [16]:

$$\mu_{eff} = \frac{L_{eff}}{W_{eff}} \cdot \frac{g_c}{Q_i} \tag{4}$$

$W_{eff} = (W_{fin} + 2 * H_{fin}) * N_{fins}$ for a tri-gate structure and $W_{eff} = 2 * (W_{fin} + H_{fin}) * N_{fins}$ for a GAA structure; N_{fins} is the total number of fins, H_{fin} is the fin height. The inversion charge is obtained by integration of the accurate gate to channel capacitance data (C_{gc}).

$$Q_i(V_g) = \int_{V_G < V_T}^{V_G} C_{gc}(V) dV \tag{5}$$

The transfer characteristics and the gate-to-channel capacitance were measured using the split C-V technique to calculate the effective mobility of devices with fin width (W_{fin}) being 60 nm and the height of the fins (H_{fin}) being 30 nm. The effective mobility can be expressed in terms of top, bottom and sidewall mobilities; μ_{top} , μ_{bottom} , $\mu_{sidewall}$ in tri-gate and GAA structures, respectively, as:

$$\begin{aligned} \mu_{eff} W_{eff} &= \mu_{top} W_{fin} + 2 * \mu_{sidewall} H_{fin} \\ \mu_{eff} W_{eff} &= \mu_{top} W_{fin} + \mu_{bottom} W_{fin} + 2 * \mu_{sidewall} H_{fin} \end{aligned} \quad (6)$$

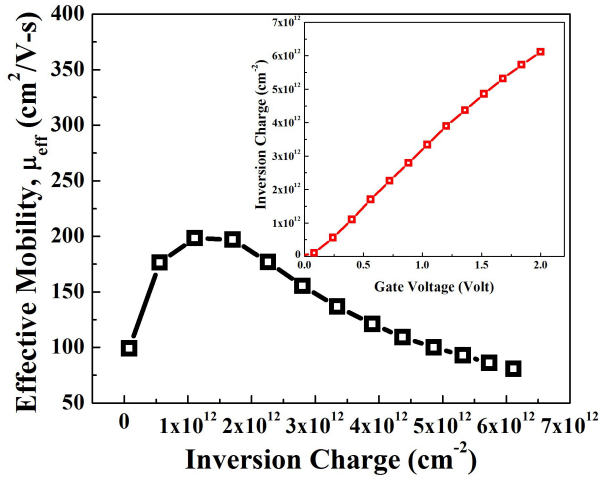


Figure 9. Extracted effective mobility in a p-type tri-gate Si-FinFET with gate length 160 nm, and gate width 60 nm; inset shows the inversion charge as a function of gate voltage.

A linear regression can be used to extract the sidewall and top-surface mobility. Eqs. (4) and (5) are used for calculating the effective mobility in the FinFET device from split C-V measurements. The inset of Fig. 9 shows inversion charge density as a function of gate voltage, as obtained from Eq. (5) using split C-V gate-to-channel capacitance. Figure 9 depicts the effective mobility of the FinFET as calculated using Eq. (4) as a function of inversion charge. The extracted mobility values agree well with the results of [16] for a p-FinFET of with gate length 160 nm.

2.5. Self Heating Effects in Nanowire Transistors

One of the significant challenges in future semiconductor device design is excessive power dissipation and rise in device temperature. With the introduction of new geometrically confined device structures like SOI, FinFETs, nanowires and incorporation of new materials with poor thermal conductivities in the device active region, the device thermal problem is expected to become more challenging in coming years. There is considerable degradation in the ON current due to self-heating effects in silicon nanowire transistors. However, insignificant current degradation is observed in nanowire transistors because of pronounced velocity overshoot effect. Placements of the source and drain contacts also play a significant role on the magnitude of self-heating effect in nanowire transistors. Self-heating and random

charge effects simultaneously influence the magnitude of the ON current for both positively and negatively charged single charges. The self-heating affects the ON current in two ways:

1. by lowering the barrier at the source end of the channel, thus allowing more carriers to go through and
2. via the screening effect of the Coulomb potential.

There is larger current degradation because of self-heating due to decreased thermal conductivity. Crystallographic direction dependent thermal conductivity is also an important aspect of self heating effects. Larger degradation is observed in the current along the [100] direction when compared to the [110] direction.

In SOI devices, the low thermal conductivity of the underlying silicon dioxide layer, which is about two orders of magnitude less than that of silicon inhibits cooling in SOI devices and causes severe self-heating, resulting in a higher channel operating temperature. The temperature rise is significant and depends on the buried oxide thickness, silicon thickness, and channel/metal contact separation. The device mobility is reduced as a result of the elevated temperature and results in reduced maximum drain saturation current. Also, high channel temperature leads to increase in interconnect temperature at the silicon-metal contact and make conduction cooling through the source, drain, and interconnects important. It should also be noted that the thermal conductivity of the silicon films decreases as the film thickness is reduced due to boundary scattering of phonons which further exacerbates self-heating and hence device performance. In brief, as semiconductor technology approaches to two-dimensional and three-dimensional transistor structures and are more isolated from the substrate self-heating effects will become increasingly important.

3. Low-Frequency Noise in Nanowire Transistors

Among various options for multi-gate device architecture, such as double-gate, tri-gate, etc., the nanowire (NW) channel with a wrap-around gate, GAA, has the largest advantage in terms of electrostatic integrity. However, several undesired effects become prominent from the miniaturization of the device dimensions. One such unwanted effect is a strong increase in the low-frequency noise generated in the transistor as the size of the device decreases. With dimension-scaling, it is necessary to also scale the power supplies. Noise cannot be completely eliminated and with small signal strength, the accuracy and measurements are limited in electronic circuits in presence of the dominant noise sources. The low-frequency noise, or $1/f$ noise, is the excess noise at low frequencies whose power spectral density approximately depends inversely on the frequency and becomes pronounced at low frequencies. The $1/f$ noise originating from the transistors is a severe obstacle in analog circuit design. For example, it can be up converted to undesired phase noise in voltage controlled oscillator circuits, which can limit the information capacity of communication systems. The problems in down-scaled devices such as the nanowire FinFETs compel one to study noise sources, mechanisms and their physical origins in detail. In this Section, we shall briefly dis-

cuss the two fundamental low-frequency noise characteristics, random telegraph signal noise and $1/f$ noise.

3.1. Low-Frequency Noise Measurement Setup

The standard noise measurement setup included an E5263A 2-channel high speed source monitor unit, a SR 570 low noise amplifier (LNA) and a 35670A dynamic signal analyzer. E5263A 2-channel high speed source monitor unit provided the necessary gate-source and drain-source biases as shown in Fig. 10. The minute fluctuations in the drain-source voltage were amplified to the measurable range using low noise amplifier. The output of the amplifier is fed to 35670A dynamic signal analyzer that performs the fast Fourier transform on the time domain signal to yield the voltage noise power spectral density (S_v) in the 1-100 kHz range after correcting for amplifier gain. In order to obtain a stable spectrum, the number of averages was set at 100 and a 90% sampling window overlap was used for optimal real time processing. A computer interface is connected with the measuring system through GPIB connection to control the dynamic signal analyzer and for noise data collection.

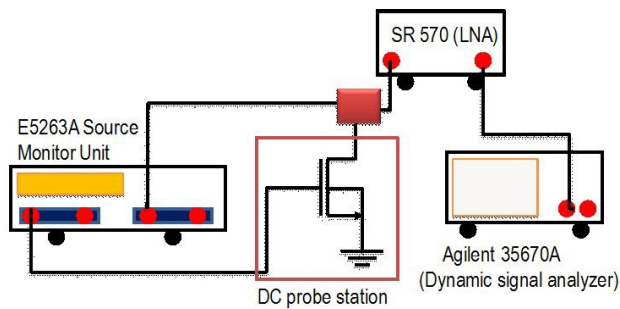


Figure 10. Low-frequency noise measurement setup.

3.2. Random Telegraph Signal (RTS)

RTS noise, also known as burst noise or popcorn noise is observed as random switching events in the time domain voltage or current signal. In a MOSFET, if a carrier is trapped in a single trap or localized defect state, the current or voltage signal displays a random shift in the level denoting a change in the channel resistance. The two-level RTS signal signifies only one active trap. However, when multiple traps are involved, the current (or voltage) can switch between two or more states resembling a RTS waveform due to random trapping and de-trapping of carriers and the phenomenon is much more difficult to explain in order to identify the trapping/de-trapping process. For simple two-level RTS pulses with equal height ΔI and Poisson distributed mean time durations in the lower state τ_l and in the higher state τ_h , the PSD of the current fluctuations is derived as [17].

$$S_I(f) = \frac{4(\Delta I)^2}{(\bar{\tau}_l + \bar{\tau}_h) \left[\left(1/\bar{\tau}_l + 1/\bar{\tau}_h \right)^2 + (2\pi f)^2 \right]} \quad (7)$$

Mainly two types of traps are identified depending on the nature of trapping mechanism. They are donor and acceptor traps. The donor trap is charged when it emits an electron (i.e. empty) and is neutral when it captures. The acceptor trap is, contrary to the donor trap, charged when it captures an electron and neutral when empty. In MOSFETs, the channel resistance increases with the charged-trap state changing the current (or voltage) to a high state. Clearly, the donor trap causes high current level after emission of carriers, and the acceptor trap causes the high current level when it captures an electron.

Depending on the values of the mean time constants of the RTS, the traps can be characterized of two types. These are the slow traps with high values of time constants, and the fast traps, with the time constants being very small (order of few 0.1 milliseconds). From RTS noise characterizations, interesting information about the trap energy, capture and emission kinetics and spatial location of the traps inside the semiconductor device can be acquired. The multi-level RTS is due to the activation of multiple traps near the quasi-Fermi level. With smaller area devices, only single traps are active as number of traps is less and the RTS becomes a simple two-level signal, with a Lorentzian PSD ($1/f^2$).

3.3. $1/f$ Noise

$1/f$ noise, also called flicker noise or pink noise, is the low-frequency noise with fluctuations with a PSD proportional to $1/f^\gamma$ with γ close to 1, usually in the range 0.7-1.3. The PSD for $1/f$ noise takes the general form

$$S_I(f) = \frac{KI^\beta}{f^\gamma} \quad (8)$$

where K is a constant and β is current exponent. There are various theories regarding the $1/f$ noise mechanisms of which most prominent are the carrier number fluctuation (surface phenomenon) and mobility fluctuation theories (bulk phenomenon). The mechanisms behind flicker noise are still a topic of research. The generally accepted origins of the $1/f$ noise are attributed to conductivity fluctuations, damage in crystal structures, and traps due to defects in semiconductors. $1/f$ fluctuations in the conductance have been observed in the low-frequency part of the spectrum (10^{-6} to 10^6 Hz) in most conducting materials and a wide variety of semiconductor devices [18, 19]. There are essentially two physical mechanisms behind any fluctuations in the current: fluctuations in the mobility or fluctuations in the number of carriers. In 1957, McWorther presented a $1/f$ noise model based on quantum mechanical tunneling transitions of electrons between traps in the gate oxide and the channel [20]. The tunneling time varies exponentially with distance from the trap and the $1/f$

noise is obtained for a trap density that is uniform in both energy and distance from the channel interface. The McWorther model is widely accepted for simplicity and its excellent agreement with experimental data, especially for nMOS transistors. However, the mobility fluctuation noise model explains the $1/f$ noise in pMOS transistors better [21]. It was later explained by the unified flicker noise theory that a trapped carrier also affects the surface mobility through Coulombic interaction. This correlated mobility fluctuation model gave a correction to the number fluctuation noise model which resolves the deviations of the theory for pMOS devices. However, the correction factor was debated for being very high since screening was not accounted for. Also, the carrier mobility at the surface is reduced compared to the bulk mobility due to additional surface scattering (by acoustic phonons and surface roughness), which has an impact on the mobility fluctuations. Moreover, the Hooge mobility noise is sensitive to the crystalline quality, which is deteriorated close to the interface. The most feasible explanation for the higher $1/f$ noise with the carriers being in close proximity of the gate oxide surface is increased mobility fluctuation noise.

3.4. Low-Frequency Noise

Figure 11 shows the RTS of a p-FinFET in time domain in a large span of 60 ms time for $V_d = -50$ mV and $|V_g - V_{th}| = 0.1$ V. For this particular RTS, two distinct sets of current switching levels are observed, each of which is consistent with trapping and de-trapping at a single discrete trapping site. A segment of the RTS is enlarged in the inset of Fig. 11 showing a distinct two-level RTS. This shows a fast varying RTS (with smaller time constants) is superimposed on a slow-varying RTS (with higher time constants) which generates the four-level RTS shown in the figure. This RTS is due to a slow (with higher time constant) and a fast trap (with lower time constant). The corresponding drain current spectral density is plotted in Fig. 12, with a corner frequency f_c and a Lorentzian $1/f^2$ nature. The traps are either donor or acceptor types as described in section 3.2. The high level in current corresponds to the charged trap state. With increasing gate bias, the trap occupancy increases [22]. Also, the time in the high current level increases with gate voltage. So the high level is the occupied charged-trap state or the emission time. The low-current level is the capture time from the same interpretation. The charged trap state is the occupied state which makes the trap to be an acceptor trap. The emission and capture time constants are thus identified in Fig. 12. The mean emission (τ_e) and capture time (τ_c) constants of the RTS in Fig. 11 are shown in Fig. 13 as a function of gate bias. The ratio of capture to emission times (τ_c / τ_e) shows a gradual decrease with gate voltage. The high current time being τ_e and the low current time as τ_c . The following can be written [22]:

$$\ln \left(\frac{\tau_c}{\tau_e} \right) = -\frac{1}{kT} \left[\frac{(E_{Cox} - E_T) - (E_c - E_F) - \phi_0}{+q\psi_s + \frac{qx_T}{t_{ox}} (V_{GS} - V_{FB} - \psi_s)} \right] \quad (9)$$

where $E_{C_{ox}}$ is the conduction band edge of the oxide, E_C is the conduction band edge of the silicon, Φ_0 is the difference between the electron affinities of Si and SiO_2 , t_{ox} is the oxide thickness, V_{GS} is the gate bias, V_{FB} is the flat band voltage, ψ_s is the surface potential and x_T is the position of the trap measured from the Si/SiO₂ interface. Differentiating in terms of the gate bias we can obtain the position of traps as:

$$\frac{d}{dV_{GS}} \ln\left(\frac{\tau_c}{\tau_e}\right) = -\frac{1}{kT} \left[\frac{qx_T}{t_{ox}} \right] \tag{10}$$

From Fig. 13, using Eq. (10), the trap depth is calculated as 0.172 nm from the Si/SiO₂ interface. A Lorentzian expression, as expected for an RTS [23, 24], is obtained as

$$WL \frac{S_{I_d}(f)}{I_d^2} = \frac{A}{\left[1 + (f/f_c)^2 \right]} \tag{11}$$

where A is a constant independent of frequency, $f_c = (1/2\pi)(1/\tau_c + 1/\tau_e)$, and τ_c and τ_e are the capture and emission times, respectively, of a single carrier by an interface trap. It can be seen that the corner frequency $f_c \sim 1$ kHz, which is consistent with the observed switching times in the order of 0.4–1.4 ms.

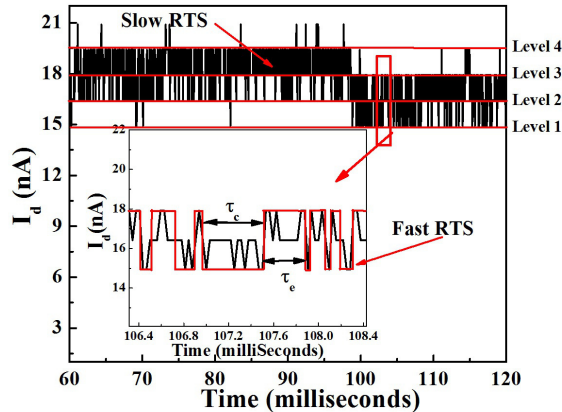


Figure 11. RTS of a p-FinFET in time domain for $V_{ds} = -50$ mV and $|V_{gs} - V_{th}| = 0.1$ V, depicting four levels with at least two traps; the inset shows a zoom of the fast RTS with the capture and emission time constants shown in the waveform.

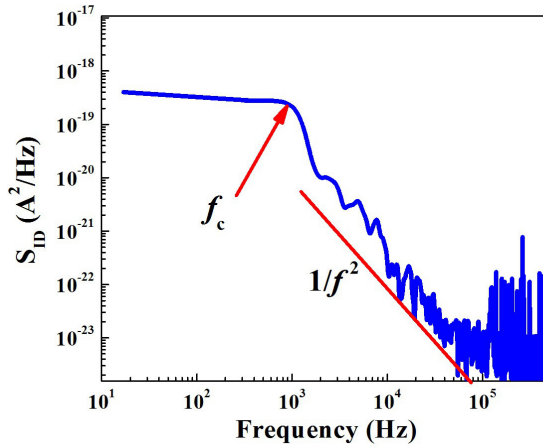


Figure 12. Drain current noise power spectral density with a corner frequency f_c and a Lorentzian nature ($1/f^2$).

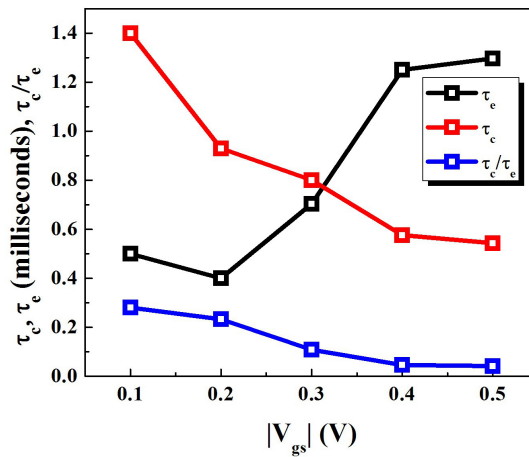


Figure 13. The mean emission (τ_e) and capture time (τ_c) constants and the ratio of τ_c/τ_e of the RTS are shown as a function of gate bias.

The entire FinFET channel is very thin and close to the interface and thus will be highly sensitive to interface defects. The defect potential perturbation, on the order of several nanometres, will have an effect on a significant cross section of the 10-nm-wide fin, hence producing a large current change when the trap is filled. The relative amplitude $\Delta I_d/I_d$ can be written as [25]

$$\frac{\Delta I_d}{I_d} = \frac{1}{WL} \left[\frac{1}{N} \pm \alpha \mu \right] \quad (12)$$

where N is the carrier density, α is the scattering coefficient, and μ is the carrier mobility. Using the double lateral channel FinFET approximation [26], $N = 2 C_{ox} |V_G - V_{TH}|/q$ and $\mu = g_m L / (2WC_{ox} V_d)$. The mobility limited by Coulomb scattering is calculated as $\mu_c = 1/\alpha N_t$, where N_t is the density of occupied traps [25].

4. Orientation Dependence: Nanowire FinFETs

Theory and measurements on planar transistors show a large difference in mobility for electrons and holes depending on the interface orientation and the direction of current flow in MOSFETs [27, 28, 29]. Figure 14 illustrates the measured drain currents (I_D - V_{DS}) for two different channel orientations; (100) and (110). It is observed that the current is higher in (100) orientation compared to the (110) orientation. The change in channel crystallographic direction (and thereby a change in the direction of current flow) greatly influences the carrier mobilities due to direction dependency of the heavy hole effective mass affecting the low field hole mobility. The effect of channel orientation is dominant in p-type devices due to different band curvatures along the <100> and <110> channel directions.

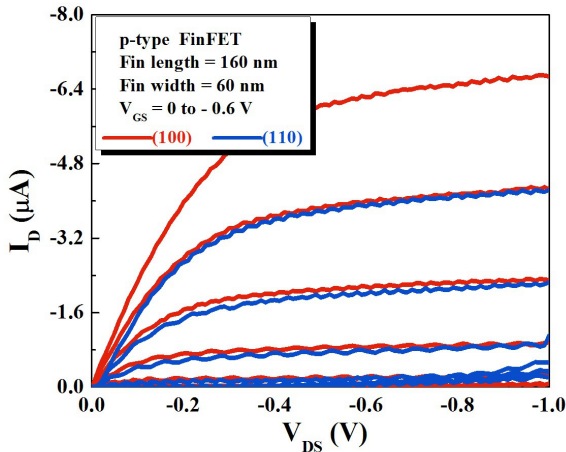


Figure 14. Comparison of the measured drain currents (I_D - V_{DS}) for two different channel orientations; (100) and (110) of a p-type tri-gate Si-FinFET.

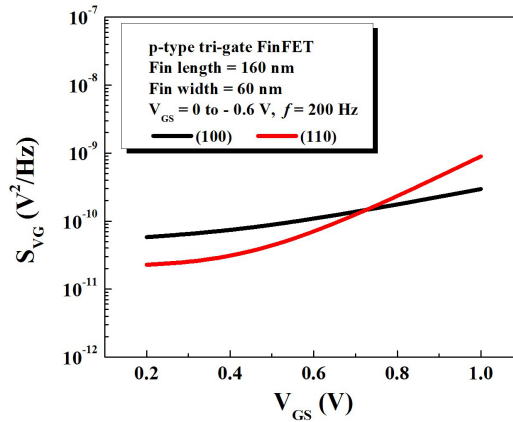


Figure 15. Comparison of the measured gate voltage noise power spectral density for two different channel orientations; (100) and (110) of a p-type tri-gate Si-FinFET.

The input referred gate voltage noise power spectral density (PSD) of the FinFET is shown in Fig. 15 for two different channel orientations ((100) and (110)) as a function of the gate-source voltage. It is observed that the gate voltage PSDs are comparable in magnitude for both orientations. It is well known that technological factors such as gate oxide quality, gate oxide material, channel material, conduction path, annealing, etc. can be of great importance for the low-frequency noise properties [30, 31, 32, 33]. The gate oxide quality and other technological factors can be considered as unchanged by the channel rotation, which explains why the orientation displays a negligible influence on the low-frequency noise. If the mobility fluctuation noise becomes dominant, the channel orientation may play significant part in determining the noise PSD. This is due to the fact that the carrier mobility depends on channel orientation. The difference in noise PSD for the two orientation is large in the subthreshold region. This is due to the fact that the mobility-fluctuation noise generation mechanism is dominant in the subthreshold region, since in the number-fluctuation model, there is no dependence of noise PSD on mobility at a fixed drain-current level. The channel orientation dependence of noise is more dominant in pMOS devices as also reported in reference 34. Stronger current and mobility enhancement in certain orientations may also cause a higher LFN level in the corresponding orientation.

5. Lattice Dynamics: Nanowire FinFETs

Lattice vibrations in small geometry devices and its orientation-dependence are important, which however, have not been studied in detail. Inelastic electron tunneling spectroscopy (IETS) has gained importance for characterization of small-geometry devices and ultra-thin-insulators due to its high resolution and sensitivity and has been used by many previous re-

searchers for studying defects and molecular vibrations in metal-insulator-semiconductor (MIS) structures [35, 36, 37, 38, 39, 40, 41].

The principle of IETS depends on the tunneling current through the ultra-thin dielectric layer of the MIS structures and becomes more sensitive as the tunneling current increases. Tunneling spectroscopy detects interaction of tunneling electrons (through the dielectric) with lattice vibrations of the substrate, dielectric, electrodes or other molecular species as inelastic peaks in the second derivative of the current-voltage characteristics. The application of tunneling spectroscopy was first demonstrated by Hall [36]. The technique of inelastic electron tunneling spectroscopy was properly introduced in 1966 by Jaklevic and Lambe [37]. With high sensitivity and resolution, IETS has been used for various applications including the determination of density of states, molecular vibrations, band gap of superconductors and semiconductors, defects in semiconductors and insulators [38, 39]. IETS has also been used for studying the traps and molecular vibrations in ultra thin oxides [40] and high-k gate dielectrics [41]. A tunneling spectrum reveals mainly the vibration energies of the molecules between the electrodes and phonon modes. Yanson *et al.* have shown that the intensity of the inelastic tunneling process is characterized by the relative change in $\Delta g/g$ for conductance g at energy $\hbar\omega$. The quantity $\Delta g/g$ is related to the observed I-V characteristics by the following expression [42]:

$$\frac{\Delta g}{g} = V \int_{V_1}^{V_2} \frac{1}{I} \frac{d^2 I}{dV^2} dV \quad (13)$$

where, V_1 and V_2 are the starting and ending voltages of the vibration band under consideration. This relation can be used to quantify the strength of the vibration modes, i.e. the change in the $\Delta g/g$ ratio indicates the strength of the interactions. In the following, we present the experimental tunneling spectra of Si, SiO₂ phonon modes obtained for p-type Al/SiO₂/Si tri-gate FinFETs and study the influence of crystal orientation. A comparison of lattice vibration modes and dispersion characteristics for (100) and (110) silicon orientation in tri-gate FinFET is made. It is observed that the lattice dynamics of silicon and SiO₂ changes for different crystal orientations.

The low temperature (77K) inelastic electron tunneling spectroscopy measurement setup includes an E5263A 2-channel high speed source monitor unit for dc biasing, and a SR830 DSP lock-in amplifier for capturing the tunneling spectra by measuring the second derivatives of the current-voltage characteristics. The setup is shown in Fig. 16. AC modulation signal generated from oscillator output of the lock-in amplifier with $f = 890$ Hz, peak amplitude of 2 mV, is superimposed on a slowly varying dc gate voltage. A time constant of 3 sec was used. A notch filter in the lock-in amplifier was used to remove the unwanted harmonic frequencies. A computer interface is connected with the measuring system through GPIB connection to control the dynamic signal analyzer and for noise data collection.

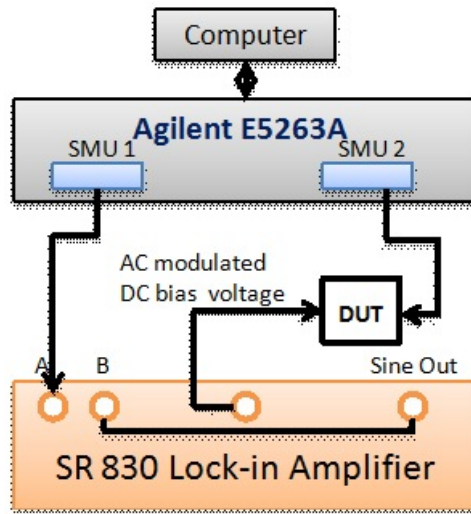


Figure 16. IETS measurement setup.

The phonon spectra of Si are observed in the 0-70 mV range. Figure 17(a) shows the inelastic peaks in the phonon spectra of Si for FinFET on (100) silicon orientation obtained from the average of six scans after de-convolution of the IETS spectra. The most intense peak is found at 60 mV (wave number 483.9 cm^{-1}). The peak is due to optical phonons at the conduction band minima (X-point) of silicon in transverse optical (TO) mode. Other significant Si-phonons include longitudinal acoustical (LA) phonon peak towards the X point at 47.2 mV (380.6 cm^{-1}), the longitudinal optical (LO) phonon towards X point at 53 mV (427.4 cm^{-1}). The transverse acoustic (TA) mode was observed at 19.7 mV (158.9 cm^{-1}). Phonons of Al-electrodes are observed at 26 and 33 mV. These findings are in well agreement with reported results for Si phonons with (100) orientation [35]. The values of phonon frequencies of unstrained silicon were calculated by Sui et al. using a modified Keating model [43]. The experimental values are compared with these theoretical values. We suspect the minor shifts in peak locations are due to the inherent strain in the small geometry structure of the FinFET. The TO and LO mode towards the Γ point, however, was not observed from the IETS. Figure 17(b) shows similar phonon modes of silicon for (110) orientation. From the Brillouin zone of the Si-crystal the dispersion in (110) direction is calculated along the main symmetry directions $\Gamma \rightarrow X$ through K point and $X \rightarrow X$ through W point [44]. The identified peaks include TO mode at Γ and W points, respectively, at 68 (548.4 cm^{-1}) and 58 mV (467.7 cm^{-1}). LO and LA mode towards X point are found at 54 (435.5 cm^{-1}) and 45.6 mV (367.7 cm^{-1}), and LA towards K point is observed at 41 mV (330.6 cm^{-1}). The TA modes at X and W points are observed at 19.5 (157.3 cm^{-1}) and 26 mV (209.7 cm^{-1}), respectively. The peaks at W point or K point are mostly of weaker intensity compared to the peaks at Γ and X points, which are the conduction band minima for the lattice. Also, unlike the (100) orientation, the symmetry di-

rections in (110) orientation reveal inelastic interactions at the K and W points along with the Γ and X points which describes the Brillouin zone for Si in more detail.

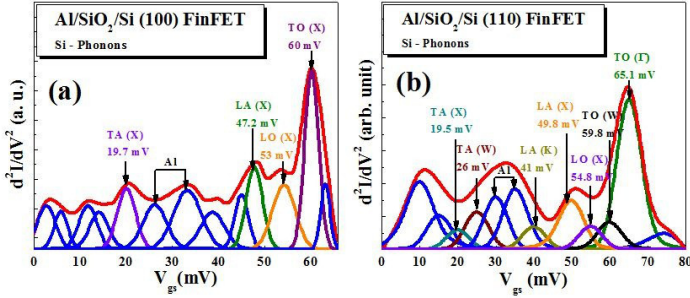


Figure 17. IETS spectra showing Si-phonons in a Al/SiO₂/Si FinFET for (a) (100) channel orientation and (b) (110) channel orientation.

Figures 18 (a) and (b) show the SiO₂ phonon modes (in the 129-170 mV range) for (100) and (110) orientations, respectively. The peaks exhibit almost the same energy position for both the Si (110) and Si (100) devices. These peaks include, TO3 mode at 134 mV, LO4 at 144.2 mV, TO4 at 149.8 and 153.4 mV for (100) device. The corresponding peaks for (110) devices are observed at 132, 144.2 148 and 159 mV, respectively. The main discrepancy between the two orientations comes in the magnitude of the phonons. The asymmetric stretch TO4 mode is theoretically found at 148.8 mV [45] which appears as a strong peak in the Si (110) device, and as a weak peak in the (100) orientation, as also described by [35]. The ratio of intensities of vibration modes may vary for different orientations of the molecular dipoles in the tunnel oxide barrier for different device orientations.

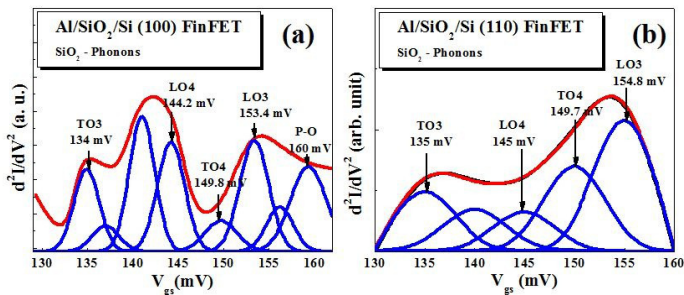


Figure 18. IETS spectra showing SiO₂-phonons in a Al/SiO₂/Si FinFET for (a) (100) channel orientation and (b) (110) channel orientation.

6. Summary

In this chapter, we have discussed silicon nanowire FinFETs in detail. Several important electrical characteristics such as mobility, self-heating, low-frequency noise, impact of channel crystallographic orientation and lattice dynamics are presented for nanowire FinFETs. The fabrication process flow of the nanowire and FinFETs are described. Application of split C-V measurement to calculate effective carrier mobilities is shown and mobility models for FinFETs including side and top-wall mobilities are developed. Low-frequency noise measurements are performed and results of $1/f$ noise and RTS in FinFET devices are presented. Effects of channel orientation on current drive and low-frequency noise are discussed. Lattice vibrations and phonon mode of Si and SiO₂ are studied for (100) and (110) channel orientations and Brillouin zone boundaries of the semiconductor are explored. Crystal dynamics in FinFETs are explained via inelastic electron tunneling spectroscopy. It is expected that the combination of strain effects with NWs can lead to very high performance devices.

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