CMOS BEOL-embedded *z*-axis accelerometer

P. Michalik, J.M. Sánchez-Chiva, D. Fernández and J. Madrenas✉

A first reported complementary metal-oxide semiconductor (CMOS)-integrated acceleration sensor obtained through isotropic inter-metal dielectric (IMD) etching of a back-end-of-line (BEOL) integrated circuit interconnection stack, without any additional substrate etching steps, is presented. The mechanical device composed of a CMOS-process 8 µm-thick metal-via-metal stack of 135 µm diameter and suspended 2.5 µm over a bottom fixed electrode, has a resonance frequency of 20 kHz, a sensing capacitance of 50 fF with sensitivity 14 aF/G and it is integrated on the same substrate with a simple low-noise amplifier reaching 25 mG of RMS noise measured from 0.25 to 100 Hz bandwidth.

Introduction: The micro electro mechanical systems (MEMS) inertial sensors market has experienced rapid growth because of the popularisation of consumer electronic devices such as smartphones, GPS, video game consoles and so on where the total device price and size are the critical factors [1]. Most of the currently available sensors are either multi-chip modules or fully integrated devices using a custom MEMS process. In both cases the necessity of a separate MEMS process is a bottleneck for price and size reduction trends.

A possible way to address this challenge is a full integration of multiple sensors with CMOS read-out electronics using CMOS micromachining and standard back-end-of-line (BEOL) metal layers as the structural material. Existing solutions are based on reactive ion etching of the BEOL stack followed by substrate etching [2] and they do not provide sensor integration on top of the electronics. Isotropic (wet or dry) etching of the inter-metal dielectric (IMD) layers [3, 4] has been applied mainly to develop relatively simple RF-MEMS devices [5, 6]. Its application to inertial MEMS, where a possibly big suspended mass is needed, required additional substrate etching as well [7].

Nevertheless, the presence of thick metal layers in RF-oriented CMOS and BiCMOS technologies opens a possibility of using simple isotropic IMD etching to develop monolithically integrated inertial sensors. Such sensors could become new IP cores ready to integrate in more complex SoCs and if a sufficient number of metal layers is available, a sensor integration on top of the electronics could provide a next major breakthrough for device cost and size reduction.

In this Letter we present a *z*-axis CMOS-integrated acceleration sensor obtained using isotropic IMD etching of the BEOL interconnection stack performed without any additional substrate etching steps.

Acceleration sensor: The device was produced using the IHP 0.25 µm process. One additional mask was used to protect the passivation layer with photoresist. The samples were released at dice level at the UPC-DEE cleanroom and the etching was done using buffered oxide etchant, followed by resist removal and a rinse in methanol which because of the low surface tension reduces stiction problems. Finally the samples were dried in an oven.

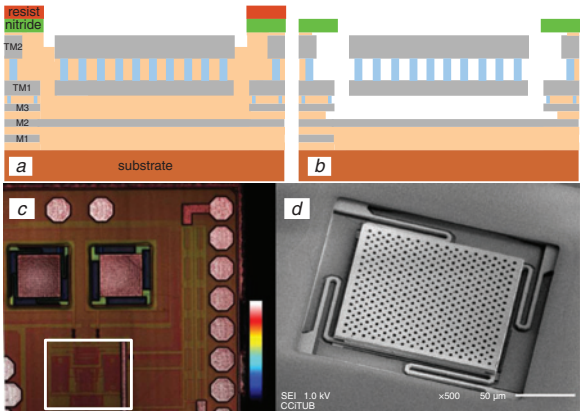

Fig. 1 *Pre-release (Fig. 1a) and post-release (Fig. 1b) cross-sections; confocal topography with highlighted sensing electronics (Fig. 1c); SEM image (Fig. 1d)*

In Fig. 1 the MEMS device cross-section before and after etching as well as the SEM image and confocal topography are presented. The 8 µm stack composed of two top thick metal layers and the via in between is used as the accelerometer square-shaped proof mass suspended over a fixed bottom electrode. Such a plate composition prevents device curling because of residual stress and provides a relatively big mass of 0.6 µg, sensing capacitance in range of 50 fF, a sensitivity of 14 aF/G (G≈9.81 m/s^2) and a 20 kHz mechanical resonance measured at mBar range pressure. Apart from the sensor, a dummy MEMS device of the same size with stiff suspension is placed as a reference capacitance to reduce the sensor offset to a level manageable by the tuning circuit.

Sensing electronics and off-chip signal processing: The acceleration signal is picked up using the continuous-time synchronous modulation-demodulation technique. To reduce the design cycle and complexity, in the current prototype only the most critical block – the low noise sensing amplifier – was monolithically integrated, while both the modulator and the demodulator blocks were implemented off-chip.

The signal processing chain (Fig. 2*a*) starts from an impedance network (ZN) that combines 1 MHz carrier with accelerometer DC bias and with optional low frequency test signal that electrostatically actuate the accelerometer. The network also compensates the offset between the accelerometer and its dummy copy by tuning the phase and amplitude difference between V_{ip} and V_{in} driving signals. These are applied to the MEMS bottom plates to cancel their high parasitic capacitance.

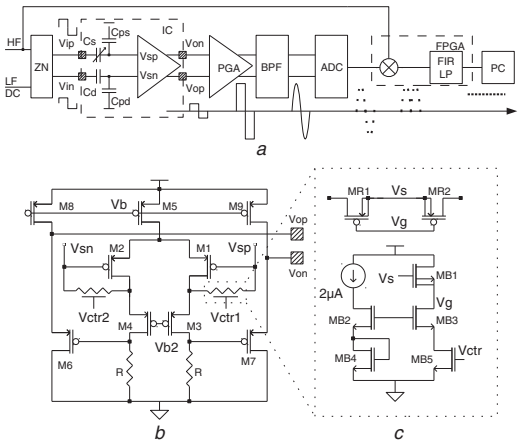

Fig. 2 *Signal processing chain architecture (Fig. 2a); integrated LNA schematic (Fig. 2b); subthreshold floating resistor providing sensing nodes with DC bias (Fig. 2c)*

The sensor and dummy capacitors (C_S, C_D) form voltage dividers with parasitic capacitors (C_{PS}, C_{PD}) associated with their top electrodes (200 fF appr.) and input capacitance (65 fF appr.) of the sensing amplifier (Fig. 2*b*). A simple single-stage fully differential low-noise amplifier with input transistors (M1, M2) sized for optimal sensor SNR at 1 MHz chopping frequency was used. The DC bias of the sensing nodes is applied through subthreshold floating resistors (Fig. 2*c*) working at GΩ range, so that the thermal noise associated with DC bias is pushed by the parasitic capacitance to frequencies well below the carrier. The cascode transistors (M3, M4) minimise the Miller capacitance that would attenuate the sensor signal, while the poly-resistor load establishes a relatively low gain of 15 dB making the common-mode feedback unnecessary. The amplifier output nodes are buffered with source followers (M6, M7) to provide sufficient driving strength. The circuit is supplied with 3 V and the LNA and source follower consume 100 µA each.

The signal from the chip is amplified with a programmable-gain amplifier (PGA) and bandpass filtered around the carrier frequency, so that the out-of-band noise is removed and the signal dynamic range fits to the next block – the ADC. The rest of the signal processing is done in the digital domain using a FPGA – the signal is demodulated with a clock phase-locked to the carrier and lowpass filtered, providing 100 Hz output bandwidth in the most typical configuration.

Measurements: The response to the orientation change (Fig. 3*a*) as well as to 30 Hz vibration (Fig. 4) was compared with a reference accelerometer LIS331. Considering that the mechanical transducer has a sensitivity much smaller than bulkier state-of-the-art sensors, a reasonable noise floor of 2 mG/$\sqrt{Hz}$ was measured at 30 Hz (Fig. 4) as well as an RMS noise of 25 mG over the bandwidth from 0.25 to 100 Hz.

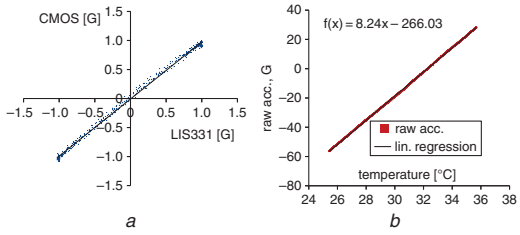

Fig. 3 *CMOS accelerometer output against LIS331 reference accelerometer output obtained during slow device rotation (Fig. 3a); prior-compensation temperature characteristics of sensor (Fig. 3b)*

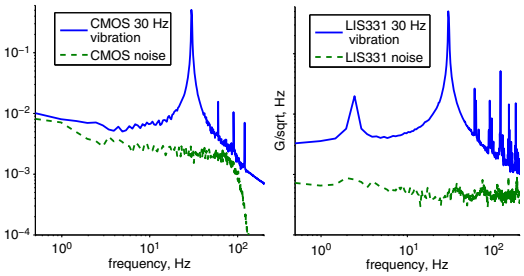

Fig. 4 *Spectra of 30 Hz vibration and noise (no excitation) for CMOS (left) and LIS331 (right) accelerometers obtained through 2048 pt*
FFT averaged over 16 datasets

The sensor demonstrated relatively high sensitivity to temperature, which was found to be 8.24 G/°C. By comparison with an unreleased sample, it has been checked that the effect was dominated by the MEMS device and not the sensing electronics, however it is not clear whether its main cause is the intrinsic change of the suspended plate shape or it is induced by packaging or board stresses, the effect of which was observed during the test board handling.

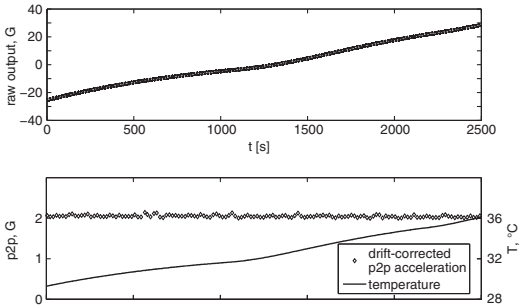

Fig. 5 *Output of device being flipped each 9 s (top) in presence of temperature rising from 29 to 36°C (bottom)*
Peak-to-peak acceleration after drift removal (bottom) shows no significant gain dependence on temperature

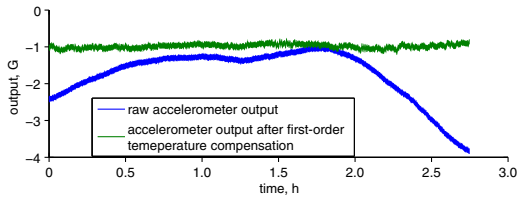

Fig. 6 *Long-time measurement of −1 G acceleration before and after first-order temperature correction*
Temperature sensor data sampled at 1 S/s rate and lowpass filtered to 0.1 Hz bandwidth

The temperature characteristics did however exhibit very good linearity (Fig. 3*b*) and no visible gain dependence (Fig. 5), which makes a precise thermal compensation relatively easy to implement if an on-chip temperature sensor is used. An attempt of a first-order temperature correction using a discrete temperature sensor was made. Despite a transient temperature error between the temperature sensor and the accelerometer, it was possible to achieve long-term stability at the cost of some resolution deterioration at shorter observation times (Figs. 6 and 7).

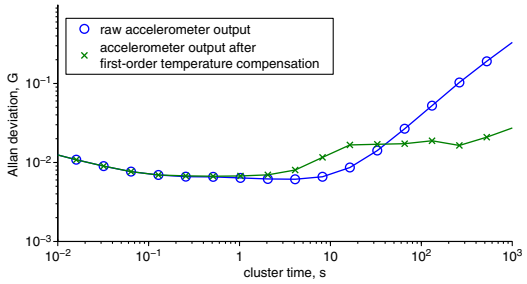

Fig. 7 *Allan deviation measured before and after first-order temperature correction calculated over signals from Fig. 6*

Conclusion: We have presented, to the best of our knowledge, a first ever reported acceleration sensor obtained by isotropic IMD etching of a CMOS BEOL without applying any additional substrate etching. Despite the limitations of the materials available in the CMOS BEOL process and very simple on-chip electronics, the sensor demonstrated a performance suitable for vibration detection (where the DC drift is not critical). If a proper on-chip temperature compensation were applied, it could be applicable for motion detection. Its main advantage is integration on the CMOS die and a very small footprint of 250 × 250 μm^2. Furthermore, as not full BEOL stack is used, it could be feasible to integrate it on top of the electronics, thus providing an even more competitive overall sensor area.

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One or more of the Figures in this Letter are available in colour online.

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