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Procedia Computer Science

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ICEBT 2010

High Speed VLSI architectures for DWT in Biometric Image Compression: A Study

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Abstract

Biometrics is a field that navigates through a vast database and extracts only the qualifying data to accelerate the processes of biometric authentication/recognition. Image compression is a vital part of the process. Various Very Large Scale Integration (VLSI) architectures have emerged to satisfy the real time requirements of the online processing of the applications. This paper studies various techniques that help in realizing the fast operation of the transform stage of the image compression processes. Various parameters that may involve in optimizations for high speed like computing time, silicon area, memory size etc are considered in the survey.

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Keywords:Biometrics; VLSI architectures;image compression;Discrete wavelet transform;Lifting Scheme; speed optimisations;

1. Introduction

This paper is a survey done to explore the part of image compression in the field of biometrics. We know that biometrics is the science of using biological features and behavior as characteristics of human beings to identify and authenticate the person for security purposes. This involve the standard database creation and query data to be validated by comparison and collusion. The enormous data that result out of it need image compression to save memory, hardware complexity, cost and compactness. This requirement has gained paramount importance as these biometric methods of security and identification has pervaded highly sensitive and critical areas like military, electoral body, nuclear reactor stations, oil fields, airports etc. The biometric system, image compression model and various VLSI architectures of the Transform stage of it for optimized parameters are discussed in the following sections

1.1 Biometric system:

The system consists of basically two phase of operation: enrollment and verification. The sample of the characteristic that is unique to a person is the template. The characteristics may be physiological, like fingerprints, hand/palm geometry, retina or iris of the eye, or facial characteristics or behavioral characteristics like signatures, voice and gait. Iris recognition has low failure rate. It uses features like furrows, ridges, coronas, crypt rings to characterize the sample. Similarly fingerprints have features like minutiae points. So template and query samples are preprocessed and feature- extracted to serve as a data base for identification by comparison of sample with template.

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doi:10.1016/j.procs.2010.11.028

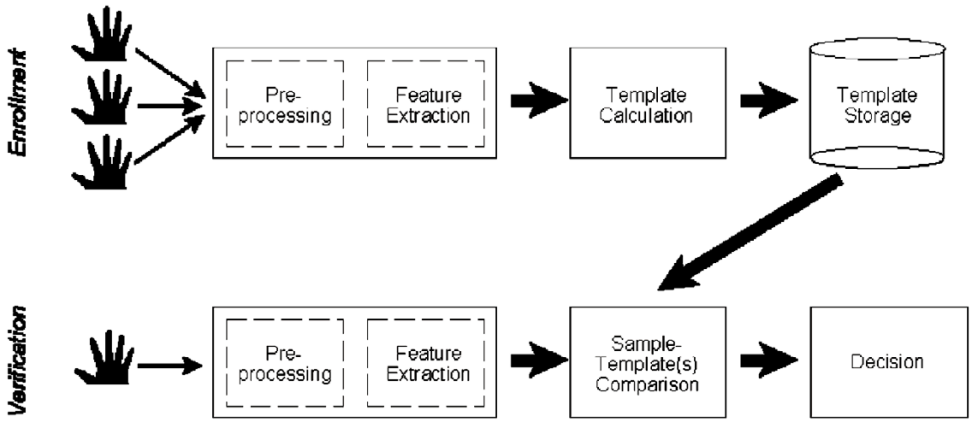


Fig. 1.A Biometric system

This system does not have loss or stealing of characteristics. It requires the physical presence of the person at the identification point. It obviates memorizing of passwords and keys. No other person can duplicate the identity. Because of its advantages it has evolved with newer technologies using features like DNA, ear shape and odor and finger geometry for supplementary characteristics in multi-biometric system.

1.2 Discrete Wavelet Transform

Image compression reduces the size of data to be stored by removing the redundant data within the message data. Redundancy may be either in data or interpixel or psychovisual [1]. The basic model has the following stages

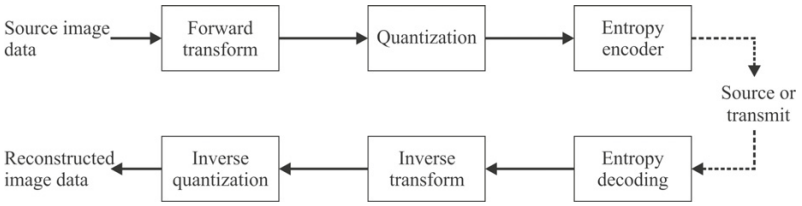


Fig.2. Basic Image compression model

Wavelet transforms have superseded other transform like Fourier transform, short term Fourier transform and discrete cosine transform because of their disadvantages. Fourier transform does not have frequency and time resolution simultaneously. Short term Fourier transform are not tractable like Discrete Wavelet Transform. Discrete cosine transform is computationally intensive transform compared to wavelet transform. So Discrete Wavelet transform is reigning over the transform domain with a bouquet of mother wavelets such as Haar, Mortlet, coifflet, Daubechies, Biorthogonal spline wavelets and many more. For image transmission and compression perfect reconstruction transforms are mandatory. Wavelet transform is realized as convolution of down sampled input x(i) with wavelet filter h(i) [2]:

$$Y_L(n)=\sum_{i=0}^{\frac{N}{2}-1} h(2n-1).x(i)\,.\,Y_{H(n)} = \sum_{i=0}^{\frac{N}{2}-1} g(2n-1).x(i) \quad (1)$$

To ensure perfect reconstruction quadrature mirror filter banks are used with filter coefficient relationship

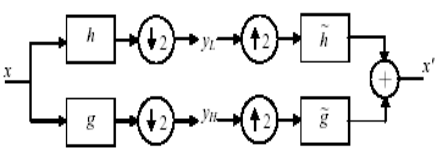
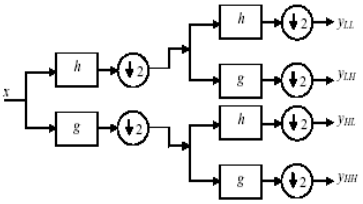


Fig. 3.(a)Analysis and synthesis filter structure



(b) Two – level multivelevel decomposition

$$\check{g}(k) = (-1)^k h(n-1-k) \tag{2a}$$

$$g_{-2} = \tilde{h}_3 = g_4,$$
$$g_{-1} = \tilde{h}_2 = g_3,$$
$$g_0 = \tilde{h}_1 = g_2,$$
$$g_1 = \tilde{h}_0. \tag{2b}$$

With refinement relation existing between the scaling functions, multilevel decompositions are possible [2].

1.3 Lifting Scheme

The computational intensity of convolution FIR filters is very high and the memory requirement to store the intermediate results is also enormous. To reduce the complexity lifting scheme is used. Its other advantages are [3]

- Signals of any arbitrary size are transformed with correct boundary treatment
- Spatial domain operation avoiding Fourier analysis
- Increase in speed of computations by factor 2
- In-place computation using minimum of the memory for storage.
- Perfect reconstruction from analysis coefficients.

Lifting scheme is implemented by factorization of polyphase matrix P(z) into lifting steps using Laurents polynomials[4,5] . On analysis side the steps are

Split: splitting input data as odd (detail) and even (approximate) signals.

Predict: step that changes the detail coefficients

$$\text{Odd}_{j+1,i} = \text{odd}_{j,i} - P(\text{even}_{j,i}) \tag{3}$$

Update: step that changes the approximate coefficients.

$$\text{Even}_{j+1,i} = \text{even}_{j,i} + U(\text{oddj+1,i}) \tag{4}$$

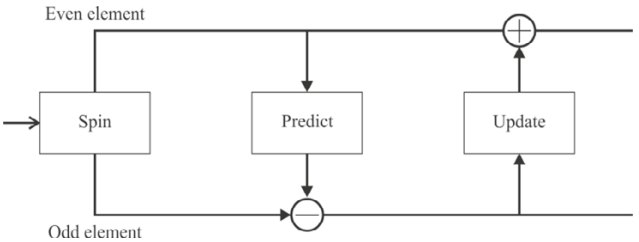


Fig. 4. Lifting Scheme – analysis

Synthesis lifting stages proceed in the reverse order: update, predict and merge to get back the image coefficients.

The recent Image compression standard JPEG 2000 has adopted lifting scheme of DWT for its preprocessing stage using 9/7 filters for lossy compression and 5/3 filters for lossless compression. In 9/7 filter, two predict & update stages are used and in 5/3 filter, one stage is used. For 5/3 filters the following equations are true

$$\tilde{h}(z) = \frac{1}{8}z^{-2} + \frac{1}{4}z^{-1} + \frac{3}{4} + \frac{1}{4}z - \frac{1}{8}z^{2} \quad (5)$$

$$\tilde{g}(z) = \frac{1}{4}z^{-2} + \frac{1}{2}z^{-1} + \frac{1}{4} \quad (6)$$

Analysis polyphase matrix in z-domain

$$P(z) = \begin{bmatrix} He(z) & Ho(z) \\ Ge(z) & Go(z) \end{bmatrix} \quad (7)$$

$$P(z) = \begin{bmatrix} 1 & 1 \\ 0 & \frac{1}{2} \end{bmatrix} \begin{bmatrix} 1 & \frac{1}{4} + \frac{z}{4} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ -\frac{z}{2} - 1 & 1 \end{bmatrix} \quad (8)$$

2. Survey of VLSI architectures

The hardware to implement the lifting scheme involves adders and multipliers. To optimize the goals of VLSI technology – low power, high speed, less cost, smaller area and high throughput, innumerable architectures have been explored and developed as modification and hybridization of basic signal processing principles like

- Pipelining
- Folding
- Parallel processing
- Flipping.

The Folded architecture using pipelining proposed by Wang et.al[7] for Discrete Wavelet Packet Transform and a similar technique proposed for Discrete wavelet transform by Hsieh et.al [8] reduces the hardware cost and improves the hardware utilization by folding technique. Pipelining is used in processing elements to reduce the critical path and increase the throughput. The flipping architecture proposed by Huang et.al [6] section, multiplies the inverse coefficient for every edge on the feed-forward cutset through the selected multiplier to reduce the critical length and minimizes the internal memory. The disadvantage with pipelining is its introduction of latency and registers in the hardware. A better VLSI signal processing technique is flipping. The architecture implemented by Huang et.al [9] minimizes the critical path without increasing the line buffer memory .The technique illustrated as below flips the multiplier coefficient with its inverse on the path from input node to computation node. The computation node is split into adders for parallel processing with other units.

Parallel Architectures using pipelining are proposed by Sung et.al [10] and Xiong et.al [11].The architecture proposed by Xiong et al has a performance which is a tradeoff among hardware cost, throughput and output latency. Four filters – two vertical and two horizontal filters accept inputs from FIFO RAMs in a parallel fashion and generate 4 outputs using pipelined processing elements. An efficient architecture called Double path Delay commutator that is based on pipelining is discussed by Wang and Gan[12]. It has high throughput of DWPT coefficients by pipelining. By Folding coefficents are configured to avoid on chip memory. The architecture of Saeed and Augustiawan[13] has higher computational rate using pipelined data path for lossless 5/3 filters and lossy 9/7 filters. The control logic is simple as internal buffers are avoided. Lack of external frame buffers lowers power consumption of the architecture. Higher efficiency, better computation rate and higher hardware utilization is achieved by parallel scan and process of 3 pixels in each cycle.

At algorithmic level techniques like Canonic Signed Digit (CSD) representation, fast convolution, etc have been investigated. Of the various parameters of optimization factors that help in faster DWT computation are considered in this paper. Four architectures that adopt different principles are discussed here.

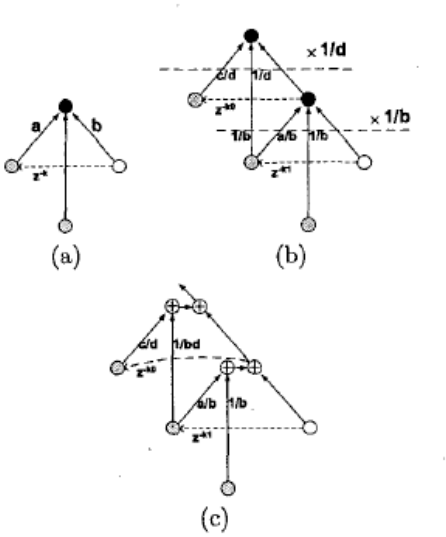


Fig. 5. Flipping operation (a) Basic computing unit (b) flipping computing unit (c) after splitting computing nodes

DWT may be implemented in non-separable fashion, as in [14]. Here the 2-D Transform is not realized as column processing followed by row processing as in [15]; rather in a serial parallel filtering method. The transform module operates at a frequency of 105 MHz with computation time of $2/3*(1-1/4^{L})*N*N$ where L is level of decomposition for 5/3 filter.

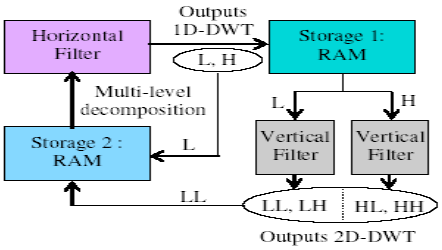


Fig. 5. Serial- Parallel module transforms

Though lifting scheme has better advantages Mountassar et.al [2] have found favor with the conventional convolution method. Direct implementation of lifting architecture has a critical path of multiplier delay (Tm) and adder delay (Ta) as 4 Tm +8Ta . But the fast convolution proposed has a delay of Tm +2Ta. Fast D latch and high speed memory with independent dual input and output achieves an operating speed of 275 MHz for 9/7 filter

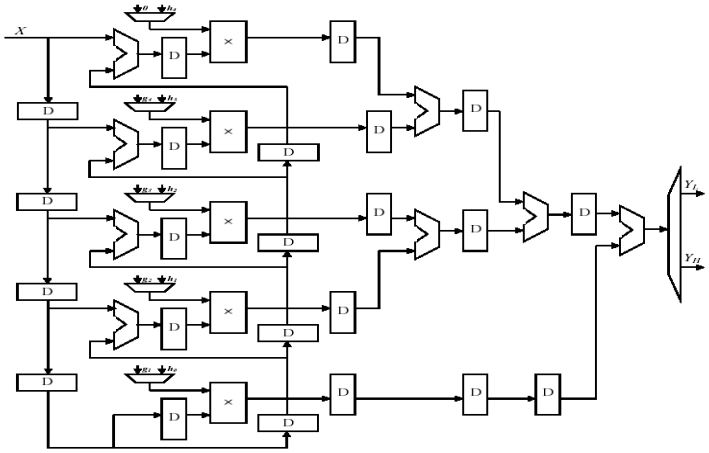


Fig. 6. Fast convolution based DWT

The architecture proposed by [16] is based on pipelining. In lifting scheme implementation a Transpose buffer of size N (image size N*N) is required when row processing is followed by column processing. This buffer is

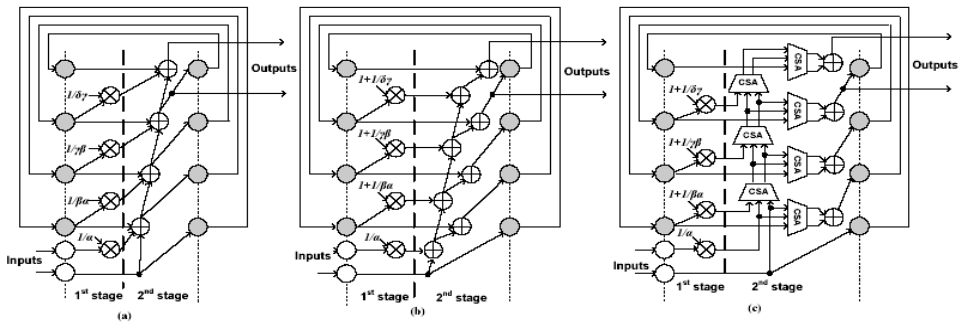


Fig.7 (a) proposed pipeline architecture (b) Changing computing topology (c) applying arithmetic optimisations

avoided using a dual line scan that scans 2 lines of data at a time. The critical path is reduced to one multiplier delay (T_m) using carry save adders (CSA) in the II stage whose delay is that of a single bit full adder. This enables higher operating frequency. This architecture uses 4 multipliers and 6.3 CSAs.

The pipelining architecture proposed by Mansouri et al.[17] aims for computational speed as high as 350MHz with a regular structure smaller transpose buffer. The computation time is N+ (N^2/2). It uses 8 adders and 4 multipliers for 9/7 filtering.

The architecture proposed by Alireza et. al [18] aims to improve the computational quality by improving the PSNR (Peak signal to noise ratio) compared to a standard architecture working with same frequency for a 9/7 filter. The architecture uses Canonic signed digit (CSD) representation of multipliers to reduce the hardware cost. CSD optimizes the number of ones used in multiplier representation to the minimum. By using a balanced pipeline and altering the constant lifting filter coefficients so that final output remains the same. 20% hardware cost reduction is achieved when compared with standard architecture.

$$n_1 = T_n\ (m_1)$$
$$n_2 = T_n\ (m_2)$$
$$n_3 = T_n\ (m_3/m_1)$$

$$n_1 = T_n\ (^{m_4}/_{m_2})$$
$$\alpha' = T_n\ (^{\alpha}/_{m_1})$$
$$\beta' = T_n\ (^{\beta m_2}/_{m_1})$$
$$\gamma' = T_n\ (^{\gamma m_3}/_{m_2})$$
$$\delta' = T_n\ (^{\delta m_3}/_{m_2})$$

$$P_{2n+1} = X_{2n+1} + \alpha(X_{2n} + X_{2n+2})$$
$$Q_{2n} = X_{2n} + \beta(P_{2n-1} + X_{2n+1})$$
$$R_{2n+1} = P_{2n+1} + \gamma(Q_{2n} + Q_{2n+1})$$
$$S_{2n} = Q_{2n} + (R_{2n-1} + R_{2n+1})$$
$$Y_{2n+1} = KR_{2n+1} \qquad Y_{2n} = S_{2n}/K \tag{9}$$

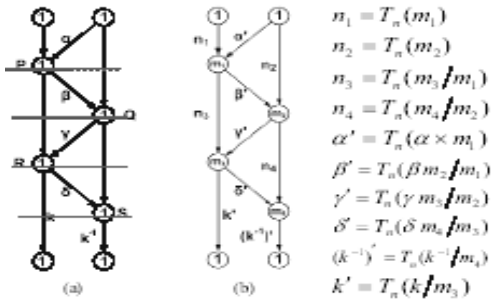


Fig.8 1-D lifting structure (a) standard structure (b) proposed

3. Conclusion

The various architectures discussed have brought insight into the scope of optimisations which is a walk on a tight rope to realise the constraints practically imposed by the end users. It is a trade-off between the parameters when area, speed and power are trimmed for higher efficiency. With newer technologies of device fabrication and architectures, applications can easily be made online in biometric field.

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