On the Design and Use of Wave Digital Structures

Karlheinz Ochs and Benno Stein

Paderborn University
Dept Mathematics and Computer Science
D – 33098 Paderborn

Report tr-ri-01-228
Series Computer Science
November 2001

Contents

1 Introduction

This paper is subjected to wave digital structures, short: WDS. The concepts of wave digital structures have their origins in the field of filter design, where they are designated more specifically as wave digital filters [Fettweis, 1971, 1986]. Generally speaking, wave digital structures can be viewed as a powerful modeling and analysis tool, which provides interesting properties.

The contributions of this paper include an introduction to wave digital structures as well as new aspects that relate to WDS theory and WDS operationalization; the paper is organized in the following five parts.

(1) Introduction (this section).

Aside from this overview the introduction presents a generic model abstraction hierarchy. The hierarchy then is used to classify both the models of this paper and the underlying model construction approaches.

(2) WDS as modeling tool (Section 2).

This section outlines the concept of WDS and its use for the modeling and analysis of electrical circuits. The special contribution of this section is that it develops a global algorithmic view to WDS with respect to modeling and simulation purposes. Moreover, special emphasis has been put on a plain but concise presentation of the underlying ideas in order to address both readers with and without background in classical network theory.

(3) Foundations of WDS (Section 3).

The first part of this section presents a succinct but complete modeling tool box for WDS. The second part discusses the special numerical advantages of WDS as well as their passivity properties.

(4) Design of WDS (Section 4).

WDS come along with interesting properties—their creation, however, is not a trivial task and usually is not taught in communications engineering. This section presents efficient algorithms for the automatic generation of an optimum WDS for a given electrical circuit.

(5) Numerics based on WDS (Section 5).

This section points out the relation between WDS and implicit integration methods. In particular it is shown, in which way WDS can be used to construct integration methods that provide a useful numerical property, which is called the “passivity property” here.

1.1 From a System to a Computer Model

The term “system” can be defined in different ways and with emphasis on different aspects. For our purposes, it is sufficient to consider a system as a spatio-temporally closed and logically interconnected unity [Kowalk, 1996, pg. 27]. A system is recursively built up from subsystems and relations. The relations divide into internal relations, which connect subsystems, and external relations, which connect subsystems and objects beyond the system boundary, that is, objects from the environment. Both subsystems and relations are characterized by attributes, called variables, which may change over time. Variables that are necessary to prescribe the system behavior are called states.

Variables that characterize external relations divide into input variables and output variables. Input variables are extraneous; they act from the environment on the system and modify the system’s states. Input variables and state variables determine the system’s output variables, which in turn affect the environment.

Creating a model of a technical system S means to shape its underlying concept or idea—a process that is first of all mental, and that always involves three major steps.

(1) Identification of the system's boundary.

(2) Identification of the subsystems and relations of $S \Rightarrow$ structure model.

(3) Characterization of constraints between the variables of the subsystems and relations $\Rightarrow$ behavior model.

The transformation of a mental model into a computer model usually happens within several steps, wherein intermediate models are constructed: a structure model, a behavior model, and an algorithmic model (see Figure 1, which shows a modified version of Wallaschek's presentation [Wallaschek, 1995]).

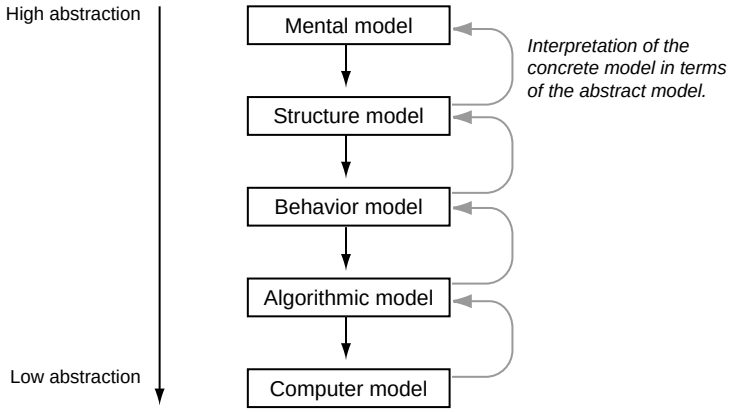

Figure 1: A hierarchy of models. Top-down model construction means to map abstract models onto less abstract models. Final objective is the operationalization of the mental model in the form of a computer program.

Typically, the human designer materializes his mental model as a textual or graphical structure model, for instance as a drawing or a diagram representation of the system S. The structure model, which defines subsystems and relations of S, becomes a behavior model of S by specifying a behavior prescription for each subsystem. Since behavior descriptions are often defined in a mathematical form, behavior models are also designated as mathematical models [Wallaschek, 1995, Kailath, 1980, Vidyasagar, 1993]. In the majority of cases the behavior model must be prepared with respect to the simulation algorithms employed. This step includes the introduction of a causal order for the behavior equations, the normalization of behavior equations, or other algebraic operations. The specification of an algorithmic model within a computer language or a simulation language like ACSL [Mitchell and Gauthier, 1976, Cellier, 1991] yields a computer model, say, a program.

1.2 The Models in this Paper

Structure Model Starting point for several analysis tasks is a structure model in the form of an electrical circuit. Here, the building blocks of an electrical circuit are voltage sources, current sources, resistances, capacitances, inductances, and diodes. An electrical circuit is usually defined graphically, in the form of a circuit diagram, and may be the result of very different modeling tasks:

- *Filter Design.* Filter design deals with the creation of (passive) electrical circuits, as they are used for signal processing in audio and video applications. Such circuits transform, say filter, a continuous-time input signal towards a specified continuous-time output signal.

- *Mechanical System Modeling.* Mechanical systems, as well as other non-electrical physical systems can be modeled as electrical circuits (see [Kumar, 1991, Paap et al., 1993] or [Meerkötter and Scholz, 1989, Meerkötter and Felderhoff, 1992, Fettweis, 1992]). By employing so-called electrical equivalent networks for the mechanical building blocks, one is able to construct an electrical set-up for the mechanical system. The simulation results then can be interpreted in terms of mechanical quantities.

- *Solving Differential Equations.* Electrical circuit analysis has shown success as a mathematical instrument. When given a set of complex (partial) differential equations, this problem specification can be transformed into a related electrical circuit. Like the construction of an equivalent network as described before, the rationale of such a transformation is based on the observation that a tailored circuit simulation algorithm may perform better than a general-purpose solution approach.

Behavior Model A behavior model of a structure model comprises local component descriptions as well as the continuity and the compatibility constraints, which define the connections of the components. In case of an electrical circuit, the component descriptions are given by the respective voltage/current (differential) equations, such as $v(t) = R \cdot i(t)$ (resistance), $di(t)/dt = 1/L \cdot v(t)$ (inductance), or $dv(t)/dt = 1/C \cdot i(t)$ (capacitance).

The continuity constraints are defined by Kirchhoff's current law, and the compatibility constraints are defined by Kirchhoff's voltage law.[1]

The overall objective is to analyze the behavior of a given electrical circuit. Clearly, by constructing the circuit as a real set-up of electronic components, its behavior could be determined by measuring all interesting signals. Typically this approach is not pursued but a circuit is "realized" in the form of a computer program: The program emulates the behavior of the circuit by running a virtual set-up. A prerequisite is the conversion of the continuous-time signal towards a digital signal, i. e., a sequence of numbers.

To go the outlined way, an *algorithmic model* must be constructed from the circuit's behavior model, and at this place several possibilities stand to reason: a model of node or loop equations, a state space model, or a wave digital structure (see Figure 2).

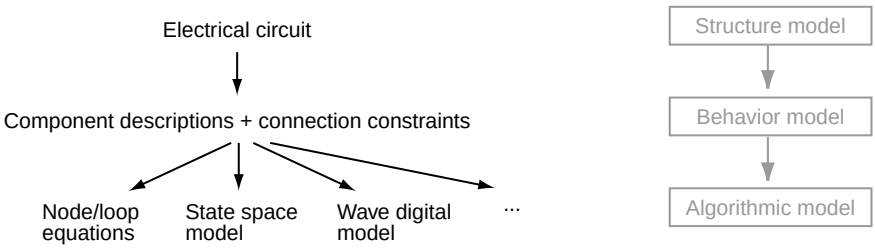

Figure 2: The electrical circuit defines a structure model of the interesting system which is to be transformed into an algorithmic model: a model of node or loop equations, a state space model, or a wave digital model.

Algorithmic Model The construction of an algorithmic model from a behavior model is often the hardest job of the entire model construction process. Note that within the behavior model the component constraints and the connection constraints are formulated locally; however, *processing* these constraints means to find a globally consistent solution. This happens by reformulating the

[1] Primarily, the concepts of electrical continuity and compatibility reflect a single-port viewpoint (see Subsection 2.2, pg. 6). They may not be applied to particular multport elements like the girator (see Subsection 3.1.2, pg. 16).

local constraints into some kind of normal form, which then is used by special algorithms to compute a globally consistent solution [Cellier, 1991]:

- *Node/Loop Equations.* These commonly used algorithmic models are based on a special selection of node equations and loop equations respectively. Before these equations can be set up, the electrical circuit must eventually be prepared in order to fulfill certain consistency conditions (conversion of voltage sources or independent current sources, etc.). If all sources operate with the same frequency, the computation of the stationary quantities involves only algebraic operations.

  It is advisable then to describe the equations in a normalized matrix form using complex terms [Fettweis and Hemetsberger, 1995]. Note that the processing of these normal forms requires the symbolic inversion of polynomial matrices.

- *State Space Model.* The previously mentioned cutset potential method or loop current method are appropriate for a stationary investigation of the electrical circuit, where all signal sources operate at the same frequency ω. To investigate the circuit for arbitrary signals in the time-domain, setting up a state space model may provide a useful approach [Kailath, 1980]. The model is of the following normal form: $\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t)$, $\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t)$.

  $\mathbf{x}(t)$, $\mathbf{u}(t)$, and $\mathbf{y}(t)$ denote the state vector, the input vector, and the output vector; $\mathbf{A}, \mathbf{B}, \mathbf{C}$, and $\mathbf{D}$ denote the system matrix, the input matrix, the output matrix, and the straight-way matrix. Additionally, a system of algebraic equations may be given.

  In the general case, the processing of normal forms requires the solution of a nonlinear differential-algebraic system (DAE) [Petzold, 1994, Vidyasagar, 1993]. Note however, that structural singularities in the electrical circuit may render the construction of a state space model difficult, if not impossible.

- *Wave Digital Structure.* Wave digital structures (WDS) differ within two points from the algorithmic models mentioned before:

  (1) The v/i (voltage/current) domain is mapped onto the a/b-wave domain.

  (2) The connection constraints are treated explicitly: The Kirchhoff interconnecting network is partitioned according to series and parallel connections.

  Wave digital structures establish models in the discrete time domain; they can be used to describe both linear and nonlinear systems. Due to their numerical properties wave digital structures are specially tailored with respect to a hardware implementation. The next section shows how WDS are constructed.

2 Introduction to Modeling with Wave Digital Structures

Wave digital structures (WDS) are a means for modeling and analysis. Targeted especially on readers with less background knowledge in classical network theory or signal theory, this section introduces the underlying ideas. Readers who are familiar with wave digital structures may skip this section.

2.1 Road Map

Given is an electrical circuit, S; it is assumed that this circuit is passive and that it consists only of voltage and current sources, resistances, capacitances, inductivities, ... From such a circuit an algorithmic model in the form of a wave digital structure can be created, which is a rather complex reformulation where several constraints are to be met. The reformulation involves the following principal steps:

(1) Topological analysis of S with respect to subcircuits that are connected in series or in parallel to each other, and reformulation of S using special series and parallel connectors.

(2) Transfer of the component descriptions from the v/i domain to the a/b-wave domain.

(3) Discretization of the continuous signals by numerically approximating the differential equations.

(4) Transfer from the time domain to the frequency domain and replacement of the complex frequency variable p by the equivalent complex frequency variable ψ.

Remarks. The above reformulation steps divide into local operations (Step 2-4), which act on the components of the electrical circuit in an isolated manner, and into the global topology reformulation in Step 1.
From a syntactical point of view, the entire reformulation of an electrical circuit into a wave digital structure is accomplished within in the steps 1-3. Also note that Step 2 and Step 3 are orthogonal to each other; i. e., their order of application can be interchanged. Step 4 is essential though: It provides insight into the passivity property of the circuit.

In a nutshell, a wave digital structure is a particular kind of signal flow graph. Its topology is constructed by means of series and parallel connectors; the signals that are processed when traveling along the signal flow graph are wave quantities. Figure 3 illustrates the principal reformulation steps from an electrical circuit to a WDS.

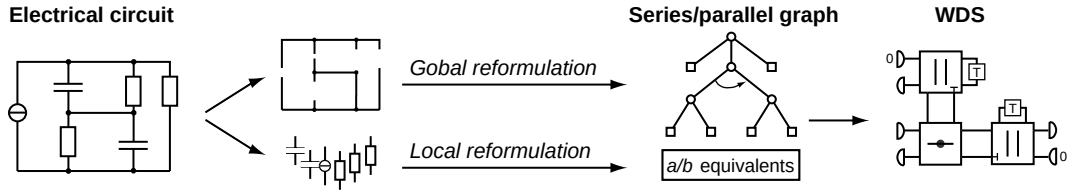

Figure 3: From an electrical circuit to a WDS; the principal reformulation steps.

In the following subsections, examples to each of the above reformulation steps will be presented and the rationale will be discussed.

2.2 Topology Reformulation

An electrical circuit, S, consists of a set of components, which are connected by a so-called Kirchhoff interconnecting network. A reformulation of a Kirchhoff network here means the identification of subcircuits in S that are either connected in series or in parallel to each other.

Port Condition

Both series connections and parallel connections are specializations of a concept called *port*, as much as each component with two terminals establishes a (single) port as well. A port fulfills the *port condition*, which claims that the currents at terminal 1 and terminal 2, i_1 and i_2, fulfill the constraint $i_1 = -i_2$ at any instant (see Figure 4).

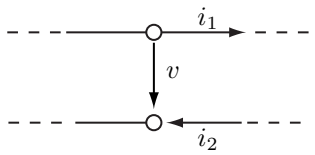

Figure 4: The port condition claims that $i_1 = -i_2$ holds.

Note that any series and parallel combination of ports again yields a port. This observation suggests a bottom-up approach for the identification and synthesis of ports, resulting in a single top-level port for the entire interconnecting network. As a consequence, the interconnecting network can be expressed in a new form, where particular construction elements—the series and parallel connectors—are used to connect the respective building blocks in S. Such a representation of the Kirchhoff interconnecting network could be called port structure of S.

Global vs. Local Computations

The replacement of the original interconnecting network by a port structure that employs only series and parallel connections leads to a special network analysis approach. Common network analysis approaches are based on mesh equations, node equations, or state equations [Fettweis and Hemetsberger, 1995, Cellier, 1991, Unbehauen, 1994]. Following a common approach means to set up and transform matrices, in a way the mesh-incidence matrix, the branch-impedance matrix, the node-incidence matrix, the branch-admittance matrix, or the state space matrix.

Computations on matrices are *global* computations in the sense that a system of equations must be treated at the same time to find the equations' solutions. By contrast, a computation will be called *local*, if a single equation at a time is sufficient to compute a solution of that equation, and if this solution is coded explicitly in the equation. See [Schulz et al., 2001] for an in-depth discussion of different behavior model types and locality.

Signal Flow Graph

If the topology of a circuit is realized solely by means of series and parallel connections, the model processing effort for this circuit can decisively be decreased: Due to the special topology, computational effort can be made up front—during model construction time—resulting in a new behavior model whose equations can be processed locally. Note that a behavior model whose equations can be processed locally establishes a *feedback-free signal flow graph*. A feedback-free signal flow graph is a processing prescription that defines the computation on signals in a definite order while employing only explicit computation rules. A feedback-free signal flow graph thus establishes an algorithmic model that can be processed easily on a computer.

The following example illustrates the idea behind the topology reformulation. Given is the electrical circuit shown in Figure 5. Here, the voltage e forms the input, the currents i_1, i_2, i_3, and the voltages v_1 and v_2 are to be determined, R_1, R_2, and R_3 are given. To handle the generic case, a global network analysis approach is necessary, where all node equations, mesh equations, and component equations are treated within a global equation system.

In the example, the global investigation is inevitable to compute the total resistance (impedance in the complex analysis) of the series-parallel connection, from which in turn i_1 and the voltages v_1, v_2, and v_3 can be computed. The underlying equations of the circuit, say, its mathematical model,

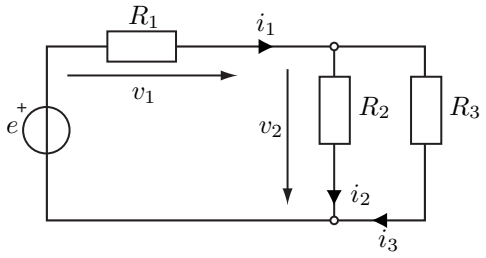

Figure 5: Electrical circuit with three resistances.

are the following.

$$\sum_{\nu=1}^{3} v_\nu = 0, \quad v_3 = e, \quad i_1 = i_2 + i_3, \quad \begin{pmatrix} v_1 \\ v_2 \\ v_2 \end{pmatrix} = \begin{pmatrix} R_1 & 0 & 0 \\ 0 & R_2 & 0 \\ 0 & 0 & R_3 \end{pmatrix} \begin{pmatrix} i_1 \\ i_2 \\ i_3 \end{pmatrix}$$

The signal flow graph depicted on the left-hand side of Figure 6 shows a graphical representation of the mathematical model. Note that this graph establishes no algorithmic model: It contains a loop and hence defines no causal ordering amongst the quantities. If we had computed in advance the total resistance of the network, all quantities could be computed *locally*. As a consequence, the computations can be formulated by means of a feedback-free signal flow graph, as shown in the same figure on the right. This graph defines an algorithmic model for the above circuit.

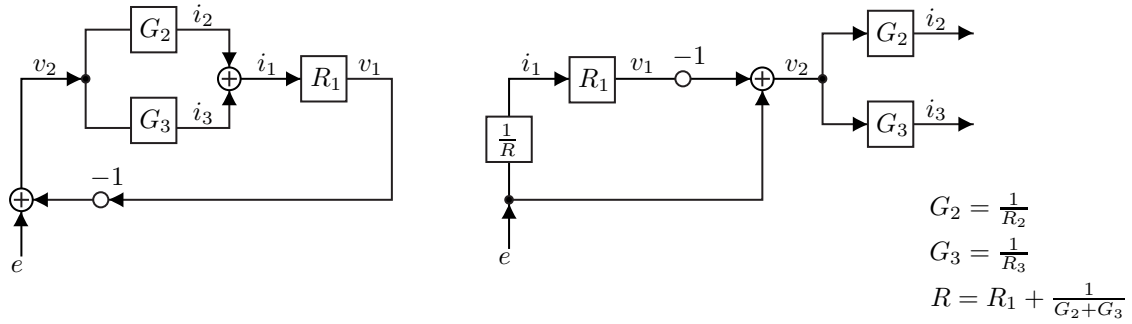

Figure 6: Two signal flow graphs of the above electrical circuit. The left one contains a feedback loop, the right one is feedback-free.

Algebraic Loop

Recall that a feedback-free signal flow graph can only be constructed for an equation system, if all subsets of depending equations, the so-called algebraic loops, have been *serialized* or "broken open". It is no sheer coincidence that ports can be transformed towards a signal flow graph in a straightforward way: The resistances and conductances of ports can be combined to a total value. In the example, the serialization became possible after having computed the total resistance of the network; of course, in case of mono-frequent excitations, this can be extended to impedances and admittances as well.

Series and Parallel Connectors

In fact, if we restrict ourselves to circuit topologies that are composed of series and parallel connections only, the construction of the related feedback-free signal flow graphs can be performed canonically. As mentioned above, it is useful to introduce two auxiliary building blocks for this purposes, a series connector and a parallel connector, which will guarantee that Kirchhoff's laws are obeyed. Figure 7 shows a connector realization of the electrical circuit example from Figure 5.

In this context the series and parallel connectors carry out the computation of the total impedance or admittance of the connected components. This computation is encoded within the connector

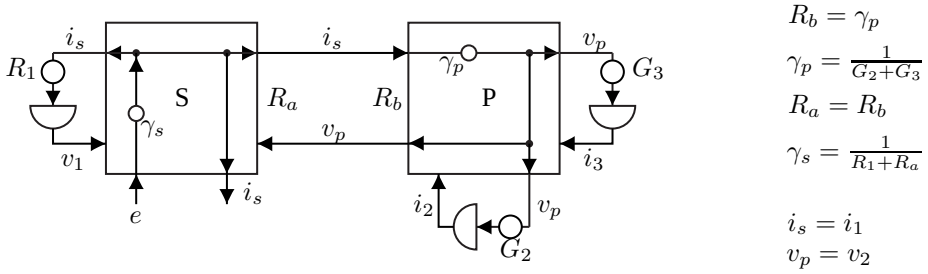

Figure 7: A possible connector realization of the electrical circuit.

coefficients γ_s, γ_p and the port unification constraint: When attaching two connectors, it must be guaranteed that the port resistances of the adjacent ports are identified (see the condition $R_a = R_b$ in Figure 7). Observe that series and parallel connections with more than two elements can be realized by attaching several connectors of the respective type.

Explicit Methods

If the electrical circuit contains reactive elements, the local propagation property of the signal flow graph is hold up if an explicit integration rule is employed for the approximation of differential relationships. Taking a capacity, for instance, the behavior for continuous-time and its approximation by the explicit Euler rule is given with the equations

$$v(t_k) = v(t_{k-1}) \; + \; \frac{1}{C}\int_{t_{k-1}}^{t_k} i(\tau)d\tau \quad \text{and} \quad v_k := v_{k-1} \; + \; \frac{T}{C} i_{k-1},$$

where $v(t_{k-1})$ denotes the known voltage at t_{k-1} with $t_k := t_0 + kT, k \in \mathbf{N}$, while v_{k-1} and i_{k-1} denote the approximate values for the exact values $v(t_{k-1})$ and $i(t_{k-1})$ respectively.

Figure 8 shows for the parallel connection of a resistance and a capacitance an algorithmic model in the form of a parallel connector, which employs the explicit Euler rule.

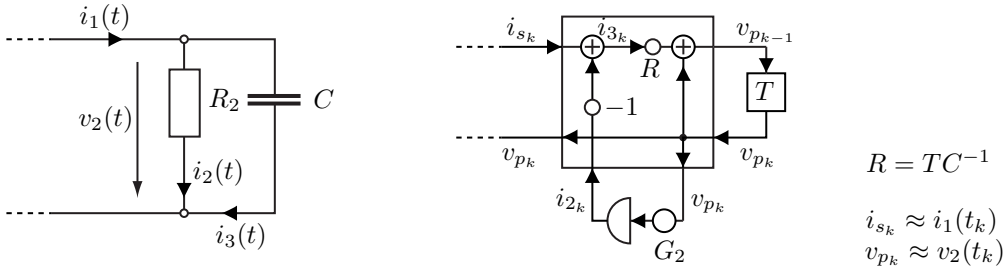

Figure 8: A possible connector realization of a resistance with a parallel capacitance.

Note that the use of an *implicit* integration method entails decisive numerical advantages but is bought with the lost of the local computability of the above signal flow graph.—At this place we anticipate an issue of the next subsection: When the electrical quantities are expressed by wave quantities, the application of an explicit method to this reformulated model yields an implicit integration in the original electrical formulation.

Remarks. (1) Connectors for Kirchhoff networks can be constructed in other ways than depicted in Figure 7 or Figure 8. (2) Connectors for wave digital structures model the connection constraints in the a/b-wave domain, and consequently they must have a different set up than the connectors shown here. Note, however, that the underlying idea is the same: The prescription of a local computation rule for the global behavior of a series-parallel structure by means of a smart computation of the elements' port resistances. Again, this computation is encoded within the connector coefficients and the port unification constraint.

2.3 Transfer to the a/b-Wave Domain and Discretization

The electrical quantities voltage, v, and current, i, can be expressed in terms of other quantities, e. g. by so-called wave quantities, a, b, which are linear combinations of v and i. The transformation pursued here is defined as follows.

$$a = v + Ri \qquad b = v - Ri \tag{2.1}$$

Voltage Waves

The wave quantities defined in the equations (2.1) are called voltage waves, where a and b represent the incident and reflected wave respectively. R is called *port resistance*; R must be positive, but apart from that its value can be chosen arbitrarily for each port. In practice, one will select that particular value of R which leads to the simplest overall expressions for the problem at hand [Fettweis, 1986, p. 273].

In the following we discuss the transfer from the v/i-domain to the a/b-domain at a reactive element, the capacitance. Starting point is the following differential relationship between the current and the voltage at a capacitance, where $v(t_{k-1})$ designates the known voltage at t_{k-1}.

$$v(t_k) = v(t_{k-1}) \; + \; \frac{1}{C} \int_{t_{k-1}}^{t_k} i(\tau) d\tau, \quad \text{where } t_k := t_0 + kT, k \in \mathbf{N} \tag{2.2}$$

Equation (2.2) must be translated into the discrete-time domain. In this place, the integral is approximated by means of the trapezoid rule, for reasons that will be discussed later on and especially in Section 5:

$$v(t_k) \approx v_k := v_{k-1} \; + \; \frac{T}{2C}\big(i_k + i_{k-1}\big), \tag{2.3}$$

where v_{k-1}, i_k, and i_{k-1} denote the approximate values for the respective exact values $v(t_{k-1})$, $i(t_k)$, and $i(t_{k-1})$.

Equation (2.3) can be translated to the a/b-wave domain, for instance by using the identities (2.4), which follow from the equations (2.1).

$$v = \frac{a+b}{2} \qquad i = \frac{a-b}{2R} \tag{2.4}$$

However, because of the special (and simple) form of the trapezoid rule, equation (2.3) can be directly expressed in terms of a and b, since from equation (2.3) follows:

$$v_k - Ri_k = v_{k-1} + Ri_{k-1} \tag{2.5}$$

$$\Leftrightarrow \qquad b_k = a_{k-1}, \qquad \text{with } R := \frac{T}{2C} \tag{2.6}$$

Choosing R as port resistance for a capacitance obviously leads to the simplest overall expression. Figure 9 shows the capacitance in the v/i-time domain and the related wave flow diagram.

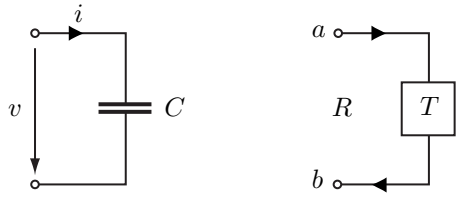

Figure 9: Capacitance and related wave flow diagram with $R = \frac{T}{2C}$.

Remarks. Equation (2.5) shows that a reformulation of the electrical quantities in terms of wave quantities is bound up with the fact that an implicit integration in v and i by means of the trapezoid method becomes explicit in a and b. Note that this powerful concept, the combination of an integration method's stability properties with a simplified numerical representation, can be generalized towards other integration methods. Section 5 dwells upon that subject.

2.4 Combining Topology Reformulation and Transfer to the a/b-Wave Domain

In this subsection we consider the circuit shown in Figure 10 and apply the outlined reformulation steps at once: The modeling of the connection constraints by means of connectors and the transfer of the electrical quantities into the a/b-wave domain.

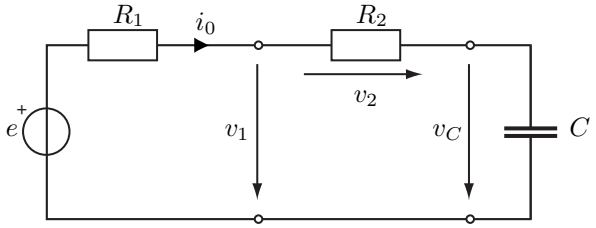

Figure 10: Electrical circuit with two resistances and a capacity.

Adaptors

The connectors in the a/b-wave domain get a special name—they are called series adaptor and parallel adaptor respectively. The circuit in Figure 10 establishes a series connection, and consequently, we will exemplary derive the determing equations for a series adaptor. Figure 11 contrasts a generic electrical series connection with voltage drops v_ν and currents i_ν (left-hand side) with the related series adaptor, where the port resistances R_ν, $\nu = 1, \ldots, 3$, indicate the port resistances of the electrical components' wave digital counterparts (right-hand side).

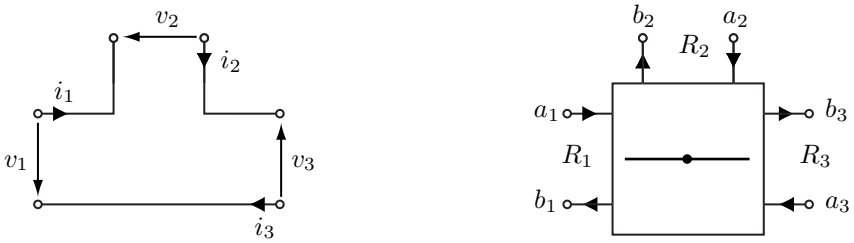

Figure 11: Electrical series connection with three elements (left) and symbol of the series adaptor with three ports (right).

Each of the three electric components can be characterized in the the a/b-wave domain, using the voltage wave transformation introduced by Equation (2.1), Page 10.

$$a_\nu = v_\nu + R_\nu i_\nu \qquad b_\nu = v_\nu - R_\nu i_\nu, \quad \nu = 1, \ldots, 3$$

To write these equations in vector form, we define the port resistance matrix $\mathbf{R}$ and the port conductance matrix $\mathbf{G} := \mathbf{R}^{-1}$.

$$\left.\begin{array}{rcl} \mathbf{a} &=& \mathbf{v} + \mathbf{R}\mathbf{i} \\ \mathbf{b} &=& \mathbf{v} - \mathbf{R}\mathbf{i} \end{array}\right\} \quad \Leftrightarrow \quad \left\{\begin{array}{rcl} \mathbf{v} &=& \dfrac{\mathbf{a}+\mathbf{b}}{2} \\ \mathbf{i} &=& \mathbf{G}\dfrac{\mathbf{a}-\mathbf{b}}{2} \end{array}\right. , \qquad \mathbf{R} := \begin{pmatrix} R_1 & 0 & 0 \\ 0 & R_2 & 0 \\ 0 & 0 & R_3 \end{pmatrix} \tag{2.7}$$

Using Kirchhoff's current law for series connections, $i_1 = i_2 = i_3 = i_0$, the equations (2.7) can be transformed as follows.

$$\left.\begin{array}{rcl} \mathbf{a} & = & \mathbf{v} + \mathbf{R}\mathbf{i} \\ \mathbf{b} & = & \mathbf{v} - \mathbf{R}\mathbf{i} \end{array}\right\} \quad \Rightarrow \quad \mathbf{b} = \mathbf{a} - 2\mathbf{R}\mathbf{i} \;=\; \mathbf{a} - 2\mathbf{R}\mathbf{e}i_0, \quad \mathbf{e} := (1,1,1)^T \tag{2.8}$$

Using Kirchhoff's voltage law for series connections, $\sum_{\nu=1}^{3} v_\nu = 0$, equation (2.8) for $\mathbf{a}$ can be transformed, resolved for i_0 and put into the equation for $\mathbf{b}$.

$$\begin{array}{rcl} \mathbf{a} & = & \mathbf{v} + \mathbf{R}\mathbf{e}i_0 \\ \mathbf{e}^T\mathbf{a} & = & \mathbf{e}^T\mathbf{v} + \mathbf{e}^T\mathbf{R}\mathbf{e}i_0 \\ \frac{\mathbf{e}^T\mathbf{a}}{\mathbf{e}^T\mathbf{R}\mathbf{e}} & = & i_0, \quad \text{since } \mathbf{e}^T\mathbf{v} = \sum_{\nu=1}^{3} v_\nu = 0 \\ \mathbf{b} & = & (\mathbf{1} - 2\frac{\mathbf{R}\mathbf{e}}{\mathbf{e}^T\mathbf{R}\mathbf{e}}\mathbf{e}^T)\mathbf{a} \;=\; \mathbf{S}\mathbf{a} \end{array}$$

Adaptor Coefficients

The vector $\gamma := 2\frac{\mathbf{R}\mathbf{e}}{\mathbf{e}^T\mathbf{R}\mathbf{e}}$ is called the vector of adaptor coefficients, and the general form of an element γ_ν is

$$\gamma_\nu = \frac{2R_\nu}{R_1 + R_2 + R_3}, \quad \nu = 1,2,3.$$

If we make use of the relation $\mathbf{e}^T\gamma = \gamma_1 + \gamma_2 + \gamma_3 = 2$ between the γ_ν, the mapping $\mathbf{S}$ between $\mathbf{b}$ and $\mathbf{a}$ can be written as follows.

$$\mathbf{b} = \mathbf{S}\mathbf{a}, \;\; \mathbf{S} = \begin{pmatrix} 1-\gamma_1 & -\gamma_1 & -\gamma_1 \\ -\gamma_2 & 1-\gamma_2 & -\gamma_2 \\ \gamma_1+\gamma_2-2 & \gamma_1+\gamma_2-2 & \gamma_1+\gamma_2-1 \end{pmatrix}$$

Figure 12 shows the symbol for the series adaptor defined by S and the related signal flow graph, which encodes the equation system $\mathbf{b} = \mathbf{S}\mathbf{a}$.

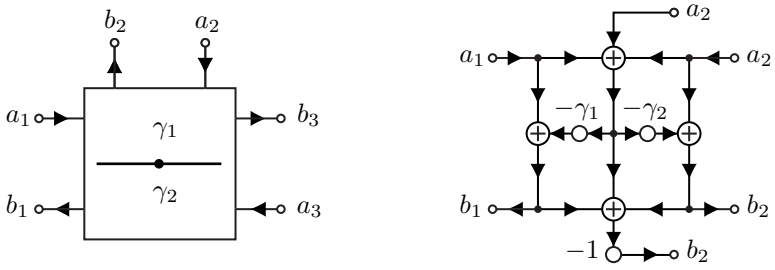

Figure 12: Symbol and signal flow graph of a series adaptor.

Also the component equations are transfered into the a/b-domain. For the capacitance this has already be shown on Page 10, for the resistance and the resistive voltage source the respective equations are derived now. We start by resolving the equations for a and b towards v and i.

$$\left.\begin{array}{rcl} a & = & v + Ri \\ b & = & v - Ri \end{array}\right\} \quad \Leftrightarrow \quad \left\{\begin{array}{rcl} v & = & \dfrac{a+b}{2} \\ i & = & \dfrac{a-b}{2R} \end{array}\right.$$

Replacing v and i in the resistance equation $v = R_0 \cdot i$ yields the following dependency between the incident wave, a, and the reflected wave, b.

$$\frac{a+b}{2} = R_0\frac{a-b}{2R} \quad \Leftrightarrow \quad b = \frac{R_0 - R}{R_0 + R}a$$

Setting the port resistance R to R_0, as declared above, a can be chosen arbitrarily and $b = 0$. The wave signal flow graph on the right-hand side of Figure 13 models this connection: a vanishes in a sink, and b is realized by a source with zero output.

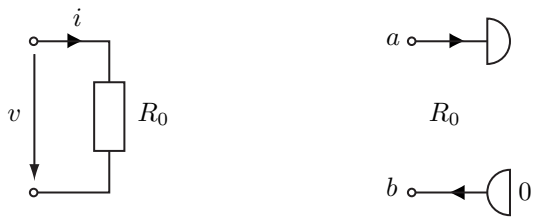

Figure 13: Resistance and the related wave flow diagram.

For the component equation of the resistive voltage source, $v = e + R_0 \cdot i$, the substitution yields the dependency $a = e$, if R_0 is chosen as port resistance. Figure 14 illustrates this connection.

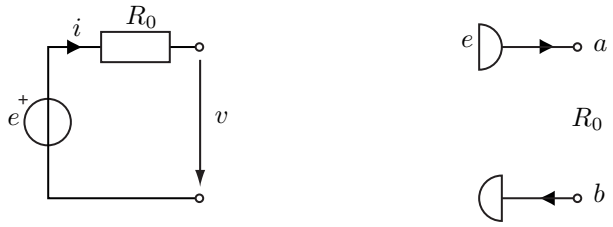

Figure 14: Resistive voltage source and the related wave flow diagram.

Finally, the series adaptor and the components' signal flow graphs can be composed to the entire signal flow graph, say, wave digital structure, as depicted in Figure 15. This signal flow graph represents an algorithmic model for the electrical circuit of Figure 10. The signal e forms the input from which all unknown wave quantities can be computed in a local fashion. The desired output values for i_0, v_1, v_2, and v_C are obtained by evaluating the equations (2.7).

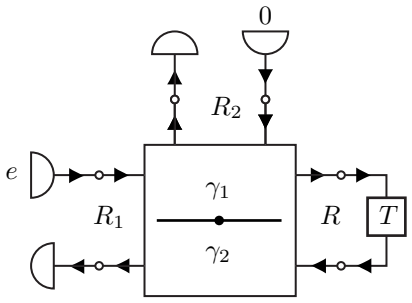

Figure 15: Wave digital structure of the electrical circuit from Figure 10 with $R_C = \frac{T}{2C}$.

2.5 Transfer from the Time Domain to the Frequency Domain

The transformation step described in this subsection is not directly necessary for the construction of a wave digital structure, but it provides insights respecting the stability behavior of the constructed WDS. Starting point is equation (2.3), Page 10; it approximates the differential relationship between

the current and the voltage at a capacitance by means of the trapezoid rule and reads as follows:

$$v_k := R\big(i_k + i_{k-1}\big) \;+\; v_{k-1}$$

with

$$R := \frac{T}{2C}.$$

By restricting ourselves to complex-valued signals of the form Xe^{pt}, the above equation obtains the following form:

$$v_k = \text{Re}\, V e^{pt_k}, \qquad i_k = \text{Re}\, I e^{pt_k}$$

$$V e^{pt_k} = RI e^{pt_k} + RI e^{pt_{k-1}} + V e^{pt_{k-1}} \tag{2.9}$$

V and I denote complex amplitudes, p denotes the complex frequency. A multiplication by e^{-pt_k} along with a rearrangement yields:

$$V = \frac{1 + e^{-pT}}{1 - e^{-pT}}\, R\, I \;=\; \frac{1}{\tanh \frac{pT}{2}}\, R\, I. \tag{2.10}$$

Rewriting equation (2.10) in terms of the equivalent complex frequency ψ yields:

$$V = \frac{R}{\psi} I \quad \Leftrightarrow \quad I = \frac{\psi}{R} V, \qquad \text{with } \psi := \tanh \frac{pT}{2} \tag{2.11}$$

Figure 16 comprises the different models (views) of the characteristic impedance of a capacitance that have been derived so far.

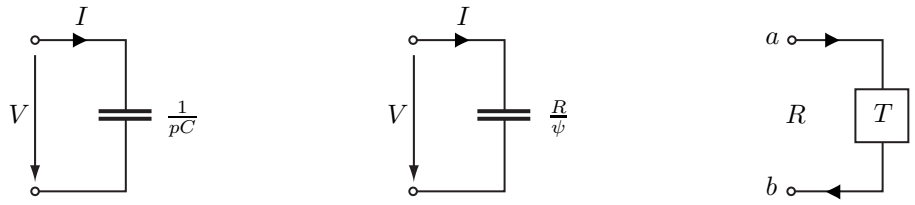

Figure 16: Three models of the capacitance. From left to right: continuous-time, discrete-time with trapezoid rule employed as integration method, and wave flow diagram.

Passivity of Models

Equation (2.11) states something about the passivity of equation (2.3). We start with the following definition of an electrical circuit's effective power P.

$$P = \text{Re}\, I^* V$$

For reactive elements, the power P is a function of the frequency, and a linear, time-invariant system S is called passive if it fulfills the following implication.

$$\text{Re}\, \psi > 0 \quad \Rightarrow \quad P(\psi) \geq 0 \tag{2.12}$$

We use this implication to verify the passivity of the capacity.

$$P(\psi) = \text{Re}\, I^* V \;=\; \text{Re}\, \psi^* \, \frac{|V|^2}{R} \;=\; \frac{|V|^2}{R} \text{Re}\, \psi \;>\; 0$$

Obviously does the algorithmic model of a capacitance conserve passivity, since for each capacitance element holds $C > 0$.

Remarks. Remind of the fact that the algorithmic model of the capacity, its wave flow diagram in Figure 16, encodes a particular integration method. I. e., if we know something about this algorithmic model, we know immediately something about the applied integration method—the trapezoid rule in our case. To become specific, the numerical properties of the algorithmic model are the same as of the integration method.

The interesting aspect is the following. If we have an interpretation of the algorithmic model as a circuit, numerical properties can be directly be read off this circuit. E. g., for the algorithmic model of the capacitance it was simple to determine its passivity by checking the compliance of this model with implication (2.12). In other words, it could be proven that the chosen integration method conserves the passivity property of the capacity.

Though it is of a local nature, this passivity analysis can be applied easily to all wave digital structures that model a linear, time-invariant system S: If each element of the wave digital structure fulfills inequation (2.12), and if the wave digital structure emerges from a port-wise connection of these elements, then it does reproduce the passivity property of the system S during simulation [Fettweis, 1971].

Section 5 picks up this thread and extends it to nonlinear systems. In this regard, the concept of a circuit's characteristic impedance is introduced and used as a tool for passivity analysis [Ochs, 2001]. Moreover, the interpretation of the algorithmic model—that results from applying an integration method—as a circuit is used to construct new integration methods. The guiding idea keeps the same as above: Numerical properties of the integration method are deduced from circuit properties.

3 Wave Digital Structures Reviewed

3.1 Synthesis of Wave Digital Structures

This section recapitulates wave digital structures, whose basic theory has been developed by Fettweis, [Fettweis, 1971]. The starting point for the synthesis of wave digital structures, is an electrical circuit whose electrical components are divided into sources and elements. For now, only linear elements are considered while the modeling of nonlinear elements can be found in [Meerkötter and Scholz, 1989, Meerkötter and Felderhoff, 1992]. All linear elements are assumed to be passive n-ports, and their interconnections obey KIRCHHOFF's law, i. e., we restrict ourselves to structural passive electrical circuits. To each port of the circuit we assign a so-called port resistance being a positive constant.

The first step for the synthesis of the related wave digital structure is the description of the electrical behavior of the components in the wave digital domain. For this purpose, we distinguish between sources, nonreactive elements, reactive elements and the remaining interconnecting network.

3.1.1 Sources

Sources of the electrical circuit can be divided into ideal current and ideal voltage sources, cf. Figure 17, which are described by

$$v = e \quad \Longleftrightarrow \quad a = 2e - b \tag{3.1}$$

$$\text{and} \quad i = j \quad \Longleftrightarrow \quad a = 2Rj + b \tag{3.2}$$

respectively. From these equations it is clear that these electrical sources do not lead to pure wave sources but to combinations of a and b.

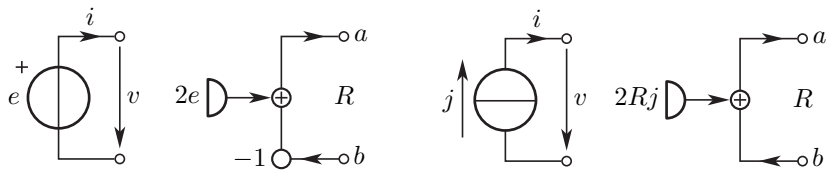

Figure 17: Ideal voltage and current source

Naturally, ideal sources never occur in electrical circuits. In fact, we have to deal with many physical phenomena but for most practical problems the major effect can be taken into consideration if each ideal source is connected to an additional resistor. Due to HELMHOLTZ's theorem, such a resistive current source is always equivalent to a resistive voltage source so that it is sufficient to consider a resistive voltage source only:

$$v = e - Ri \quad \Longleftrightarrow \quad a = e. \tag{3.3}$$

Here, the port resistance has been chosen equal to R, whereas the port resistance of an ideal source can be chosen arbitrarily. As a result, both types of resistive sources correspond to wave sources.

3.1.2 Nonreactive Elements

The simplest example of a nonreactive element is a resistor which can be derived from the resistive voltage source if the trivial case $e = 0$ is considered. It is described by

$$v = Ri \quad \Longleftrightarrow \quad b = 0 \tag{3.4}$$

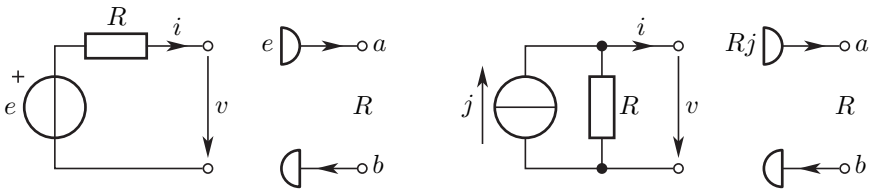

Figure 18: Resistive voltage and current source

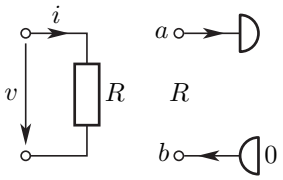

Figure 19: Resistor

when the port resistance is equal to the value of the resistance itself.

Beside the resistor there exists a variety of nonreactive elements, i. e., of elements which cannot store energy. The most important elements are the gyrator, the circulator, and the ideal transformer each of which is lossless. Such nonreactive and lossless elements are also called nonenergetic.

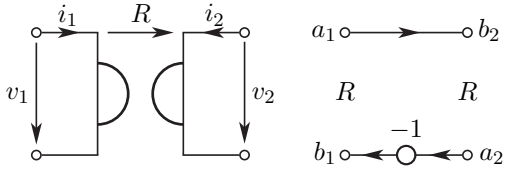

Figure 20: Gyrator

If both port resistances of the gyrator are equal to the gyration resistance this yields wave digital flow diagrams with no directed path between the terminals of each port and the realization becomes very simple, cf. Figure 20. A similar result is achieved for the circulator if all of its port resistances are equal to the circulation resistance, cf. Figure 21. The corresponding equations for the gyrator,

$$\left.\begin{array}{l} v_1 = -Ri_2 \\ v_2 = Ri_1 \end{array}\right\} \quad \Longleftrightarrow \quad \left\{\begin{array}{l} b_1 = -a_2 \\ b_2 = a_1, \end{array}\right. \tag{3.5}$$

and the 3-port-circulator,

$$\left.\begin{array}{l} v_2 - v_3 = Ri_1 \\ v_3 - v_1 = Ri_2 \\ v_1 - v_2 = Ri_3 \end{array}\right\} \quad \Longleftrightarrow \quad \left\{\begin{array}{l} b_2 = a_1 \\ b_3 = a_2 \\ b_1 = a_3, \end{array}\right. \tag{3.6}$$

show that they are closely related. As a consequence, it is always possible to describe a gyrator via a circulator and vice versa.

The ideal transformer with turns ratio n is described by

$$\left.\begin{array}{l} v_2 = nv_1 \\ i_1 = -ni_2 \end{array}\right\} \quad \Longleftrightarrow \quad \left\{\begin{array}{l} b_1 = \dfrac{1}{n}a_2 \\ b_2 = na_1, \end{array}\right. \tag{3.7}$$

if the port resistances fulfill the relationship $R_2 = n^2 R_1$. In contrast to the gyrator and the circulator, the ideal transformer does not relate voltages with currents. For this reason, ideal transformers play an important role for generalized interconnecting networks.

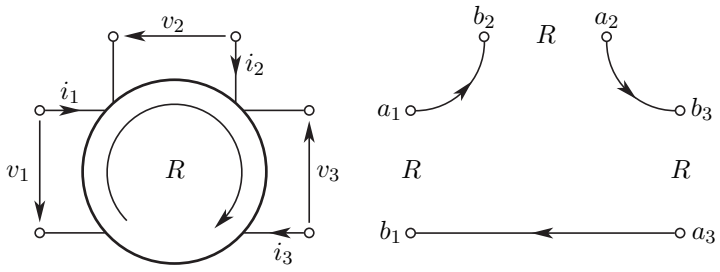

Figure 21: 3-port-circulator

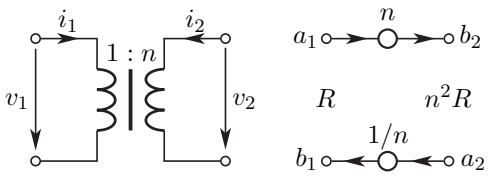

Figure 22: Ideal transformer

3.1.3 Reactive Elements

In contrast to sources and nonreactive elements, whose voltage and current relations are of pure algebraic type, reactive elements are additionally described by differential equations. Since we can only approximate an integration of these differential equations on a computer system, there is a need to introduce a method which approximates the exact solution.

Instead of using the differential equations directly, the steady state equations of the linear electrical components are used in wave digital filter theory. For this, the complex frequency variable p is replaced by the equivalent complex frequency variable, ψ,

$$\psi := \tanh(pT/2) = \frac{z-1}{z+1}, \quad z := e^{pT}, \tag{3.8}$$

where T denotes the sampling period. This transformation maps the left half plane of p onto the left and the right half plane of ψ. As a consequence, the stability properties of the discrete-time n-ports are the same as those they were derived from.

Applying this tangent hyperbolic transformation to the steady-state equations of a capacitance C and an inductance L we get the following equations

$$V = \frac{R_C}{\psi} I \quad \Longleftrightarrow \quad b(k) = a(k-1) \tag{3.9}$$

$$\text{and} \quad V = R_L \psi I \quad \Longleftrightarrow \quad b(k) = -a(k-1) \tag{3.10}$$

where the port resistances $R_C = T/(2C)$ and $R_L = 2L/T$ has been chosen. The resulting wave flow diagrams are shown in Figure 23 and they differ by a sign inversion only. This is because an inductance can always be represented by a gyrator and a capacitance, cf. Figures 20 and 23.

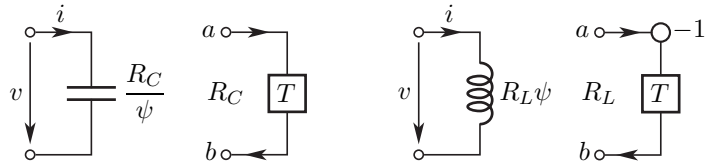

Figure 23: Capacitance and Inductance

In addition to the capacitance and inductance, unit elements are often used in wave digital structures.

3.1.4 Adaptors

Beside the electrical components we have to transfer the voltage and current relations of the interconnecting network to the wave digital domain. In many technical applications, e. g. digital filters, these topological constraints define parallel and series connections, cf. Figure 24. The corresponding equivalences in wave digital domain are the so-called parallel and series adaptors respectively, which are basic types of adaptors.

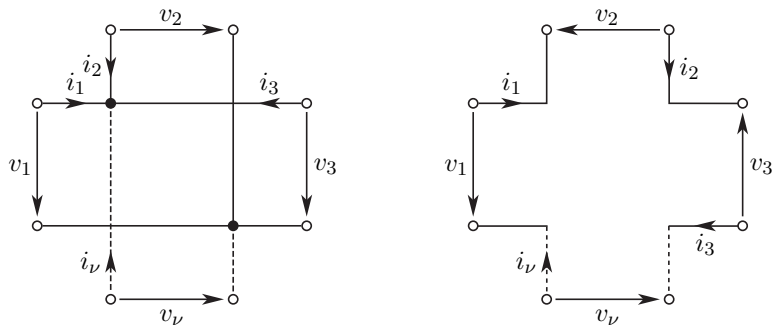

Figure 24: Parallel- and series connection

The electrical equations for the parallel connection of Figure 24 are

$$\boldsymbol{e}^{\mathrm{T}}\boldsymbol{i} = 0 \quad \text{and} \quad \boldsymbol{v} = \boldsymbol{e}v_0, \tag{3.11}$$

where all voltages, v_ν, and currents i_ν, are collected in $\boldsymbol{v}$ and $\boldsymbol{i}$, and where vector $\boldsymbol{e}$ is of proper dimension with every element equal to one.

After introducing voltage wave vectors $\boldsymbol{a}$ and $\boldsymbol{b}$ with the port conductance matrix $\boldsymbol{G} := \mathrm{diag}(G_\nu)$ one can find the scattering matrix of a n-port parallel adaptor

$$\boldsymbol{b} = (\boldsymbol{e}\gamma^{\mathrm{T}} - \boldsymbol{1})\boldsymbol{a}, \quad \text{with} \quad \gamma^{\mathrm{T}} := 2\frac{\boldsymbol{e}^{\mathrm{T}}\boldsymbol{G}}{\boldsymbol{e}^{\mathrm{T}}\boldsymbol{G}\boldsymbol{e}}, \tag{3.12}$$

where γ denotes the vector of the so-called adaptor coefficients, γ_ν. Their property

$$\boldsymbol{e}^{\mathrm{T}}\gamma = 2 \tag{3.13}$$

always allows to drop one of these adaptor coefficients in the signal flow diagram of this adaptor, cf. Figure 25.

Moreover, if the adaptor coefficient with greatest value is expressed by the others, all remaining (positive) adaptor coefficients are bounded by one, because of positive port resistances.

At first glance, there is no restriction for the choice of port conductances of parallel adaptors, besides of positiveness of course. But for reasons of realizability, there is often a need to have one port with no directed path between its terminals. This constraint is fulfilled, if the associated port conductance is chosen equal to the sum of the remaining port conductances. In Figure 26 this reflection-free port of the constrained adaptor is assigned with a stroke and one can check that the signal flow diagram contains no directed path between its associated terminals.

With respect to the series connection, the parallel connection is a dual in sense of that the roles of voltages and currents are interchanged:

$$\boldsymbol{e}^{\mathrm{T}}\boldsymbol{v} = 0 \quad \text{and} \quad \boldsymbol{i} = \boldsymbol{e}i_0. \tag{3.14}$$

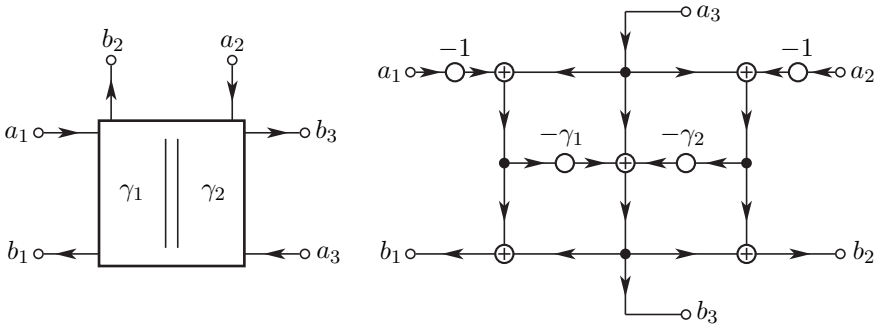

Figure 25: Symbol and wave flow diagram of a 3-port parallel adaptor

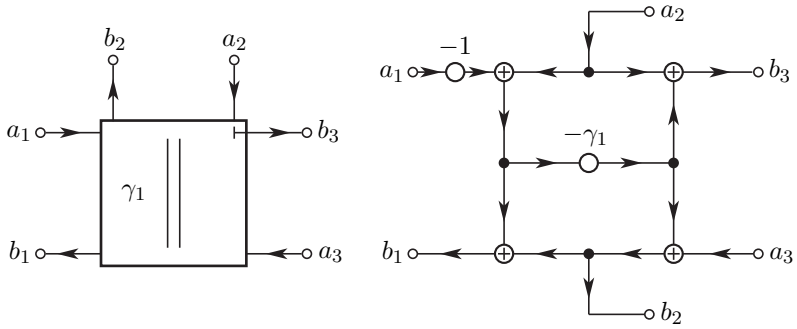

Figure 26: Symbol and wave flow diagram of a 3-port parallel adaptor with reflection-free port 3

Again, after introducing voltage wave quantities we obtain the scattering matrix of a n-port series adaptor

$$\boldsymbol{b} = (\mathbf{1} - \gamma \boldsymbol{e}^{\mathrm{T}})\boldsymbol{a}, \quad \gamma := 2\frac{\boldsymbol{R}\boldsymbol{e}}{\boldsymbol{e}^{\mathrm{T}}\boldsymbol{R}\boldsymbol{e}}, \tag{3.15}$$

were the adaptor coefficients γ_ν meet the condition (3.13).

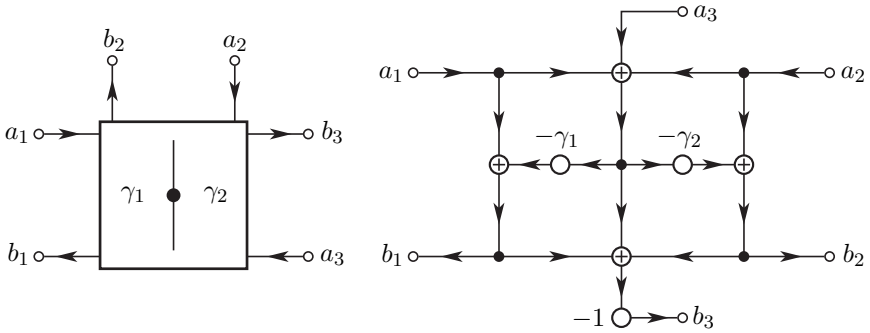

Figure 27: Symbol and wave flow diagram of a 3-port series adaptor

The close relation between these two types of adaptors can also be seen via a comparison of their scattering matrices. They are identical up to a sign inversion and a transposition. In consequence, the signal flow diagram of a parallel adaptor is the same as the signal flow diagram of a series adaptor except for a sign of the incident waves and a signal flow inversion, cf. Figures 25 and 27.

The situation for the constrained series adaptor is just the same as for the constrained parallel adaptor. The symbol of the series adaptor and its signal flow diagram are shown in Figure 28

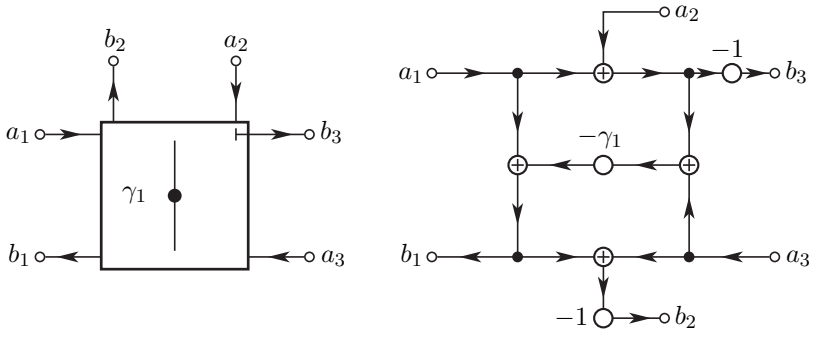

Figure 28: Symbol and wave flow diagram of a 3-port series adaptor with reflection-free port 3

where the port resistance of the reflection-free port is determined by the sum of the remaining port resistances.

For the wave digital concept, every needed n-port adaptor with more than three ports is preferably realized by interconnecting 3-port adaptors of the same type. On the other hand, if 2-port adaptors are needed of series or parallel type it is used to employ a more symmetric type of adaptor, as is shown in Figure 29.

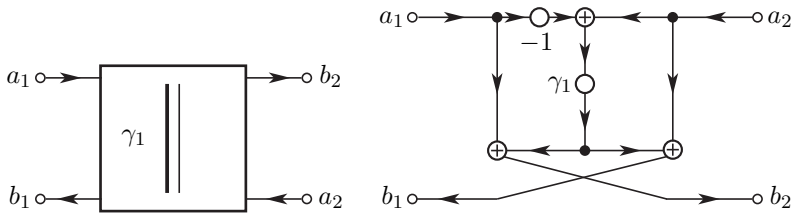

Figure 29: Symbol and wave flow diagram of an alternative 2-port parallel adaptor

Its adaptor coefficient is given by

$$\gamma_1 = \frac{R_1 - R_2}{R_1 + R_2} \tag{3.16}$$

with a magnitude that is bounded by one.

Finally, parallel and series adaptors with only one port degenerate to open- and short-circuits respectively, cf. Figure 30.

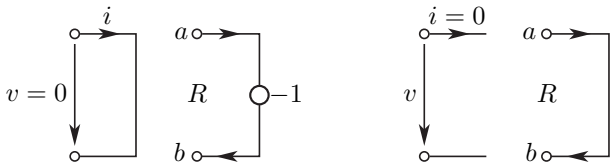

Figure 30: Short- and open-circuit

3.2 Some Basic Properties of Wave Digital Structures

Now, let us assume we have already synthesized a wave digital structure for a given electrical circuit. In order to discuss some properties of these models, we will partition the electrical into resistive sources, reactive elements, and the remaining source- and dynamic-free network as shown in Figure 31.

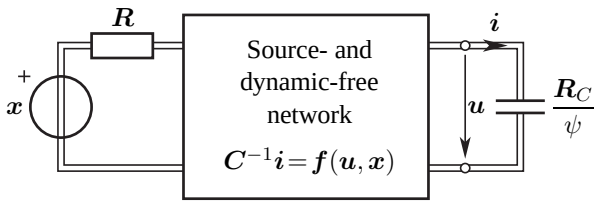

Figure 31: Discrete-time represention of the electrical model

Without loss of generality, resistive sources and reactive elements of the electrical circuit are represented by resistive voltage sources and capacitances, respectively. In correspondence with this partition, the related wave digital model is divided into wave sources, delay elements and the remaining source- and dynamic-free wave digital network with the input signals $\boldsymbol{x}$, output signals $\boldsymbol{y}$, and states $\boldsymbol{w}$, cf. Figure 32.

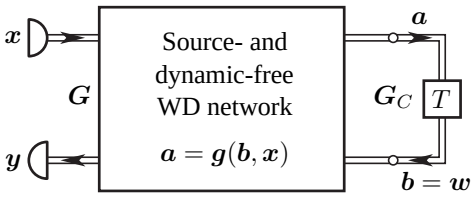

Figure 32: Discrete-time represention of the WD model

In order to define passivity, we will first write the power of a signal $\boldsymbol{x}$ as

$$\|\boldsymbol{x}\|^2 := \boldsymbol{x}^{\mathrm{T}}\boldsymbol{G}\boldsymbol{x}, \tag{3.17}$$

with its positive-definite port conductance matrix $\boldsymbol{G} := \boldsymbol{R}^{-1}$. Having this in mind, a time-discrete model is called passive if the inequality

$$\|\boldsymbol{w}(k+1)\|^2 - \|\boldsymbol{w}(k)\|^2 \leq \|\boldsymbol{x}(k)\|^2 - \|\boldsymbol{y}(k)\|^2 \tag{3.18}$$

holds. In other words, a time-discrete system is passive if the increase of its stored energy is bounded by the difference of the energy which is supplied into the system and the energy which is extracted from the system.

Here, one great advantage of passivity for those time-discrete systems occurs: The equilibrium pint of passive systems are always stable in the sense of LIAPUNOV [Hahn, 1967], where a suitable LIAPUNOV function is given by

$$V(\boldsymbol{w}(k)) := \|\boldsymbol{w}(k)\|^2.$$

In order to verify this statement, we notice that $V(\boldsymbol{w}(k))$ is bounded by

$$G_{C\min}\|\boldsymbol{w}(k)\|^2 \leq \|\boldsymbol{w}(k)\|^2 \leq G_{C\max}\|\boldsymbol{w}(k)\|^2.$$

Additionally, if a free model is considered $V(\boldsymbol{w}(k))$ satisfies also the condition

$$\Delta V(\boldsymbol{w}(k)) := V(\boldsymbol{w}(k+1)) - V(\boldsymbol{w}(k)) \leq 0.$$

As a consequence, the model has the equilibrium point $\mathbf{0}$ which is stable in the sense of LIAPUNOV.

Next, let us examine two passive wave digital models which are interconnected at some of their ports, cf. Figure 33.

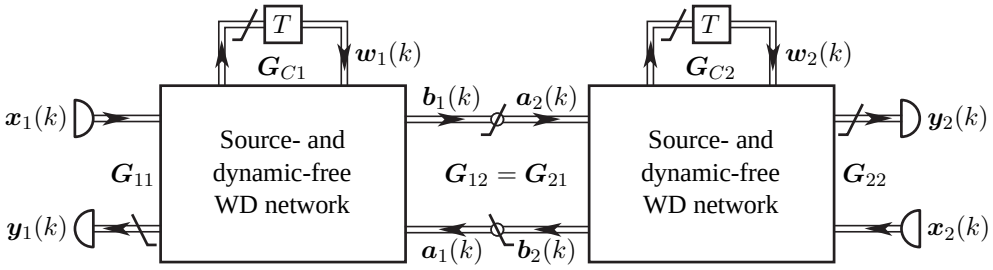

Figure 33: Coupling of two wave digital models

Due to passivity, each of both models satisfies the inequality (3.18), where $\boldsymbol{a}_1$, $\boldsymbol{a}_2$ and $\boldsymbol{b}_1$, $\boldsymbol{b}_2$ have to be assigned to the input and output signals, respectively. Under the assumption that the interconnected ports fulfill the port condition

$$\boldsymbol{G}_{12} = \boldsymbol{G}_{21} \quad \Longrightarrow \quad \boldsymbol{a}_2 = \boldsymbol{b}_1 \quad \boldsymbol{a}_1 = \boldsymbol{b}_2,$$

one can prove that the inequality still remains true for the overall model. As a result, we have found that passivity of a wave digital model follows from passivity of its elements, which are port-wise interconnected. Models with this property are called structural passive. As a consequence wave digital algorithms are robust in this sense by means of that the parameters can vary in a wide range without destroying passivity.

The special form for the energies is of major relevance if passivity has to be ensured even under the finite word-length conditions which always appear for simulations on computer systems. With a look at the definition of passivity (3.18), one can easily check that this inequality still holds if the norms $\|\boldsymbol{w}(k+1)\|$ and $\|\boldsymbol{y}(k)\|$ are decreased. To this end, these quantities are reformatted by sign magnitude truncation in order to ensure passivity. Please notice that this reformation can be done at every port because every particular n-port is also a wave digital model [Meerkötter, 1979].

If we have to deal with linear time-invariant systems only, we can deduce a necessary criterion for passivity from definition (3.18). To this end, we consider a special input signal having the form $\boldsymbol{x}(t_k) = \boldsymbol{X}\mathrm{e}^{pt_k}$ and an initial state so that the states and consequently the output signals are of the same form. Substituting these quantities in eq. (3.18) we get for some arbitrary complex frequency the inequality

$$(\mathrm{e}^{2\mathrm{Re}\,pT} - 1)\|\boldsymbol{W}\|^2 \leq \|\boldsymbol{X}\|^2 - \|\boldsymbol{Y}\|^2$$

where $\|\boldsymbol{X}\|^2$ denotes the steady-state power in correspondence to eq. (3.17). For a passive system we thus must have

$$\mathrm{Re}\,p > 0 \quad \Longrightarrow \quad \|\boldsymbol{Y}\|^2 \leq \|\boldsymbol{X}\|^2 .$$

Let us assume that the relation between the steady-state input and output quantities can be described via a scattering matrix $\boldsymbol{S}$. Then, passivity implies a unitarily bounded scattering matrix:

$$\mathrm{Re}\,\psi > 0 \quad \Longrightarrow \quad \|\boldsymbol{S}(\psi)\| \leq 1 \tag{3.19}$$

where the induced matrix norm

$$\|\boldsymbol{S}\| := \sup_{\|\boldsymbol{X}\|=1} \|\boldsymbol{S}\boldsymbol{X}\|$$

has been used. Provided the impedance matrix,

$$\boldsymbol{Z} = (\boldsymbol{1} + \boldsymbol{S})(\boldsymbol{1} - \boldsymbol{S})^{-1}\boldsymbol{R}, \tag{3.20}$$

exists, then eq. (3.19) is equivalent to the implication:

$$\mathrm{Re}\,\psi > 0 \quad \Longrightarrow \quad \boldsymbol{Z}^*(\psi) + \boldsymbol{Z}(\psi) \geq \boldsymbol{0} . \tag{3.21}$$

A matrix satisfying this condition is called a positive matrix.

Of course, the equations (3.21) or (3.19) provide only necessary conditions for passivity. But, it is known that for a unitarily bounded scattering matrix, it is always possible to synthesize a corresponding concretely passive electrical circuit [Belevitch, 1968].

4 Topological Analysis of Electrical Circuits

Objective of the topological analysis described here is the generation of the adaptor structure for a given electrical circuit, S. Such an adaptor structure is represented by a special decomposition tree. The algorithm for setting up this decomposition tree requires several definitions and is a bit extensive; it is based on the graph-theoretical concepts of connectivity, independent subnetworks, triconnected components, series-parallel graphs, and tree decomposition.

First of all, subsection 4.1 develops the necessary graph-theoretical concepts and illustrates their role in the electrical domain. Subsection 4.2 presents the linear-time algorithm ADAPTORS, which constructs an optimum adaptor structure for a given electrical circuit S.

4.1 Graph-Theoretical Concepts for Effort-Flow-Systems

A coupling between two—not necessarily electrical—systems can be represented by a pair of system variables whose product is the instantaneous power being transmitted trough an energy port [Wellstead, 1979, pg. 12]. For each port these system variables divide into one intensive flow variable (current, fluid flow, velocity, etc.) and one extensive effort variable (voltage, pressure, force, etc.). Figure 34 illustrates such a generic port, from which Figure 4 on Page 7 shows the electrical interpretation.

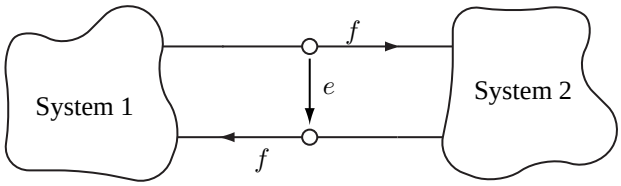

Figure 34: Energy transmittal in effort-flow-systems is realized by means of ports each of which being characterized by an effort variable, e, and a flow variable, f.

Port Property

It is reasonable to stipulate that each basic system element that provides a pair of terminals establishes a one-port. When joining together one-port elements, new constraints are introduced—the aforementioned connection constraints—which relate to the elements' effort variables and flow variables. There exist only two ways by which two one-port elements can be interconnected: in series or in parallel, as shown in Figure 35.

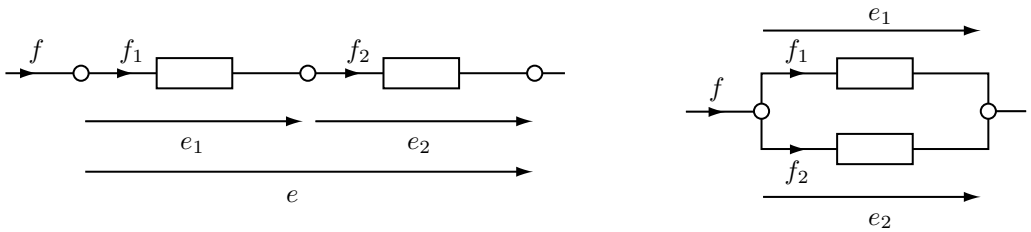

Figure 35: Connecting two one-ports in series (left-hand side) and in parallel (right-hand side).

The related connection constraints are called compatibility and continuity constraints upon the effort and flow variables; they are of the following form:

$$e = e_1 + e_2 \qquad f = f_1 = f_2 \qquad \text{(series connection)}$$
$$e = e_1 = e_2 \qquad f = f_1 + f_2 \qquad \text{(parallel connection)}$$

For electrical systems, compatibility and continuity constraints are known as Kirchhoff's voltage and current law respectively.

Note that the series as well as the parallel connection of two ports again yields a port. This fact, along with the plain form of the connection constraints, enables us to easily combine the characteristics of the basic system elements. And, as already pointed out in Subsection 2.2, Page 6, this gives rise to an algorithm that computes the system variables for a given system S by means of local propagation. If S is formulated within the a/b-wave domain and if differential characteristics are approximated by means of the trapezoid rule, this algorithm will represent a WDS; i. e., it defines a feedback-free signal flow graph whose processing resembles the dynamic behavior of S.

Prerequisite for the design of a WDS from an electrical system S thus is the detection of the ports within S. Clearly, if S is constructed from bottom-up by applying only series and parallel connections, the topology of S will be isomorphic to a series-parallel graph, and all ports can be easily found. However, typically this is not the case, and S contains "closely connected" subsystems.

A solution of this problem is described in [Stein, 1995] as part of a network preprocessing approach: The port concept is extended towards so-called independent subnetworks, and the relation between independent subnetworks and triconnected components is exploited to identify all ports within a flow network.[2] We will follow the same idea here; the remainder of the section presents the necessary definitions.

Definition 1 (Corresponding Graph of an Electrical Circuit) *Let S be an electrical circuit. The corresponding graph of S is a multigraph $G = \langle V, E, g\rangle$ whose elements are defined as follows. V is the set of segments of the interconnecting network in S that form areas of equal potential, E is the set of one-port elements in S, and g is a mapping, $g : E \to \mathcal{P}(V)$ where $g(e) \mapsto \{v, w\}$ iff e connects the potential areas v and w. E is called the set of edges, V is called the set of points, and g is called the incidence map.*

Remarks. (1) Typically, numbers are used to designate the elements in V. (2) Without loosing generality, the incidence map g is often omitted, and the elements in the multiset E are denoted as two-element sets $\{v, w\} \in \mathcal{P}(V)$: It is obvious that a bijective mapping between the elements in S and in E can be maintained.

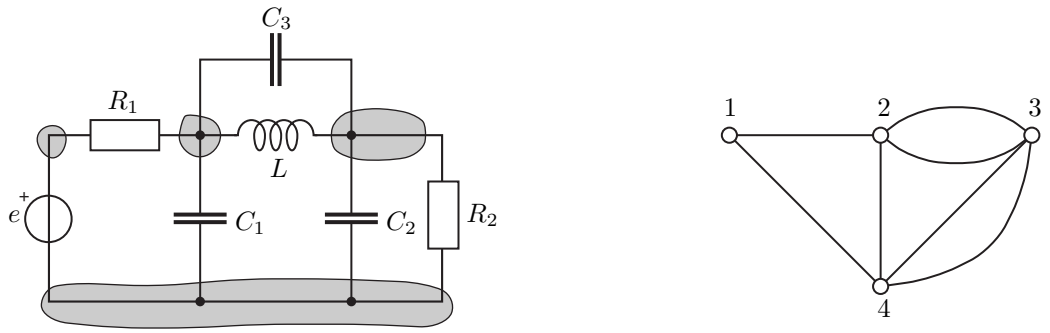

Figure 36: Electrical circuit with corresponding graph. The shaded regions in the circuit indicate the areas of equal potential in the interconnecting network.

Example. Given the electrical circuit S depicted in Figure 36; a corresponding graph G of S is defined on the set of points $V = \{1, 2, 3, 4\}$, the edge set $E = \{e, L, R_1, R_2, C_1, C_2, C_3\}$, and the

[2]There, the ports are identified to reformulate a global model of a fluidic network into a new model that can be processed by local propagation. However, with respect to its runtime $\mathcal{O}(|E| \cdot |V|)$ the used detection algorithm for triconnected components is suboptimum.

incidence map $g = \{(R_1, \{1,2\}), (e, \{1,4\}), (L, \{2,3\}), (C_3, \{2,3\}), (C_1, \{2,4\}), (C_2, \{3,4\}), (R_2, \{3,4\})\}$.

In the case the incidence map is dropped, E is described by the following multiset $E = \{\{1,2\}, \{1,4\}, \{2,3\}, \{2,3\}, \{2,4\}, \{3,4\}, \{3,4\}\}$.

Definition 1 enables us to disburden our considerations from electrical circuits and use their graph equivalents instead.

Definition 2 (Two-Terminal Graph, Flow) *A two-terminal labeled graph is a triple $\langle G, s, t\rangle$, where $G = \langle V, E\rangle$ is a (multi)graph and $s, t \in V$, $s \neq t$. s and t are called source and sink of G respectively.*

A mapping $f : E \to V \times \mathbf{R}$, $f(\{v,w\}) \mapsto (u,x)$, $u \in \{v,w\}$, on a two-terminal labeled graph $\langle G, s, t\rangle$ is called flow on G if the conservation law holds for every point $v, v \neq s, t$ in G:

$$\sum_{e \in E_v} y = 0 \quad \textit{with} \quad y = \begin{cases} x & \textit{if } f(e) = (v,x) \\ -x & \textit{if } f(e) = (w,x) \end{cases}$$

$E_v \subset E$ comprises the edges incident to v. If the function f does also depend on the parameter time, the conservation law must hold for any element in the time domain.

Remarks. Standard flow definitions refer to directed graphs and a positive flow function f. In the presented definition the flow function prescribes both flow direction and flow value since we are dealing with undirected graphs. Of course, a non-positive flow function can be made positive by partially redefining it: $(\{v,w\}, (v,x))$ is replaced with $(\{v,w\}, (w,-x))$ if $x < 0$.

Independent Subnetwork

Ports are characterized by the property that they possess two terminals where for each point in time the related flow values are of equal amount and opposite direction. In this sense, a terminal of a port corresponds to the graph-theoretical concept of an edge. For our analysis of graphs it is necessary to extend the port concept towards so-called independent subnetworks whose terminals correspond to nodes.

Definition 3 (Independent Subnetwork [Stein, 1995]) *Let $G = \langle V, E\rangle$ be a graph, and let H be a subgraph of G induced by $V_H \subset V$ with $|V_H| > 2$. A two-terminal labeled graph $\langle H, s_H, t_H\rangle$ is called independent subnetwork of G, if the following condition holds:*

(1) Every walk from a point in $V \setminus V_H$ to a point in V_H contains either s_H or t_H.

An independent subnetwork H will be called minimum, if there exists no independent subnetwork which is induced on a proper subset of V_H.

Let $\langle H, s_H, t_H\rangle$ be an independent subnetwork of a two-terminal labeled graph $\langle G, s, t\rangle$. Observe that the topology of H guarantees that an energy exchange between H and G can happen only via the nodes s_H and t_H. Moreover, KIRCHHOFF's node rule states the conservation of the electric current, which thus defines a flow in the sense of Definition 2. From this conservation property follows that for each current flow on H the sum of all in-going currents at s_H equals the sum of all outgoing currents at t_H [Jungnickel, 1990, pg. 106]. Together both aspects enable us to enclose independent subnetworks with a hull, say, to investigate them in an isolated manner. An important consequence is that the concepts "port" and "independent subnetwork" can be used interchangeably (see Figure 37).

Remarks. (1) Since each part of a system S that corresponds to an independent subnetwork must be treated by a global numerical procedure, we are interested in a decomposition of S into minimum independent subnetworks. (2) Independent subnetworks are not multiports. The physical concept of

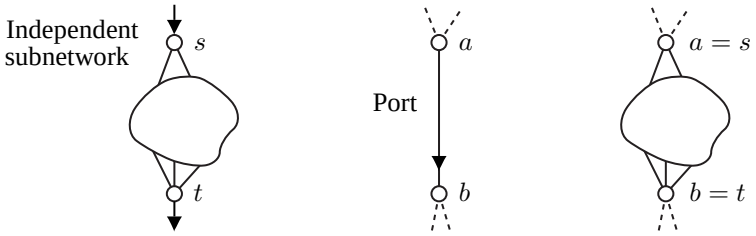

Figure 37: Substituting an independent subnetwork (left) for a port (middle) does not violate the conservation law.

a multiport can be entirely reproduced by adding to the definition of a multigraph G a decomposition $\mathcal{C}$ of the edge set E. Each set $C \in \mathcal{C}$ stands for a subset of E and defines a multiport in a definite way.

Series-Parallel Graph

Definition 4 (Series-Parallel Graph [Booth and Tarjan, 1993, Brandstaedt et al., 1999]) *Let $\langle G,s,t\rangle$ be a two-terminal labeled graph. G is called two-terminal series-parallel with source s and sink t if it can be built by means of the following three rules:*

(1) Base Graph. Any graph of the form $G = \langle\{s,t\},\{\{s,t\}\}\rangle$ is a two-terminal series-parallel with source s and sink t.

Let $G_1 = \langle V_1, E_1\rangle$ be two-terminal series-parallel with source s_1 and sink t_1, and let $G_2 = \langle V_2, E_2\rangle$ be two-terminal series-parallel with source s_2 and sink t_2.

(2) Series Composition. The graph formed from G_1 and G_2 by unifying t_1 and s_2 is two-terminal series-parallel, with source s_1 and sink t_2.

(3) Parallel Composition. The graph formed from G_1 and G_2 by unifying s_1 and s_2 and unifying t_1 and t_2 is two-terminal series-parallel, with source $s_1 = s_2$ and sink $t_1 = t_2$.

Two-terminal series-parallel graphs can be represented by decomposition trees, also called sp-trees, cf. [de Fluiter, 1997], which generalize the series and the parallel composition to more than two operands.

Definition 5 (sp-tree) *An sp-tree $T_{\langle G,s,t\rangle}$ of a two-terminal series-parallel graph $\langle G,s,t\rangle$ is a rooted tree whose nodes are either of type s-node, p-node, or leaf-node. Each node is labeled by a pair (u,v), $u,v \in V$; the children of an s-node are ordered; the leafs of $T_{\langle G,s,t\rangle}$ correspond one-to-one to the edges of G.*

Every node of an sp-tree corresponds to a unique two-terminal series-parallel graph $\langle H,u,v\rangle$, where H is a subgraph of G and (u,v) is the label of the node. The root of $T_{\langle G,s,t\rangle}$ has label (s,t) and corresponds to the graph $\langle G,s,t\rangle$. The two-terminal series-parallel graph defined by an s-node is the result of the series composition applied to its children in their given order. The two-terminal series-parallel graph defined by a p-node is the result of the parallel composition applied to its children.

Figure 38 exemplifies the definition.

The composition rules laid down in Definition 4 make apparent that a series-parallel graph whose sp-tree has a root node label of series-node and parallel-node type has a vertex connectivity of one and two respectively. Graphs of a higher vertex connectivity are the result of either connecting more than three two-terminal graphs at the same time or by connecting two-terminal graphs by a different rule. Formally, the vertex connectivity of a graph is defined as follows.

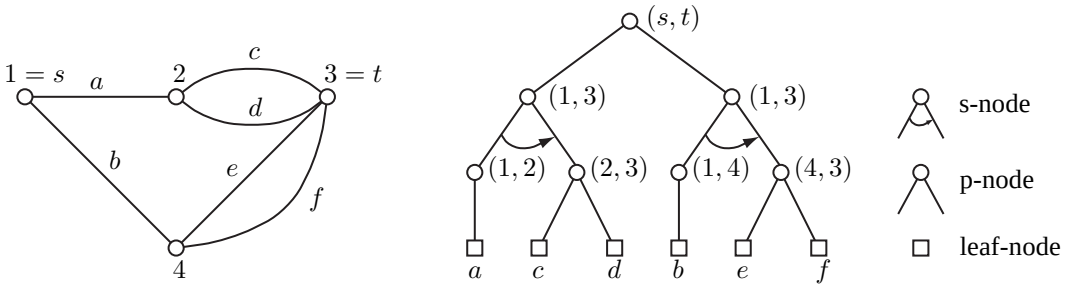

Figure 38: Series-parallel graph (left) and its sp-tree representation (right).

Definition 6 (Vertex Connectivity $\kappa(G)$) *Let $G = \langle V, E\rangle$ be a graph. $\kappa(G)$ is called vertex connectivity of G and is defined as follows. $\kappa(G) = \min\{|T| \mid T \subset V$ and $G[V \setminus T]$ is not connected $\}$. G is called k-connected, if $\kappa(G) \geq k$.*

$G[V']$ denotes the subgraph of G that is induced by $V' \subseteq V$.

Remarks. A cut point (or articulation point) of a graph G is a point $v \in V$ for which $G[V \setminus \{v\}]$ has more connected components than G. A connected graph without cut points is called biconnected; a connected graph with cut points is called separable; the maximum inseparable induced subgraphs of a graph G are called biconnected components. The separation of a graph G into its biconnected components is unique [Tarjan, 1972]. This fact, together with the fact that each biconnected component is analyzed on its own, we can assume without loss of generality that the considered graphs are biconnected.

The subsequent definition extends the cut point construct, it is derived from Hopcroft and Tarjan [1973].

Definition 7 (Separation Pair) *Let $\{a, b\}$ be a pair of vertices in a biconnected multigraph G, and let the edges of G be divided into equivalence classes $E_1, \ldots, E_n$ such that two edges which lie on a common path not containing any vertex of $\{a, b\}$ except as an endpoint are in the same class.*

The classes E_i are called separation classes of G with respect to $\{a, b\}$. If there are at least two separation classes, then $\{a, b\}$ is a separation pair of G unless (1) there are exactly two separation classes, and one class consists of a single edge, or (2) there are exactly three classes, each consisting of a single edge.

If G is a biconnected multigraph such that no pair $\{a, b\}$ is a separation pair of G, then G is triconnected.

Triconnected Components

While the triconnectivity of a graph G follows canonically from Definition 6 or 7, the characterization of a graph's triconnected components is more involved. The reason for this difficulty is that triconnected components possess no property that permits their detection by a divide-and-conquer approach. Instead, it is necessary to investigate the relation of H with respect to G if a subgraph H of G forms a suspect triconnected component. Moreover, Hopcroft and Tarjan introduce different types of triconnected components, and hence the relation between H and G must be investigated relating different properties [Hopcroft and Tarjan, 1973]. Their definitions are given now.

Definition 8 (Split Graph, Splitting, Split Component) *Let G be a multigraph with separation pair $\{a, b\}$ and related separation classes $E_1, \ldots, E_n$. Moreover, let $E' = \bigcup_{i=1}^{k} E_i$ and $E'' = \bigcup_{i=k+1}^{n} E_i$ be such that $|E'| \geq 2$, $|E''| \geq 2$, and let $G_1 = \langle V(E'), E' \cup \{(a, b)\}\rangle$, and $G_2 = \langle V(E''), E'' \cup \{(a, b)\}\rangle$. Then the graphs G_1 and G_2 are called split graphs of G with respect to $\{a, b\}$. Replacing G by two split graphs is called splitting G.*

If the split graphs are further split, in a recursive manner, until no more splits are possible, the remaining graphs are called split components of G.

Remarks. (1) The new edges $\{a, b\}$ added to G_1 and G_2 are called virtual edges; they can be labeled to identify the split. (2) If G is biconnected then any split graph of G is also biconnected. (3) The split components of a multigraph are not necessarily unique.

The split components of a multigraph are of three types: triangles of the form $\langle\{a, b, c\}, \{\{a, b\}, \{a, c\}, \{b, c\}\}\rangle$, triple bonds of the form $\langle\{a, b\}, \{\{a, b\}, \{a, b\}, \{a, b\}\}\rangle$, and triconnected graphs. To obtain unique triconnected components, the split components must be partially reassembled.

Reassembling is accomplished by merging. Suppose that $G_1 = \langle V_1, E_1\rangle$ and $G_2 = \langle V_2, E_2\rangle$ are two split components containing an equally labeled virtual edge $\{a, b\}$. Then the result of a merging operation is a graph G_{1+2} with node set $V_{1+2} = V_1 \cup V_2$ and edge set $E_{1+2} = E_1 \setminus \{\{a, b\}\} \cup E_2 \setminus \{\{a, b\}\}$.

Definition 9 (Triconnected Component) *Let G be a multigraph whose split components are a set of triangles $\mathcal{S}_3$, a set of triple bonds $\mathcal{P}_3$, and a set of triconnected graphs $\mathcal{C}$. If the triangles are merged as much as possible to give a set of polygons $\mathcal{S}$, and if the triple bonds are merged as much as possible to give a set of bonds $\mathcal{P}$, then the set of graphs $\mathcal{S} \cup \mathcal{P} \cup \mathcal{C}$ forms the set of triconnected components of G.*

Series and Parallel Reduction

Remarks. (1) The triconnected components of a graph G are unique (see [Tarjan and Hopcroft, 1972]). (2) The "triconnected components" in $\mathcal{S}$ are not triconnected in the sense of Definition 6. They establish generic series connections: Virtual edges designate the connection of a subgraph; the other edges designate single elements in S. From the viewpoint of a KIRCHHOFF interconnecting network the non-virtual incident edges can be replaced with a single edge of appropriate impedance. This process is called series reduction. (3) The triconnected components in $\mathcal{P}$ are defined on two points only. They establish generic parallel connections: Virtual edges designate the connection of a subgraph; the other edges designate single elements in S—from the viewpoint of a KIRCHHOFF interconnecting network they can be replaced with a single edge of appropriate admittance. This process is called parallel reduction. (4) The triconnected components in $\mathcal{C}$ establish minimum independent subnetworks (see [Stein, 1995]).

Figure 39 shows a graph and its split components. Except the triangles $(1, 3, 4)$ and $(1, 2, 3)$, the split components establish triconnected components; the set of triconnected components is complete if the triangles are merged.

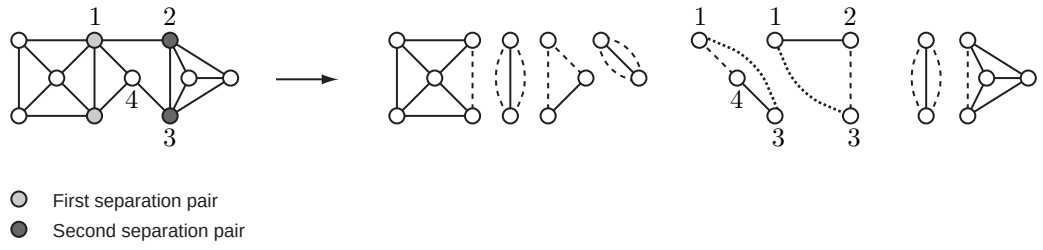

Figure 39: A graph and its split components. When the triangles $(1, 3, 4)$ and $(1, 2, 3)$ are merged, the right hand side shows all triconnected components of the graph.

The algorithm presented in [Hopcroft and Tarjan, 1973] delivers the triconnected components as defined above and runs in $\mathcal{O}(|E|)$. We will rely on it in the next section. The algorithm originates from AUSLANDER and PARTER's idea for an efficient planarity test [Hopcroft and Tarjan, 1973, Auslander and Parter, 1961]. Root of its efficiency is the statement of necessary conditions for

separation pairs along with a clever computation of these conditions within several depth-first search runs.

Inadmissible Segmentation

Hopcroft and Tarjan's algorithm does not consider the semantics of independent subnetworks. As a consequence, independent subnetworks can be torn, resulting in inadmissible segmentations. Figure 40 shows two isomorphic graphs with a different s,t-labeling. A decomposition of this graph into its split components tears the independent subnetwork with source s_2 and sink t_2.

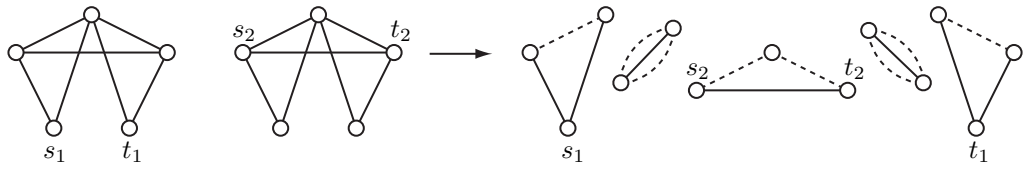

Figure 40: Two isomorphic graphs with a different s,t-labeling (left) and the related split components (right). The independent subnetwork with the labeling s_1, t_1 is torn.

Obviously all triconnected components of a two-terminal labeled graph $\langle G, s, t\rangle$ establish independent subnetworks if there is a triconnected component containing both s and t. The following definition and Lemma 1 formalize this assertion.

Definition 10 (Elementary Contraction, s-t-Contractible) *Let $\langle G, s, t\rangle$, $G = \langle V, E\rangle$, be a connected two-terminal labeled graph (not necessarily series-parallel), let $\{v, w\} \in E$, and let $V_w \subset V$ comprise the nodes adjacent to w. Then the graph $G' = \langle V', E'\rangle$ is called an elementary contraction of G respecting w, if $V' := V \setminus \{w\}$, and $E' := E \setminus \{\{w, x\} \mid x \in V_w\} \cup \{\{v, x\} \mid x \in V_w, x \neq v\}$.*

G is called s-t-contractible towards a graph $G' = \langle V', E'\rangle$, if G' is the result of a sequence of elementary contractions, and if $\{s, t\} \in E'$.

The s-t-contractibility states that the flow conservation between s and t remains intact for a two-terminal labeled graph $\langle G, s, t\rangle$. It can be ensured by simply adding the edge $\{s, t\}$ to G if s and t are not adjacent. This modification of G does not restrict its segmentation into independent subnetworks.

Lemma 1 (s-t-Contractibility) *Let $\langle G, s, t\rangle$, $G = \langle V, E\rangle$, be a connected two-terminal labeled graph (not necessarily biconnected) with source s and sink t, and let $\{s, t\} \notin E$. Moreover let G' be $\langle V, E \cup \{\{s, t\}\}\rangle$, and let $G'_1, \ldots, G'_m$ be the triconnected components of G'. Then the following holds:*

(1) $\exists G'_i$ which is s-t-contractible,

(2) G' can be decomposed into the same independent subnetworks like G.

Proof of Lemma 1. Point (1). Follows immediately from the fact that there must be some graph G'_i that contains the edge $\{s, t\}$. Point (2). Observe that for an independent subnetwork $\langle G_i, a, b\rangle$ that has s (or t) amongst its nodes one of the following equations must hold: $a = s$ or $b = s$. This follows from the independent subnetwork definition. If G' cannot be decomposed into the same independent subnetworks like G then this must be on account of the edge $\{s, t\}$. It prohibits a segmentation of some G'_i into the independent subnetworks $\langle G_i, s, a\rangle$ and $\langle G_j, t, b\rangle$, which could be formed when segmenting the original graph G. Since $\langle G_i, s, a\rangle$ and $\langle G_j, t, b\rangle$ form independent subnetworks, a and b must be articulation points of G, which in turn means that $\{s, a\}$ and $\{s, b\}$ establish separation pairs in G'. Hence, an independent subnetwork G'_k can be formed that contains $\{s, t\}$ as its only non-virtual edge. Conversely, the edge $\{s, t\}$ does not prohibit the formation of independent subnetworks that can be formed in G. ◇

Decomposition Tree

As outlined in the remarks on Page 30, the three types of triconnected components form the backbone for the segmentation of a circuit S: Based on the the sets $\mathcal{S}$, $\mathcal{P}$, and $\mathcal{C}$, a connector structure, or as the case may be, an adaptor structure is easily constructed. In this connection it is useful and quite natural to extend the concept of sp-trees (Definition 11) towards spc-trees.

Definition 11 (spc-tree) *An spc-tree $T_{\langle G,s,t\rangle}$ of a two-terminal (multi)graph $\langle G, s, t\rangle$ is a rooted tree whose nodes are either of type s-node, p-node, c-node, or leaf-node. A c-node is labeled by the graph $\langle V_H, E_H, u, v\rangle$ it stands for; the other nodes are labeled by a pair (u, v). The children of an s-node are ordered; the leafs of $T_{\langle G,s,t\rangle}$ correspond one-to-one to the edges of G.*

Every node of an spc-tree corresponds to a unique two-terminal graph $\langle H, u, v\rangle$; the root of $T_{\langle G,s,t\rangle}$ corresponds to the graph $\langle G, s, t\rangle$. The two-terminal graph defined by an s-node is the result of the series composition applied to its children in their given order, and the two-terminal graph defined by a p-node is the result of the parallel composition applied to its children. The two-terminal graph defined by a c-node is triconnected, has more than three nodes, and follows no construction rule.

The spc-tree $T_{\langle G,s,t\rangle}$, $T_{\langle G,s,t\rangle} = \langle V_T, E_T\rangle$ is easily constructed. $V_T = \{1, \ldots, n + |E_G|\}$ where n denotes the number of triconnected components and $|E_G|$ denotes the number of edges in G; the nodes in $\{1, \ldots, n\}$ correspond one-to-one to the triconnected components and are labeled respecting the triconnected component's type as S-node, P-node, and C-node respectively. E_T contains an edge $\{v, w\}$ if and only if one of the following conditions is fulfilled: (1) v and w correspond to triconnected components and have a common virtual edge, (2) v corresponds to a triconnected component and w is an edge in v.

Remarks. Since both the series adaptor and the parallel adaptor are realized as three-port adaptors, the nodes of the spc-tree that are labeled as P-node or S-node may be expanded again to account for their restricted number of ports. Moreover, observe that the height of the decomposition tree defines the longest propagation path of the adaptor structure. Consequently the root of the decomposition tree should be defined as some node leading to a minimum tree height. The subsequent definition picks up both aspects and introduces a normalized spc-tree.

Definition 12 (Normalized spc-tree) *Let $T_{\langle G,s,t\rangle} = \langle V_T, E_T\rangle$ be an spc-tree. $T_{\langle G,s,t\rangle}$ is called normalized spc-tree if each node $v \in V_T$ labeled S or P has at most two successors, and if the root v of $T_{\langle G,s,t\rangle}$ represents a center of $T_{\langle G,s,t\rangle}$ and has a degree larger than 1.*

Remarks. (1) $T_{\langle G,s,t\rangle}$ is normalized by replacing each node $v \in V_T$ labeled S or P that has more than two successors with the root of a balanced binary tree, T_v, whose leafs are the successors of v; the inner nodes of T_v get the same label as v. (2) The center of a tree $T = \langle V, E\rangle$ can be computed in $\mathcal{O}(|V|)$ [Mitchell Hedetniemi et al., 1981].

4.2 Generating the Adaptor Structure for Electrical Circuits

The previous subsection provides the theoretical underpinning for the following adaptor synthesis algorithm.

Input. An electrical circuit, S.
Output. A normalized spc-tree defining the optimum adaptor scheme and types,
the port resistances, and the adaptor coefficients.

Algorithm. ADAPTORS

(1) Generate the corresponding graph G of S.

(2) Partition G respecting its biconnected components $G_1, \ldots, G_m$. For each G_i do:

   (a) Check for inadmissible segmentation.

   (b) Detect triconnected components.

   (c) Construct an spc-tree.

(3) Construct an spc-tree $T_{\langle G,s,t\rangle}$ for the entire graph G.

(4) Normalize $T_{\langle G,s,t\rangle}$.

(5) Compute the port resistances and adaptor coefficients.

Theorem 1 *Given an electrical circuit S containing n elements. Then* ADAPTORS *computes a normalized spc-tree defining the optimum adaptor scheme and types, the port resistances, and the adaptor coefficients in $\mathcal{O}(n)$.*

Proof 1 *The runtime bounds for the Steps 1–2b follow from the considerations and algorithms pointed out in the previous section. Step 3, the connection of the forest of the m spc-trees, $m < n$, is linear. Finally, the adaptor computations within Step 5 involve only a constant number of operations for each of the n elements (see Section 2 and 3).*

In the sequel, some steps of ADAPTORS are illustrated at the sample graph of Figure 41, which establishes the corresponding graph G of some electrical circuit S.

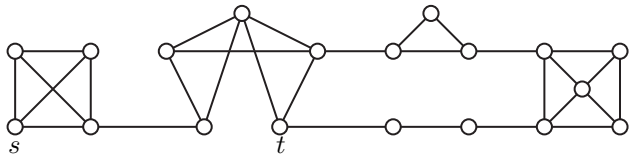

Figure 41: Corresponding graph G of some electrical circuit S.

Step 2. Partition G respecting its biconnected components, $G_1, \ldots, G_m$. Label the articulation points of the G_i by s_i or t_i, such that each biconnected component contains a source s_i and a sink t_i.

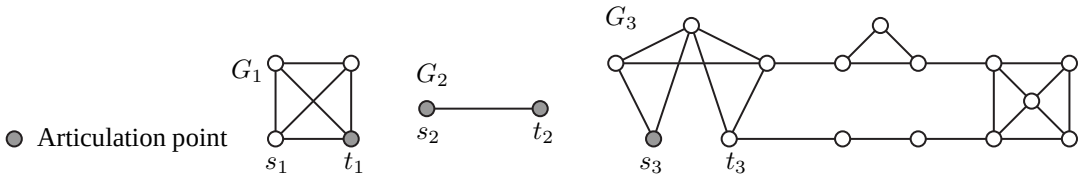

Figure 42: Decomposition of G_S respecting its biconnected components and relabeling of the biconnected as two-terminal graphs.

Step 2a. Check for inadmissible segmentations. In the sample graph an edge $\{s_2, t_2\}$ is introduced. However, in electrical circuits this step is superfluous if s and t are incident to the signal source.

Step 2b. Detect in G_2 the three sets of different triconnected components, $\mathcal{S}$, $\mathcal{P}$, and $\mathcal{C}$.

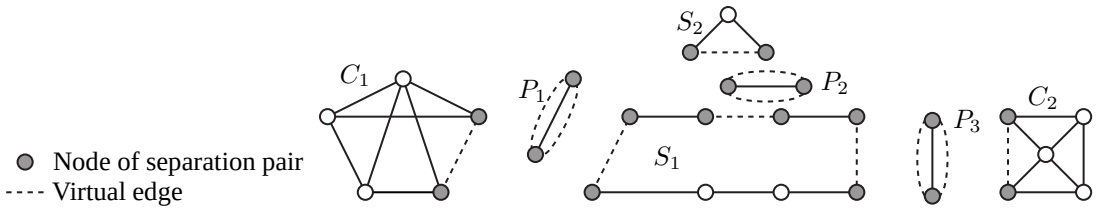

Figure 43: Detection of the triconnected components.

Step 2c. Construct an spc-tree $T_{\langle G_3,s_3,t_3\rangle}$ for G_3; the left-hand side of Figure 44 shows the result. At this place the previously mentioned series reductions and parallel reductions are ideally performed: Engineering knowledge on useful reductions can be formulated by means of simple contraction rules, which may even investigate the context of an element.[3]

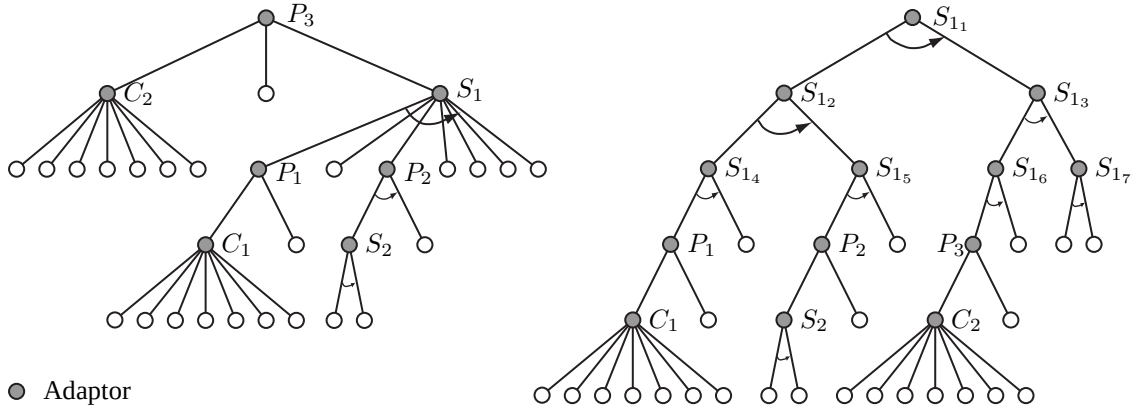

Figure 44: An unnormalized spc-tree of G_3 (left) and its normalized counterpart (right); the leafs of the trees correspond to the edges in G_3.

Step 3. Construct an spc-tree $T_{\langle G,s,t\rangle}$ for the entire graph G. This accomplished by connecting the roots of the trees $T_{\langle G_i,s_i,t_i\rangle}$ with a new node that is labeled as an S-node.

Step 4. Normalize the decomposition tree $T_{\langle G,s,t\rangle}$; the right-hand side of Figure 44 shows the result. Obviously, the ideal adaptor for having no reflection-free port is associated with the root of the normalized the decomposition tree.

Step 5. Based on the component parameters in S compute the port resistances for the adaptors as described in Section 2 and 3.

Extension The algorithm ADAPTORS can be extended with respect to multiports. To this end each subgraph that is induced by a multiport is completed such that it forms a clique.

Of course there are other concepts for a special treatment (preprocessing) of multiports. The usage of cliques may establish the most elegant solution since it does not require a modification of the presented procedures.

[3]Such rules may treat the introduction of resistive sources, or the comprisal of elements of the same type. Note that design graph grammars provide an ideal means to encode this type of knowledge [Schulz et al., 2001].

5 Passive Linear Multistep Methods

This section extends the passivity considerations outlined in Subsection 2.5, page 13. In particular it is shown, in which way numerical integration methods for passive nonlinear electrical circuits can be developed that conserve the passivity property (cf. [Fettweis, 1971, Felderhoff, 1994, Ochs, 2001]).

To this end, we will restrict our considerations towards nonlinear electrical circuits that are built up from resistive sources and, as the only reactive element, the capacitance, which can be used to realize the other reactive elements. Note that even nonlinear reactive element can be put down to an appropriately controlled capacitance.

A formulation of such an electrical circuit as differential equation system is given by

$$\dot{\mathbf{v}}(t) = \mathbf{C}^{-1}\mathbf{i}(t) \tag{5.1}$$

where the capacitances have been collected in the diagonal matrix $\mathbf{C}$. The equation system (5.1) can be written as a function of a voltage vector $\mathbf{v}(t)$ and the vector of signal sources, $\mathbf{x}(t)$.

$$\dot{\mathbf{v}}(t) = \mathbf{f}(\mathbf{v}(t), \mathbf{x}(t)), \qquad \mathbf{v}(t_0) = \mathbf{v}_0, \tag{5.2}$$

This notation corresponds to a separation of the reactive elements from the remaining network.

The sequel of this section is organized as follows. The next subsection introduces the new concept of the characteristic impedance, which then is used in Subsection 5.2 and Subsection 5.3 to develop conditions for consistency orders of linear multistep methods.

Note that the results of this section can be transferred to all systems whose behavior model can be formulated as a source- and dynamic-free (nonlinear) algebraic network that is coupled with a set of linear capacitances.

5.1 Characteristic Impedance

A linear multistep method is an integration method which approximates the solution of eq. (5.2) by the rule

$$\boldsymbol{v}_k = -\sum_{\sigma=1}^{s} \alpha_\sigma \boldsymbol{v}_{k-\sigma} + T\boldsymbol{C}^{-1} \sum_{\sigma=0}^{s} \beta_\sigma \boldsymbol{i}_{k-\sigma} \tag{5.3}$$

with the separated (nonlinear) algebraic equations

$$\boldsymbol{C}^{-1}\boldsymbol{i}_k := \boldsymbol{f}(\boldsymbol{v}_k, \boldsymbol{x}_k) \tag{5.4}$$

where α_σ and β_σ are arbitrary parameters. With regard to the underlying electrical circuit, this separation is natural because we have divided the circuit into reactive elements and the remaining network, cf. Fig. 31. On this account, the nonlinear algebraic equations can be implemented with the aforementioned concepts but we have to find proper realizations for the linear difference equations.

For this purpose, let us consider the steady-state voltage-current relation of a single reactive element C, i. e., its signals are of the form $v_k := V\mathrm{e}^{pt_k}$ and $i_k := I\mathrm{e}^{pt_k}$. Putting these quantities into the linear difference equation (5.3) we get

$$V = \frac{T}{2C}\hat{Z}(\mathrm{e}^{pT})I, \quad \hat{Z}(\mathrm{e}^{pT}) := \frac{2\sum_{\sigma=0}^{s} \beta_\sigma \mathrm{e}^{-\sigma pT}}{1 + \sum_{\sigma=1}^{s} \alpha_\sigma \mathrm{e}^{-\sigma pT}}, \tag{5.5}$$

cf. [Nitsche, 1993, Fischer, 1984, Felderhoff, 1994, Genin, 1973]. In this paper, the rational fraction is designated as the (normalized) characteristic impedance of a linear multistep methods.

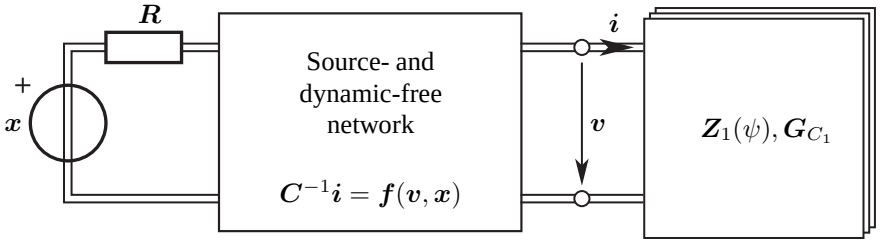

Figure 45: Discrete-time representation of a reference circuit of a linear multistep method..

As will be exposed later on, it will be convenient to employ the equivalent complex frequency variable ψ instead of p. If we make use of the transformation (3.8), we obtain

$$Z(\psi) := \hat{Z}\left(\frac{1+\psi}{1-\psi}\right) = \frac{\sum_{\sigma=0}^{s} c_\sigma \psi^\sigma}{\sum_{\sigma=0}^{s} d_\sigma \psi^\sigma} \tag{5.6}$$

where one of these coefficients can be normalized. Here, linear multistep methods having a positive characteristic impedance $Z(\psi)$ will be called passive.

With regard to a realization of $Z(\psi)$, we will focus on methods having a canonic realization of the characteristic impedance. In particular, we will only consider irreducible methods, i. e., methods whose numerator and denominator polynomials have no common divisor.

A linear multistep method as defined by eq. (5.3) is called explicit if $\boldsymbol{v}_k$ depends only on past values of $\boldsymbol{v}$ and $\boldsymbol{i}$. Clearly, the method as given by eq. (5.3) is explicit if and only if $\beta_0 = 0$. But the passivity of linear multistep methods excludes explicit methods because $\beta_0 = 0 \Longleftrightarrow Z(1) = 0$ implies that $Z(\psi)$ has a zero in the right half ψ-plane in contradiction to properties of positive functions, cf. [Belevitch, 1968]. Since we are interested in passive integration methods only, we will restrict ourselves to implicit linear multistep methods.

5.2 Consistency Order

In order to have a measure of quality for linear multistep methods, it is appropriate to inspect the so-called local error being defined by

$$\varepsilon_k := \sum_{\sigma=0}^{s} \alpha_\sigma \tilde{\boldsymbol{v}}_{k-\sigma} - T\beta_\sigma \boldsymbol{C}^{-1} \tilde{\boldsymbol{i}}_{k-\sigma} \tag{5.7}$$

where $\alpha_0 := 1$ has been adopted. The goal for the design of a linear multistep method is to determine the free parameters in order to minimize the local error in a certain manner. To this end, we will again make use of steady-state quantities at a complex frequency p where $\tilde{\boldsymbol{V}}$, $\tilde{\boldsymbol{I}}$ and $\boldsymbol{E}$ denote the complex amplitudes of $\tilde{\boldsymbol{v}}$, $\tilde{\boldsymbol{i}}$ and ε, respectively. According to eq. (5.1), $\tilde{\boldsymbol{V}}$ and $\tilde{\boldsymbol{I}}$ are related to each other by $p\tilde{\boldsymbol{V}} = \boldsymbol{C}^{-1}\tilde{\boldsymbol{I}}$ and eq. (5.7) becomes

$$\boldsymbol{E} = \tilde{\boldsymbol{V}} \sum_{\sigma=0}^{s} (\alpha_\sigma - pT\beta_\sigma) \mathrm{e}^{-\sigma pT}. \tag{5.8}$$

Now, the sum is expanded into a MACLAURIN series with respect to pT. The parameters α_σ and β_σ are typically chosen so that as many as possible of the first terms of the MACLAURIN series vanish. In fact, we place as many as possible zeros at the origin in order to have a maximal flat

approximation of zero for the local error. If the multiplicity of this zero is $q+1$ then q is called the consistency order.

A suggestive method should have a bounded local error if pT tends towards zero. In view of eq. (5.8), the parameters have then to fulfill the relation

$$\sum_{\sigma=0}^{s} \alpha_\sigma = 0. \tag{5.9}$$

Next, let us make use of the LANDAU order symbol $\mathcal{O}$ in order to enable a condense formulation:

$$\sum_{\sigma=0}^{s} (\alpha_\sigma - pT\beta_\sigma)\mathrm{e}^{-\sigma pT} = \mathcal{O}((pT)^{q+1}). \tag{5.10}$$

Regardless of the steady-state considerations, the evaluation of this equation leads to the consistency equations being the same as for the classical approach, cf. [Felderhoff, 1994].

However, these consistency equations are somewhat bulky and, additionally, we have to determine the parameters of $Z(\psi)$ from the parameters of the difference equation. For these reasons, we will directly derive consistency equations formulated in dependence of the parameters c_σ and d_σ as appearing in eq. (5.6).

Primarily, we can state that for an irreducible method eq. (5.9) implies

$$\sum_{\sigma=0}^{s} \beta_\sigma \neq 0. \tag{5.11}$$

With regard to the equations (5.5) and (5.6), the relations (5.9) and (5.11) are equivalent to

$$d_0 = 0 \quad \text{and} \quad c_0 \neq 0\ . \tag{5.12}$$

Since c_0 cannot vanish and one coefficient of Z can be normalized, let us choose c_0 equal to one. Having this in mind, eq. (5.10) divided by the numerator polynomial of $\hat{Z}(\mathrm{e}^{pT})$ leads to

$$\frac{1}{\hat{Z}(\mathrm{e}^{pT})} - \frac{pT}{2} = \mathcal{O}((pT)^{q+1}).$$

Before we reformulate this equation in dependence of the complex equivalent frequency variable ψ, we will recall the MACLAURIN series of the artanh function:

$$\operatorname{artanh}(\psi) = \sum_{\mu=0}^{\infty} \frac{\psi^{2\mu+1}}{2\mu+1} \quad \text{for all } |\psi| < 1\ . \tag{5.13}$$

Now, we can state that a linear multistep method can be interpreted as a frequency transformation where $1/Z(\psi)$ approximates the artanh function:

$$\frac{1}{Z(\psi)} - \operatorname{artanh}(\psi) = \mathcal{O}(\psi^{q+1}). \tag{5.14}$$

Finally, we will make use of the concept of a PADÉ approximation in order to derive consistency conditions in dependence of c_σ and d_σ. For this purpose, we multiply eq. (5.14) with the numerator polynomial of $Z(\psi)$ where the right side remains unchanged because of $c_0 = 1$:

$$\sum_{\sigma=0}^{s} d_\sigma \psi^\sigma - \sum_{\mu=0}^{\infty} \frac{\psi^{2\mu+1}}{2\mu+1} \sum_{\sigma=0}^{s} c_\sigma \psi^\sigma = \delta_\varepsilon \psi^{q+1} + \mathcal{O}(\psi^{q+2})\ . \tag{5.15}$$

Here, the constant $\delta_\varepsilon \neq 0$ has been adopted which is designated as the local error constant. By comparing both sides of this equation, we obtain the sought formulation of the consistency conditions depending on the parameters of the characteristic impedance $Z(\psi)$ given in Table 1.

$q \geq 0$:	$d_0 = 0$
$q \geq 1$:	$d_1 = c_0 := 1$
$q \geq 2$:	$d_2 = c_1$
$q \geq 3$:	$d_3 = c_2 + c_0/3$
$q \geq 4$:	$d_4 = c_3 + c_1/3$
$q \geq 5$:	$d_5 = c_4 + c_2/3 + c_0/5$
$q \geq 6$:	$d_6 = c_5 + c_3/3 + c_1/5$
$\vdots$	$\vdots$

Table 1: Consistency conditions of linear multistep methods.

5.3 Maximum Consistency Order

Unfortunately, passive linear multistep methods possess a limited accuracy with respect to numerical integration. In order to show this, let us assume a linear multistep method having a consistency order $q \geq 1$. As a result, $Z(\psi)$ has a single pole with residue 1 in the origin which will be extracted now. Here, it is important to note that – for a passive linear multistep method – $Z(\psi)$ remains positive after extracting this pole. In other words,

$$Z'(\psi) := Z(\psi) - \frac{1}{\psi} = \frac{\sum_{\sigma=2}^{s} (c_{\sigma-1} - d_\sigma)\psi^{\sigma-2} + c_s\psi^{s-1}}{1 + \sum_{\sigma=2}^{s} d_\sigma\psi^{\sigma-1}}$$

also satisfies condition (3.21) under this assumption.

Altogether, the linear multistep method of least implementation effort is the trapezoidal rule having a characteristic impedance $Z(\psi) = 1/\psi$, compare Figs. 31 and 32. Due to its accuracy of $q = 2$, its local error constant of $-1/3$ with respect to ψ, and in particular its simple realization, this rule is customary used for wave digital structures, cf. Figure 32.

Except for the trapezoidal rule, linear multistep methods need more than one step in order to achieve a consistency order of at least two. If we focus on multistep methods with $s \geq 2$ only, we can realize that the consistency condition for $q \geq 2$ requires $d_2 = c_1$ or, according to $Z'(\psi)$,

$$Z'(0) = 0. \tag{5.16}$$

Finally, we examine the reciprocal value $Y' := 1/Z'$ having a pole in the origin with residue $1/(c_2 - d_3)$. Now, if the method is passive then Z' and consequently also Y' are positive functions. For this reason, it is necessary to have a positive residue for this pole, i. e.,

$$c_2 > d_3. \tag{5.17}$$

As a conclusion from Table 1, passive linear multistep methods cannot achieve a consistency order of three and their local error, $d_3 - c_2 - c_0/3$, has minimal magnitude for the trapezoidal rule.

Of course, this result is not new. Because passivity of a linear multistep method is equivalent to A-stability[4] [Felderhoff, 1994] the result in fact is well known as DAHLQUIST's second barrier [Dahlquist, 1963]. However, the line of arguments presented in this paper establishes yet another proof of this barrier, cf. [Genin, 1973, Grigorieff, 1977, Hairer and Wanner, 1996].

[4]This is in particular true for linear multistep methods, but for more general integration methods it can be shown that passivity is stronger than A-stability. A detailed discussion of some stability properties of passive RUNGE-KUTTA methods will be given elsewhere [Ochs, 2001, Fränken and Ochs, 2001].

6 Summary and Outlook

The paper presents an approach for the systematic synthesis of wave digital structures for given reference circuits. Based on our ideas, the synthesis of an optimum wave digital structure can be realized in $\mathcal{O}(n)$, where n denotes the number of elements in the corresponding reference circuit. The concepts presented here are exemplified for one-ports only; however, they can be transferred easily to the case of using multi-ports (see the Remarks on Page 27).

The paper recapitulates wave digital modeling and some fundamental properties. Special emphasis has been put on the generation of suited adaptor structures, which forms a crucial point during the WDS synthesis procedure. The method proposed here is based on the graph-theoretical concept of triconnected components playing a role in graph planarity tests and for which Hopcroft and Tarjan developed an efficient detection algorithm. Although their algorithm has been invented for a very different problem, it provides us with an efficient method for identifying the three elementary types of minimum independent subnetworks: parallel, series, and closely connected components, designated by capital letters S, P, and C respectively. The result of our structure synthesis algorithm is a special graph, called SPC-tree, which indicates the relationship between the aforementioned components.

The SPC-tree is a powerful representation of the topological interconnection structure allowing for a direct derivation of the adaptor structure. Moreover, it can be used for rule-based simplifications as well as for searching structural singularities.

Current and further research concentrates on the following aspects.

- Operationalization of the presented ideas in the form of a prototypic synthesis work bench for wave digital structures.
- Algorithms for a systematic detection of structural singularities.
- A library with predefined special adaptor structures occurring typically in electrical networks, such as bridged-T configurations.

References

L. Auslander and S. V. Parter. On Imbedding Graphs in the Plane. *Journal of Mathematics and Mechanics*, 10(3):517–523, May 1961.

Vitold Belevitch. *Classical network theory*. Holden-Day, San Francisco, 1968.

Heather Booth and Robert E. Tarjan. Finding the Minimum-Cost Maximum Flow in a Series-Parallel Network. *Journal of Algorithms*, 15:416–446, 1993.

Andreas Brandstaedt, Van Bang Le, and Jeremy P. Spinrad. *Graph Classes—A Survey*. Society for Industrial and Applied Mathematics, New York, 1999.

Francois E. Cellier. *Continuous System Modeling*. Springer, New York, 1991.

Germund Dahlquist. A special stability problem for linear multistep methods. *BIT*, 3:27–43, 1963.

B. de Fluiter. *Algorithms for Graphs of Small Treewidth*. Dissertation, University of Utrecht, Netherlands, 1997.

Thomas Felderhoff. A new approach to design A-stable linear multistep integration algorithms. *Proceedings of the IEEE International Symposium on Circuits and Systems*, 5:133–136, 1994.

Alfred Fettweis. Digital Filter Structures Related to Classical Filter Networks. *Archiv für Elektronik und Übertragungstechnik*, 25(2):79–89, 1971.

Alfred Fettweis. Wave digital filters: Theory and practice. *Proceedings of the IEEE*, 74(2): 270–327, February 1986.

Alfred Fettweis. Discrete passive modelling of viscous fluids. *Proceedings of the IEEE International Symposium on Circuits and Systems*, 4:1640–1643, 1992.

Alfred Fettweis and Gerald Hemetsberger. *Grundlagen der Theorie elektrischer Schaltungen*. Brockmeyer, 1995.

Hans Dieter Fischer. Wave digital filters for numerical integration. *NTZ Archiv*, 6(2):37–40, 1984.

Dietrich Fränken and Karlheinz Ochs. Synthesis and design of passive Runge-Kutta methods. Zur Veröffentlichung angenommen. *Archiv für Elektronik und Übertragungstechnik*, 2001.

Yves Genin. A new approach to the synthesis of stiffly stable linear multistep formulas. *IEEE Transactions on Circuit Theory*, 20(4):352–360, 1973.

Rolf Dieter Grigorieff. *Numerik gewöhnlicher Differentialgleichungen 2*. Teubner, Stuttgart, 1977.

Wolfgang Hahn. *Stability of Motion*. Springer, New York, 1967.

Ernst Hairer and Gerhard Wanner. *Solving Ordinary Differential Equations II*. Springer, New York, 1996.

J. E. Hopcroft and R. E. Tarjan. Dividing a Graph into Triconnected Components. *SIAM Journal of Computing*, 2(3):135–158, September 1973.

Dieter Jungnickel. *Graphen, Netzwerke und Algorithmen*. BI Wissenschaftsverlag, Wien, 1990. ISBN 3-411-14262-6.

Thomas Kailath. *Linear Systems*. Prentice-Hall, New Jersey, 1980.

Wolfgang Kowalk. *System, Modell, Programm*. Spektrum Akademischer Verlag, Heidelberg Berlin, 1996.

K. B. Kumar. Novel Techniques to Solve Sets of Coupled Differential Equations with SPICE. *IEEE Circuits and Devices Magazine*, 7:11–14, 1991.

Klaus Meerkötter. Beiträge zur Theorie der Wellendigitalfilter. Dissertation, Ruhr-Universität Bochum, 1979.

Klaus Meerkötter and Thomas Felderhoff. Simulation of nonlinear transmission lines by wave digital filter principles. *Proceedings of the IEEE International Symposium on Circuits and Systems*, 2:875–878, 1992.

Klaus Meerkötter and Reinhard Scholz. Digital simulation of nonlinear circuits by wave digital filter principles. *Proceedings of the IEEE International Symposium on Circuits and Systems*, pages 720–723, 1989.

E. E. L. Mitchell and J. S. Gauthier. Advanced Continuous Simulation Language (ACSL). *Simulation*, 25:72–78, 1976.

S. Mitchell Hedetniemi, E. J. Cockayne, and S. T. Hedetniemi. Linear Algorithms for Finding the Jordan Center and Path Center of a Tree. *Transportation Science*, 15:98–114, 1981.

Gunnar Nitsche. Numerische Lösung partieller Differentialgleichungen mit Hilfe von Wellendigitalfiltern. Dissertation, Ruhr-Universität Bochum, 1993.

Karlheinz Ochs. Passive Integration Methods: Fundamental Theory. *Archiv für Elektronik und Übertragungstechnik*, 55(3):153–163, 2001.

K. L. Paap, M. Dehlwisch, R. Jendges, and B. Klaaßen. Modeling Mixed Systems with SPICE3. *IEEE Circuits and Devices Magazine*, 9:7–11, 1993.

Linda Petzold. Differential/Algebraic Equations are not ODE's. *SIAM Journal on Numerical Analysis*, 3(3):277–385, September 1994.

André Schulz, Benno Stein, and Annett Kurzok. On the Automated Design of Technical Systems. Technical Report tr-ri-00-218, University of Paderborn, Department of Mathematics and Computer Science, June 2001.

Benno Stein. *Functional Models in Configuration Systems*. Dissertation, University of Paderborn, Institute of Computer Science, 1995.

Robert E. Tarjan. Depth-First Search and Linear Graph Algorithms. *SIAM Journal of Computing*, 1 (2):146–160, June 1972.

Robert E. Tarjan and J. Hopcroft. Finding the Triconnected Components of a Graph. Technical Report 140, Department of Computer Science, Cornell University, Ithaca, New York, 1972.

Rolf Unbehauen. *Grundlagen der Elektrotechnik 1*. Springer, Berlin NewYork, 1994.

M. Vidyasagar. *Nonlinear Systems Analysis*. Prentice-Hall, New Jersey, 1993.

J. Wallaschek. Modellierung und Simulation als Beitrag zur Verkürzung der Entwicklungszeiten mechatronischer Produkte. *VDI Berichte Nr. 1215*, pages 35–50, 1995.

P. E. Wellstead. *Physical System Modelling*. Academic Press Inc., London New York, 1979.