A Design and Implementation of 32-paths Parallel 256-Point FFT/IFFT for Optical OFDM Systems

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Abstract— **This paper presents the design and implementation of thirty-two paths parallel FFT/IFFT for optical OFDM systems. Employing OFDM over high speed optical transmission systems requires large hardware resources due to computational-intensive operations such as full-parallel FFT implementation. The proposed 256-point FFT/IFFT adopts 32-paths parallel architecture with mixed radix-2^3 and radix-2^5 algorithm to reduce large number of complex multipliers. With this architecture, 256 full parallel data signals can be divided into eight sequential groups. Each group, composed of 32 parallel signals, is pipeline- processed. As a result, the hardware resources for full parallel 256-point FFT operation can be reduced to as much as those of 32-point FFT resource plus 32-path 8-point single-path delay feedback (SDF). The proposed FFT architecture is implemented with field programmable gate array and integrated in 12 Gbps, 64-QAM encoded real-time optical OFDM system. The implementation result shows that an 86% complex multiplier reduction can be achieved in comparison with full parallel architecture. The attained error vector magnitude (EVM) is approximately up to -32 dB for 64-QAM OFDM signals.**

Keywords— **Fast Fourier Transform (FFT), Optical OFDM (Orthogonal Frequency Division Multiplexing), Single-path Delay Feedback (SDF)**

I. INTRODUCTION

To meet the rapid growth of internet traffic and increase of high bandwidth demand for optical networks, Optical Orthogonal Frequency Division Multiplexing (OOFDM) technology has been widely researched and developed in recent years. OFDM, as a multicarrier transmission technique, has several advantages of simple equalization, intolerant to dispersive fiber channel, spectral efficiency, and flexibility [1]. Since the modulation and demodulation in OFDM are achieved digitally with the aid of Inverse Fast Fourier Transform (IFFT) and FFT requiring high computational complexity, hardware-efficient implementation is very crucial for real-time realization of OOFDM system.

To realize FFT implementation for real-time OOFDM applications, experimental results and demonstrations using field programmable gate array (FPGA) have been reported, which are, however, obtained by adopting the full-parallel architecture. 32/128/256-point full-parallel decimation-in-time FFT are presented for intensity modulation, direct detection (IMDD) and coherent optical OFDM (CO-OFDM) applications [2-5]. Gokhan [4] reported full parallel a 256-point FFT processor for 100 Gbps applications, which uses radix-4 scheme to reduce complexity as well as maintaining high-speed data flow. For further complexity reduction, Schmogrow [5] proposed IFFT implementation using precomputed IFFT values with lookup tables. But its method could not be applied to FFT operation because of not being able to precompute receive signal in advance. In addition, its applicability is limited since its complexity grows as the number of QAM level and FFT points increase. From all these studies, full parallel architecture has been adopted, resulting in low speed internal clock operation, to meet excessive data rate demands at the cost of higher logic consumption. However, considering current state of the art FPGA devices has enough marginal slack of operation speed, there needs to adopt FFT architecture with smaller paths. Thus we propose 32-paths parallel 256-point FFT architecture to reduce logic resources for real-time realization of OOFDM systems.

The rest of paper is organized as follows: Section II describes the mathematical formulations of the 32-paths 256-point FFT algorithm. Section III gives the proposed FFT architecture and hardware complexity. And explains implementation and test results under the environment of optical OFDM experiment, and finally conclusion follows in Section IV.

II. 32-PATHS 256-POINT FFT DESIGN

To derive a 32-paths 256-point decimation-in-frequency (DIF) FFT mathematical formulation, Cooley-Turkey (CT) algorithm firstly is applied to FFT equation [6]. Given a length N complex input sequence $x(n)$, N-point FFT equation is given in (1) where n represents a discrete time-domain index, k is a discrete frequency index, and $W_N^{nk} = e^{-j2\pi\frac{nk}{N}}$ is the twiddle factor (TF).

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk} \tag{1}$$

N-point FFT can be divided into two smaller FFT, as represented in (2), by applying CT algorithm to (1) with conditions of $N\ N_1 \cdot N_2 = 8 \cdot 32, n = r + qN_2, r = 0,..,N_2 - 1$, and $k = l + mN_1, l = 0,..,N_1 - 1$. Mixed radix-$2^3$ and radix-2^5 form can be obtained by using that $n = 2^{v-1} \cdot n_1 + 2^{v-2} \cdot n_2 + \cdots + n_v$ and $k = k_1 + 2 \cdot k_2 + \cdots + 2^{v-1} \cdot k_v$, where $v = log_2 N$.

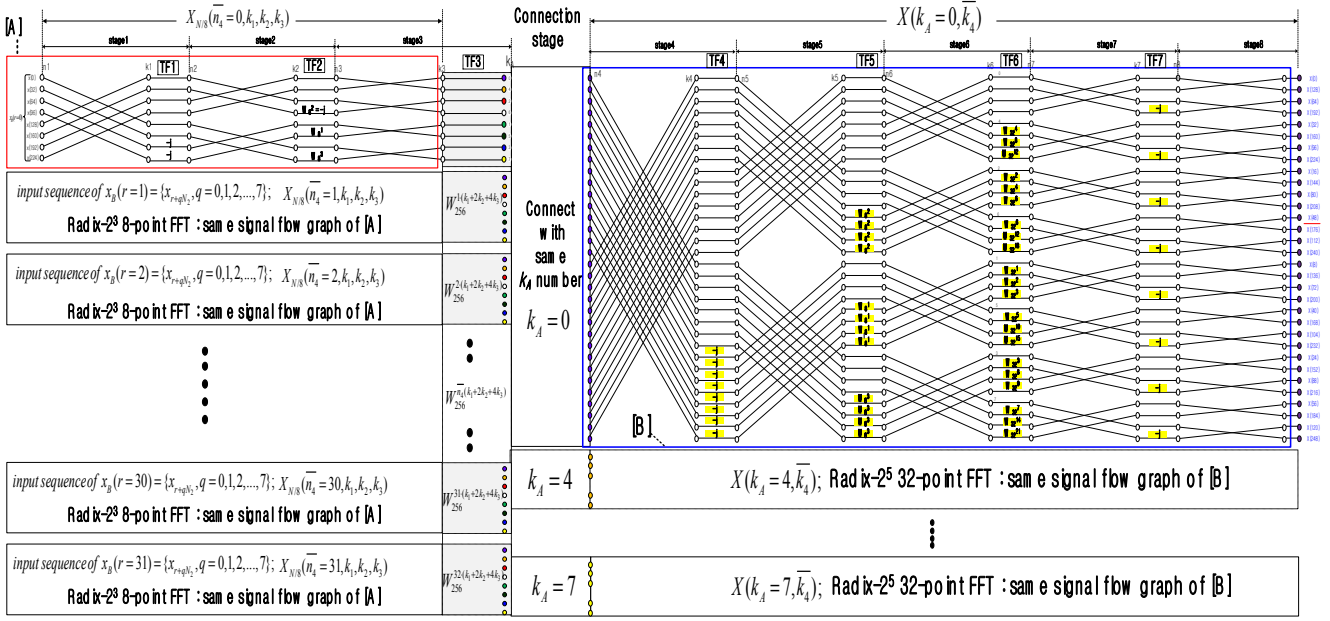


Figure 1. Signal flow graph of mixed radix-2^3 and radix-2^5 256-point FFT

$$X_{mN_1+l} = \underbrace{\sum_{r=0}^{N_2-1}\left[\left\{W_N^{rl}\underbrace{\left[\sum_{q=0}^{N_1-1} x_{r+qN_2} W_{N_1}^{lq}\right]}_{N_1\text{-point DFTs}}\right\} W_{N_2}^{mr}\right]}_{N_2\text{-point DFTs}} \quad (2)$$

For radix-2^3 N_1-point DIF, rewriting the index n and k as ($n = \frac{N}{2}n_1 + \frac{N}{4}n_2 + \frac{N}{8}n_3 + \overline{n_4} = n_A + \overline{n_4}$; $n_1 = n_2 = n_3 = 0,1$; $\overline{n_4} = 0,1,2,\ldots,\frac{N}{8}-1$;) and ($k = k_1 + 2k_2 + 4k_3 + 8\overline{k_4} = k_A + \overline{k_4}$; $k_1 = k_2 = k_3 = 0,1$; $\overline{k_4} = 0,1,2,\ldots,\frac{N}{8}-1$;) , respectively, (2) becomes

$$X(k_A + \overline{k_4}) = \sum_{n_4=0}^{31}\sum_{n_3=0}^{1}\sum_{n_2=0}^{1}\sum_{n_1=0}^{1} x\left(n_A + \overline{n_4}\right) W_N^{(n)(k)}$$
$$= \sum_{n_4=0}^{31}\left\{\left[X_{N/8}(\overline{n_4}, k_1, k_2, k_3)\right] W_N^{\overline{n_4}k_A} W_{N/8}^{\overline{n_4}\overline{k_4}}\right\},$$
$$where\ X_{N/8}(\overline{n_4}, k_1, k_2, k_3) = \quad (3)$$
$$\left(\sum_{n_3=0}^{1}\left(\sum_{n_2=0}^{1}\left(\sum_{n_1=0}^{1} x\left(n_A + \overline{n_4}\right) W_2^{n_1 k_1}\right) W_4^{n_2 k_1} W_2^{n_2 k_2}\right) W_8^{n_3(2k_2+k1)} W_2^{n_3 k_3}\right)$$

From (3), $X_{8/N}$ of (3) can be expressed as 2^3-radix 8-point FFT with $TF1 = W_4^{n_2 k_1}$ and $TF2 = W_8^{n_3(2k_2+k_1)}$, where TF1 is twiddle factor of stage1, TF2 for stage2. And $X(k_A + \overline{k_4})$ is composed of thirty-two $X_{8/N}$ and eight 32-point FFT, in which the twiddle factors of $W_N^{\overline{n_4}k_A}$ are multiplied between $X_{8/N}$ and 32-point FFTs. For further decomposition of 32-point FFT into radix-2^5 form, similar procedures can be applied by replacing $\overline{k_4} = k_4 + 2k_5 + 4k_6 + 8k_7 + 16k_8$ and ($\overline{n_4} = \frac{32}{2}n_4 + \frac{32}{4}n_5 + \frac{32}{8}n_6 + \frac{32}{16}n_7 + \frac{32}{32}n_8$). Thus, (3) can be rewritten as

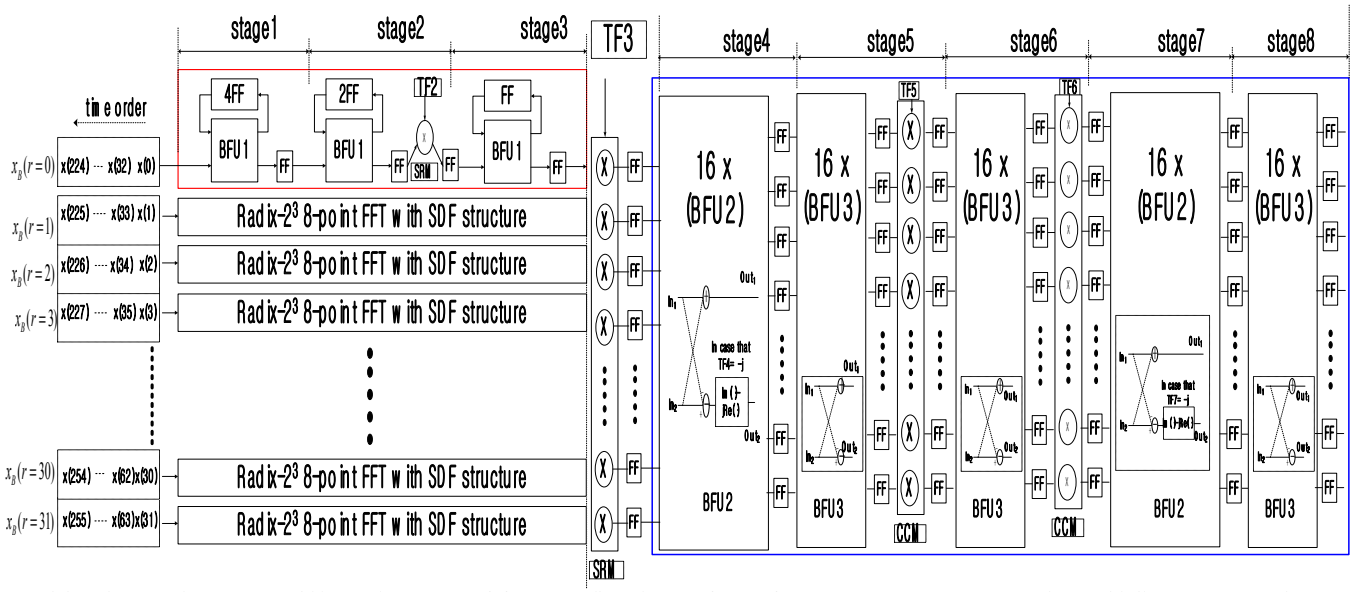
$$X(k_1 + 2k_2 + 4k_3 + 8k_4 + 16k_5 + 32k_6 + 64k_7 + 128k_8)$$
$$= \sum_{n_8=0}^{1}\sum_{n_7=0}^{1}\sum_{n_6=0}^{1}\sum_{n_5=0}^{1}\sum_{n_4=0}^{1}\left\{\left[D_{N/8}(\overline{n_4}, k_1, k_2, k_3,)\right] W_{N/8}^{\overline{n_4}\overline{k_4}}\right\} \quad (4).$$
$$where\ D_{N/8}(\overline{n_4}, k_1, k_2, k_3) = X_{N/8}(\overline{n_4}, k_1, k_2, k_3) W_N^{\overline{n_4}k_A}$$

By evaluating $W_{N/8}^{\overline{n_4}\cdot\overline{k_4}} = W_{N/8}^{(16n_4+8n_5+4n_6+2n_7+n_8)(k_4+2k_5+4k_6+8k_7+16k_8)}$, equation (4) can be express as

$$(4) = D_{N/128}(0) + \underbrace{W_4^{k_7}}_{TF7} \cdot D_{N/128}(1) \cdot W_2^{k_8}, where$$
$$\begin{cases} D_{N/128}(n) = D_{N/64}(n) + \underbrace{W_{32}^{(4k_6+2k_5+k_4)}}_{TF6} \cdot D_{N/64}(n + \frac{N}{128}) \cdot W_2^{k_7}, \\ D_{N/64}(n) = D_{N/32}(n) + \underbrace{W_8^{(2k_5+k_4)}}_{TF5} \cdot D_{N/32}(n + \frac{N}{64}) \cdot W_2^{k_6}, \\ D_{N/32}(n) = D_{N/16}(n) + \underbrace{W_4^{(k_4)}}_{TF4} \cdot D_{N/16}(n + \frac{N}{32}) \cdot W_2^{k_5}, \end{cases} \quad (5),$$

By considering (3) and (5), we can decompose the 256-point FFT into an 8-point FFT and a 32-point FFT in which are implemented radix-2^3 and radix-2^5 algorithm.

Signal flow graph (SFG) of a 256-point FFT algorithm, as shown in figure 1, represents that $X_{N/8}(\overline{n_4}, k_1, k_2, k_3)$ has the same 8-point FFT structure for input sequence of $x_B(r)|_{r=0,1,\ldots 31} = \{x_{r+qN_2}, q = 0,1,\ldots,7\}$. In addition, it shows that $X(k_A + \overline{k_4})$ for each value of k_A has the same SFG.



FF: delay elements for SDF (ex: shifter register), BFU1/2/3: Butter-fly unit type-I/type-II/type-III, CCM: Constant Complex Multiplier, SRM: Complex Multiplier with strength reduction transformation.

Figure 2. Architecture of the proposed 32-paths parallel 256-point FFT

Therefore, if we break input sequence *x(n)* into $x_B(r)|_{r=0,1,\dots 31}$ groups and multiply TF3 in accordance with $X_{N/8}(\overline{n_4}, k_1 k_2 k_3)$, a full parallel 256-point FFT can be processed with only one 8-point FFT and a 32-point FFT, which results in reducing hardware resources.

Inverse FFT calculation can be performed by swapping the real and imaginary parts of input sequence, taking forward FFT, and swapping real and imaginary parts of FFT's results [7].

III. Implementation and Experimental Results

In this section, we describe 32-paths parallel 256-point FFT architecture based on the SGF in section II. A full parallel 256-point FFT can be processed sequentially if $X_{N/8}(\overline{n_4}, k_1 k_2 k_3)$ are implemented with single-delay path feedback (SDF) units [8]. In this case input sequences of $x_B(r)$ is performed as an 8-point FFT operation. The proposed architecture, as shown in figure 2, consists of thirty-two 8-point SDF blocks, twiddle factor of TF3, and a 32-point FFT block in which contains sixteen butterfly units (BFU1, BUF2 and BFU3), constant complex multipliers (CCM), complex multiplier with strength reduction transformation (SRM), and delay elements such as flip-flop (FF). Non-trivial complex multipliers in this architecture are exploited in TF2, TF3, TF5 and TF6, while other TFs are –j multiplication resulting in exchange between real and imaginary parts. Since TF2 and TF3 vary depending on the sequence order q and r of $x_B(r) = x(q+32r)$, variable complex multipliers with strength reduction are used. The total number of real multiplications is reduced to only three for one complex multiplication [9]. CCM in TF5 and TF6 can be made with shift and add operations. Butterfly unit type-I (BFU1), as depicted in figure 3, carries out complex addition and subtraction by controlling the switch to make them work in a serial way [10]. BFU2 in figure 2 shows the butterfly structure with –j multiplication which is performed in stage 4 and stage 7. BFU3 is a conventional radix-2 butterfly.

Table 1 summarizes complexities in the proposed architecture. Assuming full parallel architecture is implemented with radix-2 form, the proposed architecture has an 86% complex multiplier reduction, an 80 % of complex adders, and a 76% of complex registers in comparison with full parallel architecture. On the other hand, operating clock rate requires eight times of full-parallel-architecture's one. Thus the proposed architecture accomplishes high reduction of complexities unless clock rate is constrained.

TABLE 1. Complexity summary of the proposed architecture

	The proposed architecture	Full parallel architecture
No. of constant complex multipliers (CCMs)	28	642
No. of variable complex multipliers (SRMs)	63	0
No. of butterflies (BFs)	186	1024
No. of complex adders	2x186 = 392	2048
No. of complex registers for SDFs	224	0
No. of complex registers for pipelining	256	2048
Throughput rate (R : clock rate)	8R	R

Fixed point simulation using SPW and Matlab is done to acquire bit accuracies of FFT. The word length of input and output of each stage is 12 bits. Different bit size processed internally in each stage. Twiddle factor bits are also 12 bits. The acquired SQNR is approximately up to 45 dB. Based on the word length chosen, the FFT architecture was simulated with VHDL and ModelSim simulator. And the proposed architecture is implemented with Xilinx FPGA - XC7K480T.

TABLE 1. COMPASION OF THE PROPOSED WITH EXISTING RESULTS FOR OPTICAL OFDM

	The proposed architecture	Gokan Polat et al. [5]	Beril Inan et al. [4] [(b)]	R. Schmogrow et al. [3] [(b)]
Architecture	32-paths mixed radix-2^3 and radix-2^5	Full parallel Radix-4	Full parallel	Full parallel (precomputed IFFT using LUTs)
No. of FFT points	256	256	1024	64
Word length [bits]	(input: 12), (output: 12)	(input: 5), (output: -)	(input: 5), (output: 10)	(input: -), (output: -)
QAM Levels	64-QAM	- [(a)]	4-QAM	16-QAM
Used FPGA devices	XC7K480T-2	XC6VHX565T-2	XC5VFX200T [11] (2 devices)	XC5VFX200T (2 devices)
Number of Slice LUTs	87,209	213,700	172,032	152,371
Number of Registers	28,806	123,406	203,980	164,659
Number of DSP	0	0	630	0
Block RAM	0	0	3612 Kb	0
Operating clock rate (Max.)	219.546 MHz	335.914 MHz	-	-
Error Vector Magnitude(EVM)	-32 dB (2.5%)	-	-	-19.72 dB (11%)
(notes) (a) '-'means no record in the reference paper. (b) Considering that one slice contains 4 LUTs and 4 registers, numbers of used resources are calculated from the utilization percentage per one device written in [4] and [3].				

Table 2 shows the implementation results and comparison of the existing ones. The utilization factor is found to be 4% of slice registers and 29% of slice LUTs available. In spite of wider word-length and higher modulation levels, it is shown that the proposed FFT processor consumes less hardware resources than the previous works. Table 2 indicates that the proposed 256-point FFT architecture is hardware-efficient and thus appropriate to high-speed OOFDM applications. Experimentally, OOFDM transmitter using the proposed FFT works with 10 bits digital-to-analog converter (DAC) running at 4 GS/s, which results in an aggregate line rate of 12 Gbit/s. Figure 3 illustrates the experimental results of constellations (a), EVM per subcarrier (b), frequency spectrum (c), and demodulation information (d), respectively. Average EVM of approximately 32 dB is obtained for 64-QAM modulation.

IV. CONCLUSIONS

In this paper, we proposed 32-paths parallel 256-point FFT architecture by applying the mixed radix-2^3 and radix-2^5 algorithm. The proposed FFT processor proved that it significantly reduce hardware complexities through the FPGA design and implementation. And also we confirmed experimentally that it can be used for OOFDM systems requiring excessive data rates. For further studies, we need to investigate on more sophisticated multiplier structures for additional optimizations.

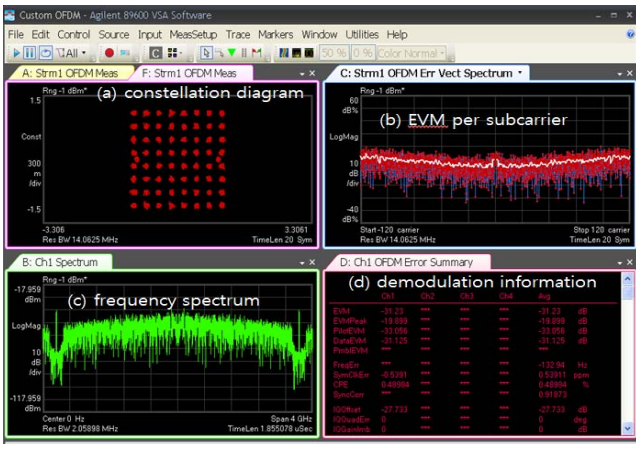


Figure 3. Experimental results using the proposed FFT architecture

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