Guest Editors' Introduction

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1 INTRODUCTION

It is with great pleasure that we introduce the special issue on Defect Tolerance of Digital Systems to the readership of the *IEEE Transactions on Computers*. It consists of six papers that have been selected from a large number of submitted manuscripts; each paper has undergone a rather extensive review process such that many good submissions were not accommodated in this issue.

The last decade has seen an explosive growth in techniques for attaining defect tolerance in the manufacturing and operation of complex digital systems. Tolerance to defects is substantially different from the commonly established practice of fault-tolerant computing. Defects are physically based events which result from faults in the physical design and manufacturing of systems using advanced technologies; the rapid acceleration in the decrease of device geometries (as encountered in deep submicron VLSI) and the large costs involved in developing high density systems (such as the much heralded system-on-a-chip) have encountered significant practical problems such as yield reduction, incomplete coverage of defects/faults, and lack of tools. Defect tolerance has been advocated both in industry and academia as a possible solution to some of these problems. Defect tolerance must however fulfill high expectations; in particular, issues such as redundancy costs, area overhead, and performance are still widely debated. There is considerable difference between theory and implementation, thus suggesting that a large volume of investigation is still needed.

The first paper of this special issue is "Incorporating Yield Enhancement into the Floorplanning Process" by I. Koren and Z. Koren This paper deals with the important issues related to floorplanning and its relation to yield. Yield enhancement is analyzed with respect to different trade-offs involving routing complexity and its minimization. This is approached as a multiobjective minimization problem by considering different sensitivities to defects within a chip. A construction algorithm which integrates yield into the process of generating a floorplan, with reduced wiring cost by placement, is presented in detail. A yield fitness function is introduced in the floorplanning algorithm to incorporate yield enhancement in a comprehensive fashion and to make it computationally efficient.

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Two distinct objectives (total wiring length minimization and yield maximization) are studied using numerous examples of VLSI chips. The first type of chip consists of modules with very different defect sensitivities, while the second type includes chips with redundant modules. It is proven that the yield and wiring cost objectives are often conflicting. A set of Pareto-optimal solutions allowing consideration of the trade-off and the selection of one of the solutions, according to the relative importance of each of the objectives, are introduced very elegantly.

The next two papers address a rather classic problem in defect tolerance, namely the configuration of array systems is extensively analyzed with respect to yield enhancement by reconfiguring in the presence of defective processors.

Horita and Takanami, in the paper "Fault-Tolerant Processor Arrays Based on $1\frac{1}{2}$-Track Switch with Flexible Spare Distributions," address the issue of two-dimensional array reconfiguration in the presence of failures in the processors. This is particularly advantageous in the modular design of large parallel systems for high performance computing. The conditions for reconfigurability are fully analyzed and are based on the concept of covering paths by introducing novel routing procedures.

The proposed model has the property that physical distances between logically adjacent processors in the reconfigured array are within a constant that is independent of size. While hardware overhead is slightly more than the original $1\frac{1}{2}$ track switch model, the yield of the proposed model is significantly better. Novel distributions for spare placement are proposed for improvement in yield and reduced degradation of interprocessor delay in the reconfigured array. In particular, an allocation policy, which places spares along the main diagonal, is proposed to enhance the probability of reconfiguration; additional switches are required around each processor to permit routing of the connections once it is diagnosed as faulty.

C.-P. Low, in his paper "An Efficient Reconfiguration Algorithm for Degradable VLSI/WSI Arrays," considers a different aspect of reconfiguration. This consists of harvesting an array (target) of size different from the original one in the presence of defective processors, hence a possible degradation can be encountered. Under the constraint of row and column rerouting, it is shown that a special instance of this problem can be solved optimally in linear time using greedy criteria. The general problem addressed is also greedy, albeit no optimality can be guaranteed to its NP-completeness. An extensive analysis is provided to show that the target array is indeed very near in size com-

pared with the theoretical maximum and the harvesting rate using this technique is superior to existing works on this topic.

The next two papers of this special issue deal with testing of multiple faults with the specific objective of achieving diagnosis, i.e., faults are detected, located, and characterized such that corrective actions (such as repair) can take place to return the system to its original fault-free state.

Metra, Ricco, and Favalli are the authors of the first paper on this topic (titled "Self-Checking Detection and Diagnosis Scheme for Transient, Delay, and Crosstalk Faults Affecting Bus Lines"). This paper presents a comprehensive analysis of a wide set of faults/defects for bus lines. Faults that are likely to result in the connected sampling bus data are on-line detected, while identification and proper encoding of the position of the affected line are fully and efficiently met. A realistic fault analysis is pursued for on-line detection by taking into account the fault sensitivity/tolerance levels.

The proposed scheme is very fast, requires low area overhead, makes diagnosis possible, and does not require static power consumption. The additional bus load due to the proposed scheme is negligible compared to general data bus loads, thus minimally affecting speed of the system-under-test. Electrical level simulation results are reported for a possible VLSI implementation of the scheme. The proposed technique is applicable to custom and semicustom VLSI manufactured using su-micron technology, as well as to FPGAs.

In the next paper, "On the Adaptation of the Viterbi Algorithm for Diagnosis of Multiple Bridging Faults" by C. Thibeault, a new current-based method is proposed, having the advantage of general applicability in spite of technology scaling. This method uses differential Iddq probabilistic signatures together with a modified version of the Viterbi algorithm, as commonly used for error correction in communication systems. It departs significantly from today's practice of using a maximum likelihood estimation, thus permitting in most cases an accurate diagnosis of multiple bridging faults. As diagnosis relies on both fault identification and fault location, a list is utilized in matching measured results (obtained through experiments) to possible faults. In this work, the author shows that the values of the parasitic contact causing a bridging fault, as well as the load of the nodes involved in such a fault, have a limited effect on the rank of the list when more than a fault are considered. The proposed technique is robust with respect to Gaussian noise, thus showing its potential applicability to deep-submicron CMOS technology and its increased sub-threshold current.

The last paper describes an application of a defect tolerant technique to arithmetic division. In the paper "Fault Tolerant Newton-Raphson and Goldschmidt Dividers Using Time-Shared TMR," Gallagher and Swartzlander propose a concurrent error correction technique based on a combined time-shared triple modular redundancy arrangement. This technique has been applied to two commonly used dividers (Newton-Raphson and Goldschmidt's) in the multiplier implementation. Both hardware overhead and fault latency are analyzed as figures of merit. The objective of concurrent fault correction is achieved by considering different redundancy arrangements (employing time and space) in the basic multiplication step of the division process; in particular, lower precision on the early iterations of the multiplication is proposed as a solution to produce a low area overhead. This is significantly lower than raw triplication for immediate voting. First, the multiplier is divided into thirds, then, the rest of the divider is replicated around each smaller multiplier. Appropriate routing and feedback logic must be added so that multiplies can be completed over three cycles instead of one. A voter is provided for the outputs of the dividers so that erroneous values are concurrently corrected. All circuitry for division lies behind the voters, so failures in all parts of the redundant divider (except the voter) can be corrected; if the voter is self-checking, then failure of the voter can be detected, though not corrected.

The impact on performance and, specifically, on multiplication due to the time redundancy is reduced by routing and storing data in read-only memory devices; the dominance of multiplication on cycle time is further analyzed by evaluating the latency with respect to precision. A comprehensive treatment of the arithmetic involved in this process is pursued to substantiate the validity of this technique.

We sincerely hope that you enjoy reading this special issue; the contributions are significant and timely. In conclusion, we would like to thank all authors, reviewers, and staff members for making this issue a reality. We would also like to recognize Prof. Jane Liu, former Editor-in-Chief, and Prof. Jean-Luc Gaudiot, current Editor-in-Chief, for allowing this issue to be included in an archival journal of this stature.

Please feel free to contact us if you have questions or comments.

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Fabrizio Lombardi graduated in 1977 from the University of Essex, United Kingdom, with a BSc (Hons.) in electronic engineering. In 1977, he joined the Microwave Research Unit at University College London, where he received the Master in Microwaves and Modern Optics (1978), the Diploma in Microwave Engineering (1978), and the PhD from the University of London (1982). He is currently the chairperson of the Department of Electrical and Computer Engineering and holder of the International Test Conference (ITC) Endowed Professorship at Northeastern University, Boston. Prior to this, he was a faculty member at Texas Tech University, the University of Colorado-Boulder, and Texas A&M University. He has received many professional awards including the visiting fellowship at the British Columbia Advanced System Institute, University of Victoria, Canada (1988), the TEES Research Fellowship twice (1991-1992, 1997-1998), the Halliburton Professorship (1995), and an International Research Award from the Ministry of Science and Education of Japan (1993-1999). Dr. Lombardi was the recipient of the 1985/86 Research Initiation Award from the IEEE/Engineering Foundation, a Silver Quill Award from Motorola-Austin (1996), and was a distinguished visitor of the IEEE Computer Society for the period 1990-1993. He is an editor of the *IEEE Transactions on Computers*. He has been involved in organizing many international symposia, conferences, and workshops sponsored by organizations such as NATO and IEEE, as well as a guest editor in archival journals and magazines such as the *IEEE Transactions on Computers*, *IEEE Micro*, and *IEEE Design & Test*. His research interests are fault-tolerant computing, testing and design of digital systems, configurable computing, defect tolerance, and CAD VLSI. He has extensively published in these areas and has edited six books.

Mariagiovanna Sami graduated in electronic engineering from the Politecnico di Milano in 1966, in 1971, she received her Libera Docenza in "Switching Theory and Computers." From 1970 to 1980, she was an associate professor at the Politecnico di Milano; she has been a full professor there since 1980. She was chairperson of the Department of Electronics at the Politecnico di Milano from 1987-1990 and she is currently chairperson of the University Library System and the Rector's Delegate for Innovative Didactic Initiatives. She has received a number of professional awards in her career. Her research interests focus on VLSI testing, design of self-checking and fault-tolerant VLSI architectures, and design of high-performance processing systems. She has published more than 150 papers on these subjects, as well as one book and chapters in other books, and has edited five books. She is a senior member of the IEEE and has been involved as general chair, organizing chair, or program chair of a number of international conferences and workshops sponsored by organizations such as the IEEE and Euromicro, as well as two schools sponsored by NATO. She has been an associate editor of *IEEE Design and Test* and *IEEE Transactions on Computers*, a member of the advisory board of *Computer*, and editor-in-chief of the *Journal of Systems Architecture*. She is an associate editor of the *Journal on Electronic Testing, Theory, and Applications* (*JETTA*).