Guest Editors' Introduction: Board Test

Monica Lobetti-Bodoni
Siemens Mobile Communications

R.G. (Ben) Bennetts
Bennetts Associates

■ **MODERN, LOADED-BOARD** assemblies are multilayer constructions, heavily populated by under-the-package bonded devices such as micro ball grid, column grid, and flip-chip arrays. Such boards offer very limited physical access to traditional, in-circuit bed-of-nail testers. Other test issues include defects in buried components; higher operating frequencies than earlier boards, which lower the tolerances on signal integrity; lower power supply voltages; the need for more-accurate thermal analysis; and electromagnetic compatibility. Many systems companies are struggling to design new boards that support prototype board debugging (design verification and defect analysis), manufacturing test for volume production (defect detection and location), systems integration (backplane testing), and field service (fast fault identification and repair).

One solution is to develop ad hoc DFT methodologies that return the board-testing problem to the earliest phase of board development. This implies the development of new DFT techniques, skills, competence centers, methodologies, and organizations.

The First IEEE Board Test Workshop (BTW), held in Baltimore during the 2002 International Test Conference's Test Week, targeted these problems and provided a forum to discuss possible solutions. The workshop's success in terms of papers and audience participation reflected a renewed interest in board test issues. This special issue presents the best from this workshop.

This special issue

We selected four articles based on the content and quality of the original BTW 2002 papers, the discussion arising during the presentations, and the audience votes. The authors have updated the articles since their presentation at BTW 2002. In some cases, the work described might still be incomplete, and the solution not 100% proven. However, this is the nature of papers presented at a workshop, as opposed to those presented at a conference.

The first article, by Erik Jan Marinissen et al. (Philips Research Laboratories), addresses the problem of ground bounce on a board containing boundary scan devices compliant with IEEE Std. 1149.1, when all devices are in full external-test mode. Ground bounce is the phenomenon of shifting power and ground voltage levels that arises when too many transistors switch state simultaneously. In board-level boundary scan for interconnect tests based on using the EXTEST instruction, ground bounce can occur if the total number of boundary scan cell transitions between consecutive interconnect tests rises above a certain limit, called the simultaneous switching output limit (SSOL). Automatic pattern generators reduce the number of SSOs to the SSOL by inserting additional bridging tests. This article explores the theoretical solution to the question of what the minimum number of additional tests to satisfy a given SSOL constraint is. The authors liken the question to the well-known traveling-salesman problem, and they present several solutions based on exploiting the various degrees of freedom in the pattern generation process for the interconnect.

In the second article, Brad Van Treuren and Jose Miranda (Lucent Technologies) address the adoption of boundary scan as an embedded-test method for high-complexity systems; it allows a profitable separation of the test generation and test execution phases. Using Lucent proprietary software and commercially available hardware, the authors reapply a boundary scan test program generated for a single board to the same board mounted on a backplane. In typical Lucent architectures for telecommunications applications, an IEEE-1149.1-compliant multidrop test bus activates test execution for each system board using procedures described in Lucent's Test Flow Control Language. The embedded-test methodology can accommodate various types of traditional tests (such as boundary scan for interconnect test and in-system configuration), and can

adapt to new methods such as on-board built-in self-test (BIST), in which an embedded engine performs the test program execution.

Still on the subject of complex boards, especially when physical access is extremely limited, the authors of the third article, Mahnaz Salamati and Dag Stranneby (Orebro University) propose a nonintrusive method of test. Their method centers on measuring the electromagnetic field associated with the unit under test (UUT) during various operating modes. The method compares an electromagnetic signature generated by a set of connectionless probe configurations with a prestored reference signature. The best results come from UUTs that contain RF components, because the operating frequencies are known. If the UUT is densely populated with digital devices, there is a risk of aliasing between a known-good UUT and a faulty one. The article discusses the use of filters to reduce this risk. The connectionless test method can be effective for both defect detection and location, providing a visual, spatial localization of the defect.

The early availability of IEEE-1149.1-compliant devices assisted the commercial acceptance of the original 1990 version of the IEEE 1149.1 boundary scan standard. However, limited availability of commercial compliant devices is hampering commercial acceptance of the new IEEE 1149.4 mixed-signal standard. In addition, mixed-signal designers face the difficulties of designing a proper test infrastructure that allows the application of simple test procedures with high diagnostic capabilities. In the fourth article, Uroš Kač et al. (Jozef Stefan Institute and LIRMM) discuss the experimental implementation of an IEEE-1149.4-compliant device, including some feature extensions. Their design relies on an analog boundary scan cell extension and the definition of additional instructions. These instructions can isolate some areas of the design (switching architecture) according to the type of test to be applied. The authors claim their approach is efficient because it simplifies the IEEE 1149.4 design without reducing coverage, allows high diagnostic capabilities, and supports the development and application of functional tests.

ITC panel on test coverage

During BTW 2002, Ken Parker of Agilent Technologies organized and moderated a panel with the topic, "Board test coverage: Is it broken?" Earlier in the week, Ken had presented a paper on this hot topic at ITC.[1]

The panelists (C.J. Clark of Intellitech, Bill Eklow of Cisco Systems, Bill Follis of Agilent Technologies, Carlos O'Farrill of Jabil Circuit, and Bernard Sutton of Teradyne) focused on the need for a standard way of defining the proper fault model and measuring the corresponding fault coverage, both for a single step based on a single test technique (for example, optical inspection) and for a mixture of test techniques applied in several steps (optical inspection followed by x-ray inspection and in-circuit test). Having a standard way of defining and measuring coverage for these techniques would help identify the best test technique combination and minimize the overlap of different techniques. Each test technique's overlapping contributions prevent test engineers from actually seeing what the aggregate contribution of the sum of tests is and what is left to test.

The main drawback of the lack of a comprehensive metric is that test strategies tend to become very ad hoc, manual, and inaccurate. This makes it impossible to answer questions such as the following: How do I increase the defect coverage in one afternoon? What area of the board should I investigate to improve defect coverage? Can my coverage data tell me the exact location of defects on my field returns? Where is the source of a test escape?

Nevertheless, the ultimate reason for playing with coverage is to increase true board yield and the accuracy of yield prediction. In fact, yield relates to the test coverage and to the probability that a defect will occur.[2] The cost of not finding each defect as it moves through the manufacturing process is also part of the equation.

For nonassembly defects—such as crosstalk, jitter, noise, and interconnect delays—embedded test (based on BIST in the silicon) might be one possible solution, but a more structured approach involves providing strict adherence to DFT rules. DFT serves to provide physical, visual, and virtual access. The following formula provides a simple way to calculate defect coverage:

Defect Coverage = (Total Available Access – Access Constraints)/Total Available Access.

Finally, the panelists addressed some questions about the role of functional test: Can functional test provide measurable defect coverage? Does functional test solve coverage problems in specific board areas, complementing other test methods? The conclusion was that test engineers need new coverage metrics that work across technology boundaries—that is, for aggregate coverage when using functional and traditional structural tests—plus new technologies in various combina-

tions. The problem then is to extract meaningful and actionable information from the resulting sea of data.

Enjoy this special issue on board test. ∎

∎ References

1. K. Hird, K.P. Parker, and B. Follis, "Test Coverage: What Does It Mean When a Board Test Passes?" *Proc. Int'l Test Conf.* (ITC 02), IEEE Press, 2002, pp. 1066-1074.
2. B. Davis, *The Economics of Automatic Test*, McGraw-Hill, 1982.

Monica Lobetti-Bodoni is a DFT and test engineer at Siemens Mobile Communications. Her research interests include ASIC and PCB test, with an emphasis on defining a test methodology and providing the tools, training, and support required for the chosen strategy's application. Lobetti-Bodoni has an MSc in nuclear engineering and a master in information technology, both from Politecnico of Milan, Italy. She is a member of the IEEE and the Board Test Action Group for ITC's Test Week, and was chair of BTW 2002.

R.G. (Ben) Bennetts is an independent DFT consultant and teaches on-site educational courses about DFT technologies. His research interests include DFT strategies for the electronic-product life cycle and DFT technologies at chip, board, and system levels. Bennetts has a BS in aeronautical engineering from Farnborough Technical College; and an MS in electronics and a PhD in computer science, both from Southampton University. He is an advisory member of ASSET InterTech Inc.'s board of directors and Teseda Corp.'s technical advisory board.

∎ Direct questions and comments about this special issue to R.G. (Ben) Bennetts, Bennetts Associates, Burridge Farm, Burridge, Southampton, SO31 1BY, UK; ben@dft.co.uk.

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