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Evaluation of Current Control Structures for Multi-Phase Interleaved DC-DC Converters

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ABSTRACT Several current control concepts for non-isolated interleaved DC-DC converters are systematically evaluated in terms of their dynamic and steady state performance, based on defined performance evaluation indicators. Various current control structures suitable for multi-phase interleaved systems are studied: i) a conventional PI controller with a single update per switching period, ii) a PI controller with a fast execution rate, equal to the sampling frequency instead of the switching frequency iii) a LQR-based state feedback controller (SFC), iv) a model predictive controller (MPC), and v) an adaptive hybrid controller that consists of a hysteretic controller during transient and a PI controller during steady state. Each of these control structures is optimized based on the same multi-objective optimization routine and a defined cost function. After the optimal controller design for each control structure is identified, the optimized designs are compared to identify the advantages and disadvantages of each structure. Additionally, a high current prototype current source based on a multi-phase interleaved converter with 6 interleaved modules switching at 60kHz is used to verify the most promising control structures, the developed models, and the results presented in this paper. Among the different studied structures, the adaptive hybrid controller is shown to exhibit the best performance to step transients and the MPC shows great potential following arbitrary waveforms, but also striking shortcomings in the presence of measurement noise.

INDEX TERMS Current control, interleaved converter, optimal control, multi-objective optimization, high dynamic performance, high power DC-DC converters.

I. INTRODUCTION

High bandwidth and precise current sources with the ability to deliver step-like as well as arbitrary/controllable current waveforms are emerging nowadays, finding a broad spectrum of applications, such as power hardware-in-the-loop (P-HiL) simulations [1]–[3], driving accelerator magnets for medical and fusion energy applications [4]–[7] or testing equipment for HVDC grids [8], [9]. The specifications for these applications are ever increasing, as they often require a high current rating, with a high dynamic (i.e. low rise/settling time) combined with a low ripple, and a good reference tracking capability.

In order to fulfill these specifications, a combination of optimized hardware and control software design is necessary. The hardware optimization includes the development/selection of a proper topology and its parameters. The topology and the parameters are often chosen based on a specification-driven design space methodology, aiming to find a design space with solutions, which are theoretically able to meet the specifications [10], [11]. On the other hand, the control software requires the design of a controller that takes advantage of the chosen topology and ensures that the full potential of the system is met.

Fig. 1 shows the topology of the current source chosen in this study as a test-bench. Unlike two-stage inverters, which have also gained attention recently [12], [13], the chosen topology is a single-stage, 6-phase interleaved, two-level buck-type converter with split DC-link. The multi-phase structure of the source offers the flexibility to fit different applications and increases the current rating of the source, making it suitable for various high current applications in the kA range. Moreover, interleaving the module currents $i_{L,i}$ allows for an increased effective switching frequency and

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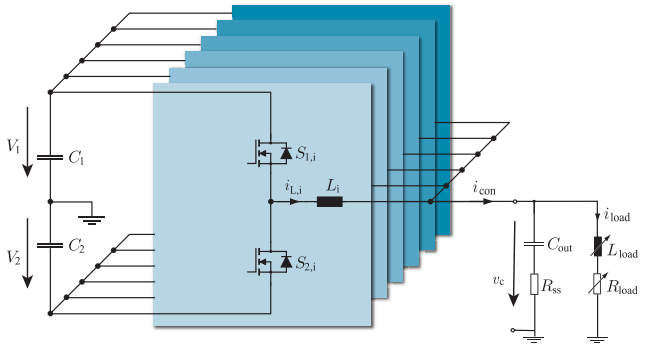

FIGURE 1. Schematic of the 6-phase interleaved current source converter.

TABLE 1. Parameters of the studied current source.

Quantity	Symbol	Value
Output current range	i_{con}	0..1500A
Output voltage range	v_c	0..550V
Upper DC-link capacitor voltage	V_1	750V
Lower DC-link capacitor voltage	V_2	50V
Module inductance	L_i	240μH
Output capacitance	C_{out}	3μF
Damping resistance	R_{ss}	5Ω
Module switching frequency	f_{sw}	60kHz

bandwidth, and significantly reduces the converter current ripple i_{con}. The main parameters of the source are listed in Table 1. It should be observed that the two-level buck-type topology might not be the most efficient topology for the whole output voltage range that needs to be served (measured efficiency surpasses 98% for v_c of 550V but is lower than 95% for v_c lower than 50V at nominal current). However, efficiency and power density are rather secondary goals for the aforementioned applications, where high dynamic performance, low ripple and high modularity are considered primary goals [9]. Note also that due to the high effective switching frequency and the ripple cancellation that is ensured by the interleaved operation, a rather low output capacitance is used. A damping resistance chosen to properly shape the natural response of the system's load current (which is not actively sensed/controlled) is also used in series to the output capacitance. A low effective output capacitance is essential to ensure that the load current features a high bandwidth. A detailed explanation about the choice of the topology, its parameters, and the output stage (i.e. C_{out}-R_{ss}) can be found in [9] and [14].

Regarding the control strategy, the most widely used current control approach for interleaved DC-DC converters are linear average-based current control methods (e.g. PI control) [15]. This method uses the average current of each phase in order to provide precise reference tracking while ensuring a constant switching frequency and an equal current sharing between the phases. Despite its benefits and its simplicity, the maximum achievable bandwidth of this concept is compromised by inevitable closed-loop delays (i.e. measurement, communication, and power stage delays). The concept was applied in multi-phase converters implemented as a conventional PI control in [16], as an LQR-based state feedback control (SFC) in [17] and as a H-infinity control in [18].

Another widespread control scheme that is often used for interleaved systems is the hysteretic controller [19], [20]. Due to its simple implementation, intuitive design, and near optimal large signal properties, it is particularly attractive for highly dynamic systems. However, in its conventional form, it suffers from i) switching frequency jittering, that results in imprecise interleaving and therefore increased ripple, ii) inaccurate reference tracking, and iii) imbalanced current sharing between the phases, in the presence of parameter mismatch [21], [22]. To overcome these issues, an adaptive hybrid control scheme for interleaved converters is presented in [23], making use of the hysteretic controller during fast transients, and smoothly transitions to a PI controller once the steady state is reached. Another hybrid controller using a PID controller in combination with a sliding mode scheme was presented in [24]. The presented control concept exhibited time-optimal response and good disturbance rejection capability. Although the concept is particularly interesting, its conceptual complexity due to its non-linear nature and high implementation cost makes it impractical, as highlighted in [25].

Furthermore, model predictive control structures (MPC) have gained popularity, driven by the increased computational power of modern micro-controllers and FPGAs. In MPC, an optimization problem is formulated and solved in each time step in order to achieve the control objectives without violating pre-defined constraints. Generally, a longer prediction horizon leads to improved performance and stability of the MPC [26] in DC-DC power electronic converters. Nevertheless, the growing need for higher switching frequencies imposes limitations on the maximum allowable computation time to solve the aforementioned optimization problem and practically results in a rather limited prediction horizon [27]. Specifically for current control of DC-DC converters, where the plant is a simple single-input single-output (SISO) system without cascaded loops and constraints for states, a long prediction horizon does not provide a significant benefit and therefore MPC schemes are an attractive solution to increase the system's performance.

All mentioned control structures are well suited for systems like the current source converter of Fig. 1. Identifying the best possible controller requires not only a structured optimization procedure, but also a systematic comparative evaluation of their performance, which is missing from the existing literature. Furthermore, the comparative evaluation that takes place in this work provides a structured comprehensive framework for control optimization routines based on performance evaluation indicators and highlights the possible control design trade-offs in a systematic way. It also allows to identify the maximum performance limitations of each control structure, in terms of their dynamic and steady state performance. Additionally, recent technological advancements have allowed fast computational and sampling

operations (e.g. high-end FPGAs, high sampling rate ADCs). These advancements enable the use of advanced control schemes coupled with high sampling frequencies and fast processing speeds, without increasing the cost to unacceptable levels. These advancements can potentially disrupt the optimization results and reshape the picture of what is achievable, highlighting again the need for a detailed comparative evaluation.

In the scope of this work, the performance of i) a conventional PI controller with an update rate equal to the switching period, ii) a PI controller with a fast execution rate, equal to the sampling frequency instead of the switching frequency iii) a LQR-based SFC, iv) a model predictive controller (MPC), and v) an adaptive hybrid controller, are systematically compared. For a fair comparison, first a general optimization routine, suitable for all the above schemes is developed and presented. The optimization routine identifies the optimum control parameters of any given control structure, based on pre-defined control performance evaluation indicators of the steady state as well as of the dynamic performance, and a well-defined cost function that encompasses the control objectives. Then, a comparison between the optimal control designs is performed and the advantages and disadvantages of each scheme are revealed. Finally, experimental results on a high-power prototype current source are carried out to verify the used models as well as the most important findings.

This paper is structured as follows: Section II presents an overview of the compared control concepts and the underlying models that are used in this study. Section III describes performance evaluation indicators for steady state and transient operation, and the optimization routine for the identification of the optimum control design point. Section IV provides the optimization results for the different control structures and discusses the common trade-offs between steady state and transient performance. Then, the different optimally designed control structures are compared. In section V, experimental results obtained with a full-scale prototype system are shown. The results verify the models that have been used throughout this study. Finally, section VI summarizes the main conclusions and contributions of this work.

II. MODELING AND CONTROL STRUCTURES

This section presents the investigated control structures, as well as the necessary models and analytical expressions that are used to describe/simulate their performance.

Initially, the power stage and the feedback loop are identical for all the discussed control structures and the main assumptions for the common elements of the control loop are listed below.

- The measured states of the system are the individual module currents $i_{\mathrm{L,i}}$, the output voltage v_{c}, and the input capacitor voltages V_1 and V_2. Since V_1 and V_2 are only slowly changing, their measurements are assumed to be ideal and possible delays are neglected.
- The power semiconductor stage (half-bridge) is assumed to be ideal with a turn-on delay that is equal to the interlocking time. For the considered setup a rather conservative interlocking time of 500ns is assumed. Since modern SiC devices are used in the prototype system, the rise/fall times are considered to be significantly lower than the interlocking time and therefore they are neglected. The on-state resistance of the switches is also neglected, as it does not influence the control performance and usually can be compensated. It should be noted that the power stage is modeled with the detailed switching model and not with a sub-cycle average model [28]. The power stage is represented in the following schematics with the blocks "Power stage delay" and "Switching stage" (e.g. in Fig. 2).
- The module currents $i_{\mathrm{L,i}}$ are measured with a DC-500kHz bandwidth current sensor. The output voltage v_{c} is measured with a compensated RC voltage divider, with a bandwidth of 500kHz. To filter the high frequency harmonics of the analog signal, an additional 4th order analog low pass filter is included, with a cut-off frequency of 400kHz in the design of both $i_{\mathrm{L,i}}$ and v_{c} measurement circuits. The analog signal delay of the filter can be expressed as:

$$G_{\mathrm{analog}}(s) = e^{-s \cdot T_{\mathrm{sense}}} \tag{1}$$

  The current and voltage sensors together with the analog filter are responsible for an analog signal delay T_{sense} of approximately 3μs, that is modeled in the following schematics by the block "Sensor delay" (e.g. in Fig. 2).
- The sampling frequency of $i_{\mathrm{L,i}}$ and v_{c} is considered to be 960kHz, which is 16 times faster than the switching frequency of each individual module. Oversampling allows the reduction of the digital delays of the measured states, and enables the use of a controller that can be executed faster than the switching frequency, as will be discussed later.

$$G_{\mathrm{digital}}(s) = e^{-s \cdot N \cdot T_{\mathrm{sample}}} \tag{2}$$

  In this study, a two sampling periods delay ($N = 2$) is assumed (i.e. one for the sampling of the ADC locally in the converter's module, and one for the serial communication of the measured value to the master controller). The digital delay of the system is modeled in the following schematics with the block "Sampling delay" (e.g. in Fig. 2).
- Due to oversampling, some of the sampling instances might coincide with switching actions resulting in noisy sampled values (a problem that is pronounced in high power interleaved converters). An intuitive and low delay method to filter out these values is to use a "median filter", that buffers k samples, sorts them, and picks their median value. The transfer function of this median filter can be expressed as in (3), where the symbol $\lfloor\rfloor$ is used for the floor function.

$$G_{\mathrm{median}}(s) = e^{-s \cdot \lfloor k/2 \rfloor \cdot T_{\mathrm{sample}}} \tag{3}$$

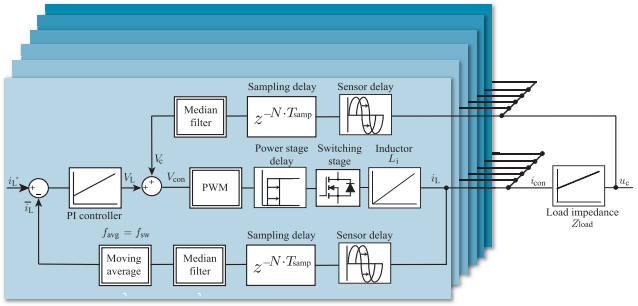

FIGURE 2. Schematic of the PI closed loop control structure for the six-phase interleaved converter system.

In this study, a median filter with $k = 3$ is used both in the current as well as in the voltage measurement of the studied system and results in a digital delay of one sampling interval.

- In order to reduce the static error and to minimize the influence of the ripple, a "moving average filter" with an average frequency equal to the ripple frequency of the measured state, is often used in converter systems. The transfer function of the moving average filter is given in (4), where m is the number of samples of the moving window.

$$G_{\text{avg}}(s) = \frac{1}{m} \cdot \frac{1 - e^{-s \cdot m \cdot T_{\text{sample}}}}{1 - e^{-s \cdot T_{\text{sample}}}} \tag{4}$$

In this study, a moving average window with $m = 16$ is applied on the current measurements of the control loop.

- A conventional saw-tooth shaped PWM modulator is assumed with a finite resolution that is defined by the switching frequency and the maximum clock frequency of the controller (i.e. 100MHz for this work). The transfer function of the PWM module can be modeled as a Zero-Order-Hold (ZOH) block with a sampling frequency equal to the update speed of the controller (T_{exc}), or equivalently the update rate of the duty ratio that acts as a reference signal for the modulator. It should be observed that having an update rate higher than the sampling frequency is of no benefit. The transfer function of the PWM model is given in (5).

$$G_{\text{PWM}}(s) = \frac{1 - e^{-s \cdot T_{\text{exc}}}}{s} \tag{5}$$

In the following, the investigated control structures and their detail feedback loops are presented and shortly discussed.

A. PI CONTROLLER WITH A SINGLE UPDATE PER SWITCHING PERIOD

Due to its robustness, intuitive design, and wide application in industrial systems, the PI control structure with a single update per switching period acts as the benchmark for this study. For interleaved converters, each phase can control its current individually and the sawtooth-shaped carriers used for the generation of the PWM can be phase-shifted to obtain an interleaved total converter current i_{con}. For optimum interleaving, a phase-shifting controller can be added and various methods that account for imbalances between the phases can be used [16], [29], [30]. The phase-shifting controller is not further discussed, as it is irrelevant for the present study. It should be noted that an external control loop for the total converter current can also be included but a preliminary study quickly showed that it offers no benefit to the performance of the overall system. The feedback control structure including the control delays and the converter plant is shown in Fig. 2.

In its conventional implementation, the controller of each phase is updating its output (duty ratio) once per switching period. The duty ratio is updated at the start of a new switching period and as a result phase 1 updates its duty ratio at times [0, T_{sw}, $2T_{\text{sw}}$,..], phase 2 at times [$\frac{1}{6}T_{\text{sw}}$, $\frac{7}{6}T_{\text{sw}}$, $\frac{13}{6}T_{\text{sw}}$,..], and so on. This strategy guarantees a constant switching frequency, but also results in a relatively high delay as can be deduced from (5). For the studied system with a 60kHz switching frequency per module, the delay of the PWM module based on (5) is $T_{\text{exc}} = 16.67\mu$s. For this control structure, the aim of the optimization procedure (Section III) is to identify the optimum gains K_{p} and K_{i}.

B. PI CONTROLLER WITH A FAST UPDATE RATE

In contrast to the conventional PI control implementation, in this variation the control output is updated multiple times per switching period. A common variance of this control structure is the PI controller that updates its reference duty ratio twice per switching period [31]. In this study, however, the control output is updated at every sampling period (i.e. 16 times per switching period), aiming to maximize the control performance and harness the fast switching capabilities of the latest generation of SiC devices that are used in the prototype system. The control structure is identical to the one shown in Fig. 2. For the studied system the only modeling difference is that the PWM module is modeled with $T_{\text{exc}} = 1.04\mu$s in (5).

While the conventional implementation results in a constant switching frequency, updating the duty ratio multiple times may result in a higher switching frequency, especially during transients. Consequently, a switching frequency limiter is implemented to limit the generated switching losses. This clearly increases the control complexity compared to the conventional scheme. Another downside of this scheme is that it usually requires a high-end control hardware with the capability to perform fast operations and a power stage that consists of fast switching semiconductors. As in the previous case, the aim of the optimization procedure for this control structure (Section III) is to identify the optimum gains K_{p} and K_{i}.

C. LQR-BASED STATE FEEDBACK CONTROLLER

In general, state space design allows the control designer to have a better overview of the system and implement an

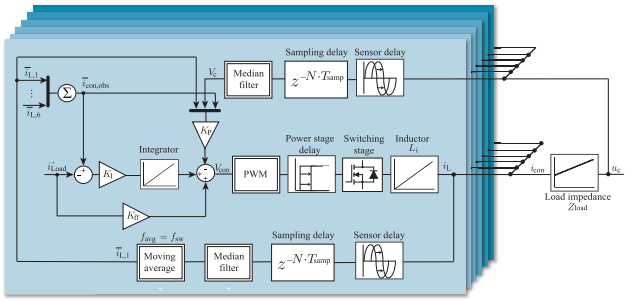

FIGURE 3. Schematic of the implemented SFC with a simple observer, for the six-phase interleaved converter system.

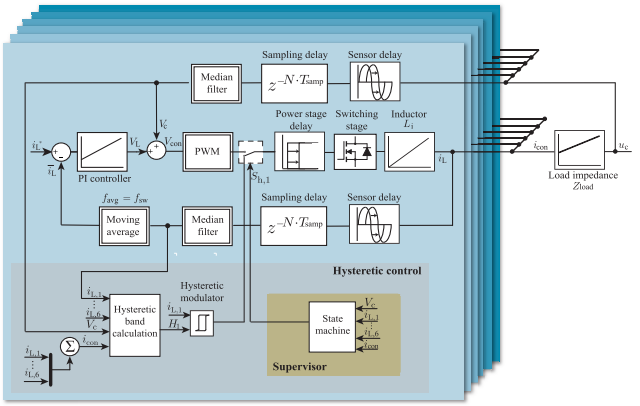

FIGURE 4. Schematic of the hybrid controller designed specifically for the six-phase interleaved converter system [23].

optimized control law, achieved by pole placement or by LQR-tuning solving an optimization problem [32], [33]. Observer-based SFC has been shown enable an increased bandwidth compared to conventional PI controllers, as delay information can partly be accounted for during the observer design [34]. The formulation of the state feedback control problem and the calculation of the relevant matrices and reference signals are explained in [35].

The control structure used in this study is shown in Fig. 3. First, it should be highlighted, that the load current of the investigated current source converter is not directly measured. Due to its high nominal amplitude (more than 1kA) and its high bandwidth, an expensive sensor would be required [36]. Therefore, the total converter current $i_{\mathrm{con,obs}}$ is calculated by adding the available module currents $i_{\mathrm{L,i}}$ and the load current i_{Load} is assumed to be approximately equal to i_{con}, which is guaranteed by the design of the output filter in systems acting as current sources [14]. Furthermore, an observer based on the state space representation of the system (e.g. Leunberger observer) could be used for the reconstruction of i_{Load}, accounting for the output stage parameters as well as the feedback loop delays. This approach is not applied in this study, in order to provide a fair comparison with the previously described controllers in terms of complexity. Furthermore, reducing the complexity of the controller allows using a faster execution rate, which increases the system transient performance as shown in section IV. Additionally, an integral action is included for the i_{Load}, as shown in Fig. 3.

In order to calculate the gains K_{P} and K_{I}, the unconstrained LQR optimization problem is formulated [37] for the state space system, augmented with the integrator. The Q and R matrices are given in (6)-(7). Q is a 9×9 matrix and R is a 6×6. For the currents $i_{\mathrm{L,i}}$, the same weights w_{i} are used.

$$Q = \mathrm{diag}[w_{\mathrm{i}}, .., w_{\mathrm{i}}, w_{\mathrm{v}}, w_{\mathrm{icon}}, w_{\mathrm{int}}] \tag{6}$$

$$R = w_{\mathrm{R}} \cdot I_6 \tag{7}$$

In this control structure, the aim of the optimization procedure (Section III) is to identify the optimum weights w_{i}, w_{v}, w_{icon}, w_{int} and w_{R}, that in turn result in the optimum gain matrices K_{P} and K_{I}.

D. ADAPTIVE HYBRID CONTROLLER FOR INTERLEAVED CONVERTERS

In [23], an adaptive hybrid current controller that consists of a hysteretic controller and a PI controller is specifically designed for interleaved converter systems, like the one of Fig. 1, in order to exploit their full dynamic potential, when step transients occur.

The schematic of the controller is shown in Fig. 4. The PI controller is used during steady state and during non-step transients due to its simplicity, constant switching frequency and good reference tracking capability. When a step transient is required, the supervisor shown in Fig. 4 switches the control mode to the hysteretic mode, which is significantly faster and inherently stable for every operating point. Details regarding the band calculation and the algorithm of the state machine of the supervisor as well as the transition techniques from one mode to the other to minimize the disturbance can be found in [23].

To evaluate the performance of the adaptive hybrid controller in this study, its algorithm is simulated. It should be noted that the band calculation block and the hysteretic modulator (Fig. 4) do not result in additional loop delays. For better performance the analog signal delay of the current measurement needs to be compensated or equivalently the hysteretic band needs to be adapted. In this case, the optimization procedure of Section III simply optimizes the PI controller as described in Section II-A.

E. MODEL PREDICTIVE CONTROLLER

Model predictive controllers (MPC) determine the next control action by solving an optimization problem at every time step. Depending on the type of the optimization problem, MPC methods are mainly classified for power electronic systems, into two different types, i.e. the finite control MPC (FCS-MPC) and the continuous control set MPC (CCS-MPC) [38], [39]. The FCS-MPC takes into account the switching behavior of the converter and formulates an integer optimization problem for deciding the switch signals directly.

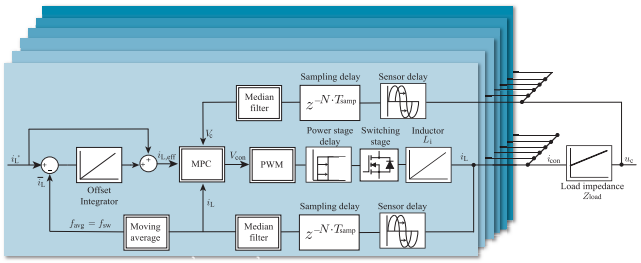

FIGURE 5. Schematic of the MPC closed loop control structure for the six-phase interleaved converter system.

On the other hand, the CCS-MPC typically solves a convex optimization problem to compute a continuous control signal and generates switching signals of power semiconductors with a modulator. In this paper, a CCS-MPC is formulated and compared such that a fair comparison with the other control schemes can be made. Note that the use of CCS-MPC ensures a constant switching frequency and allows straightforward current sharing between interleaved phases.

The schematic of the controller is shown in Fig. 5. Each phase computes its optimal averaged input voltage (i.e. duty ratio) at every switching period ($1/f_{\mathrm{sw}}$) and triangular carriers are used for the generation of the PWM. Note that the PWM carriers are phase-shifted and so are the MPC computation instances, just like in the case of the PI with a single update rate.

The plant model for each phase corresponds to the differential equation (8), where R_{p} represents the sum of the parasitic resistances of the semiconductor devices and the phase inductor, and V_{con} is the averaged input voltage over one switching interval.

$$\frac{\mathrm{d}i_{\mathrm{L}}}{\mathrm{d}t} = -\frac{R_{\mathrm{p}}}{L} \cdot i_{\mathrm{L}} + \frac{1}{L} \cdot (V_{\mathrm{con}} - V_{\mathrm{c}}) \tag{8}$$

The next state of the current can be discretized as given in (9), where a, b, and f are coefficients that can be determined based on (8), assuming that V_c is constant during switch periods.

$$i_{\mathrm{L}}[k+1] = a \cdot i_{\mathrm{L}}[k] + b \cdot V_{\mathrm{con}}[k] + f \cdot V_c[k] \tag{9}$$

The optimization problem can then be formulated in a linear MPC format, aiming to find the future control input that minimizes the difference between the predicted current state and the current reference.

$$\min_{\mathbf{U}[k]} \sum_{l=1}^{N} \left\| i_{\mathrm{L}}[k+l] - i^*_{\mathrm{L}}[k+l] \right\|^2_{\mathbf{Q}} \tag{10a}$$

$$s.t. \; -V_2[k] \leq V_{\mathrm{con}}[k+l] \leq V_1[k] \tag{10b}$$

In the equations above, $\mathbf{U}[k] = [V_{\mathrm{con}}[k], \cdots, V_{\mathrm{con}}[k+N-1]]^{\mathrm{T}}$ is the future control input, N is the prediction horizon, $\mathbf{Q} \geq 0$ is a weighting matrix and $\|\mathbf{z}\|^2_{\mathbf{Q}}$ denotes a 2-norm with the weighting matrix. V_1 and V_2 are the voltage levels of the split DC-link, shown in Fig. 1. As long prediction horizons do not provide much benefit for current control of SISO systems, $N = 2$ is chosen in this work.

The prediction model is represented in a linear system and only polytopic constraints are applied on control inputs. As a consequence the resulting optimization problem is a quadratic programming (QP) problem and an explicit MPC method as proposed in [40] based on multi-parametric quadratic programming (mp-QP) is utilized in this work. Explicit MPC handles an optimization process offline and enables implementation at very fast sampling rates [41]. With the optimization parameters $\theta = [i_{\mathrm{L}}, V_{\mathrm{c}}, i^*_{\mathrm{L}}, V_1, V_2]^{\mathrm{T}} \in \mathbb{R}^5$ for the given problem, the parametric solution to (10) is computed with the Multi-Parametric Toolbox [42] comprising a piecewise-affine function defined over 14 polytopic regions.

Additionally, an offset integrator is used in the MPC structure to account for inevitable model mismatches [43]. The integrator is enabled only when the average module current $i_{\mathrm{L,avg}}$ reaches approximately its steady state value (within a 5% tolerance band).

$$i^*_{L,\mathrm{eff}} = i^*_L + \sum K_i \cdot T_{\mathrm{sw}} \cdot (i^*_L - i_{L,\mathrm{avg}}) \tag{11}$$

In order to avoid excessive overshoot during transients, a simple prediction of the future current state based on a first order delay model of the current measurement is used in this work.

III. CONTROLLER OPTIMIZATION

In this section each of the presented controllers is optimized in a systematic way based on the performance evaluation indicators defined in Section III-A. Based on these indicators the ideal system performance is defined and the physical limits of the system are explained in Section III-B. Finally in Section III-C, the optimization procedure (common for all controllers) that is followed for the different control structures is shown and the choice of the cost function that needs to be minimized is discussed.

A. PERFORMANCE EVALUATION INDICATORS

To evaluate the performance of the controller, the following indicators are defined (see Fig. 6).

- Overshoot constraint: The peak of the converter current $i_{\mathrm{con,max}}$ should be lower than a pre-defined percentage Q of the commanded reference I^*_{con}. This acts as a constraint in the optimization procedure and the solutions that do not fulfill this requirement are discarded.

$$Q = \frac{I^*_{\mathrm{con}} - i_{\mathrm{con,max}}}{I^*_{\mathrm{con}}} \tag{12}$$

- Switching frequency constraint: When the sampling frequency is higher than the switching frequency and the update rate of the duty ratio is also higher than the switching frequency, the converter modules might switch with a frequency higher than the nominal. In order to protect the switches from overheating and limit the switching losses, a maximum average switching frequency $\bar{f}^{\mathrm{max}}_{\mathrm{window}}$ within a defined time window

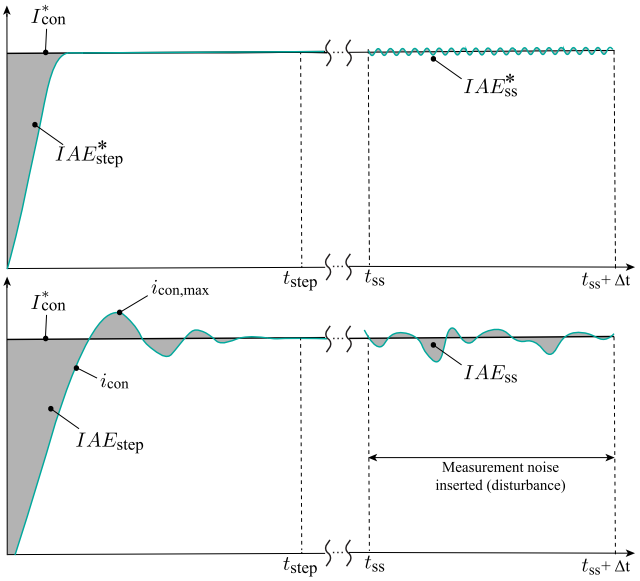

FIGURE 6. Graphical representation of the performance evaluation indicators. Upper graph: Ideal. Lower graph: Non-ideal.

needs to be set. The average switching frequency $\bar{f}_{\text{window}}$ is then calculated as given in (13), where N is defined in (14), and $p[k]$ is 1, if a rising edge is detected for switch $S_{1,\text{i}}$ (Fig. 1) and 0 otherwise.

$$\bar{f}_{\text{window}} = \left(\frac{1}{N} \cdot \sum_{k=1}^{N} p[k]\right) \cdot \frac{1}{T_{\text{sample}}} \tag{13}$$

$$N = \frac{t_{\text{window}}}{T_{\text{sample}}} \tag{14}$$

In (14), t_{window} is the time window within which the average switching frequency $\bar{f}^{\text{max}}_{\text{window}}$ is evaluated and it is the hardware designer's choice, that depends on the thermal limits of the semiconductor devices. In this study t_{window} of 0.5ms is used and the maximum average switching frequency is 10% higher than the nominal switching frequency (66kHz).

- Transient Performance: The transient performance is evaluated based on the integral absolute error (IAE) of the total converter current i_{con}. For consistency reasons, IAE_{step} is always evaluated with the same simulation model, during the optimization procedure, until a defined time t_{step} assuming that the converter current has settled by then. The IAE_{step} is defined then as in (15).

$$IAE_{\text{step}} = \int_0^{t_{\text{step}}} \left|I^*_{\text{con}} - i_{\text{con}}(t)\right| \, dt \text{ [As]} \tag{15}$$

- Steady State Performance: The steady state performance and the disturbance rejection of the controller is evaluated based on the integral absolute error (IAE) of the total converter current i_{con}. The evaluation takes place for a specified duration Δt_{ss}, after the steady state is achieved (t_{ss}), under the presence of measurement noise, as defined in (16).

$$IAE_{\text{ss}} = \int_{t_{\text{ss}}}^{t_{\text{ss}}+\Delta t_{\text{ss}}} \left|I^*_{\text{con}} - i_{\text{con}}(t)\right| \, dt \text{ [As]} \tag{16}$$

The time duration Δt_{ss} is chosen appropriately in order to study the impact of low frequency harmonics that are induced in the controlled currents due to actions of the closed loop control system. Clearly, the choice of Δt_{ss} depends on the studied system and the control requirements. For the studied system, a $\Delta t_{\text{ss}} = 1\text{ms}$ is chosen, in order to study the effect of sub-hamornic content down to 1kHz.

In high power electronic systems, measurement noise arises due to a variety of reasons (e.g. switching actions of the power stage, ripple of the reference voltage of the analog measurement circuitry etc). For this study, a realistic noise model is used based on measurements performed on the prototype system. The noise model for the current measurements $i_{\text{L,i}}$ is assumed to follow a Gaussian distribution with a mean value of 0A and a variance of 1A, as noted in (17). Similarly, the voltage measurement v_{c} is assumed to follow a Gaussian distribution with a mean value of 0V and a variance of 1V given in (18).

$$i_{\text{noise}} \sim \mathcal{N}(0,\ 1) \tag{17}$$

$$v_{\text{noise}} \sim \mathcal{N}(0,\ 1) \tag{18}$$

It is worth mentioning, that the noise model is a random variable and in order to compare the results of different simulations, the same seed is used in the random number generator, which produces the random noise, and therefore the same random numbers are generated in every simulation. Furthermore, the same seed is used for the random noise of all the i_{L} measurements as a worst case scenario.

B. IDEAL SYSTEM PERFORMANCE

Based on the described performance evaluation indicators, the ideal control performance can be derived. In this study, the ideal controller is defined as the controller that has its performance limited only by the physical constraints of the converter system. In the case of step transients, the ideal controller has a zero overshoot ($Q = 0$) and the minimum IAE_{step} is limited only by the control loop's plant (i.e. switching stage and module inductor L_{i}). The exemplary IAE^*_{step} is graphically depicted in Fig. 6.

Similarly, the minimum IAE_{ss} is only limited by the ripple of the total converter current i_{con} in the considered operation point. In other words, the ideal controller is able to reject the disturbances introduced by the noise sources of the measurements and achieve a flattop accuracy that is only limited by the unavoidable switching ripple. The exemplary IAE^*_{ss} is graphically depicted in Fig. 6. Based on these considerations the reference transient evaluation indicator IAE^*_{step} as well as the steady state one IAE^*_{ss} can then be calculated.

These serve as normalization factors in the optimization procedure described in Section III-C.

C. OPTIMIZATION PROCEDURE

Fig. 7 shows the optimization procedure for identifying the optimal gains of the control structures. The procedure is the same for every control structure and the only differences are the gains that need to be identified. For the PI controllers the aim is to extract the K_p and K_i parameters, while for the SFC the weight inputs to the LQR method w_i, w_v, w_{load}, w_{int} and w_R need to be identified.

- At step 1, a discrete search grid for the gains is defined along with the overshoot constraint Q_{max}, which is usually given by the specifications of the system. The maximum average switching frequency constraint $\bar{f}^{max}_{window}$, which is given by the hardware design limitations of the system, is also defined. Furthermore, the performance of an ideal controller can be calculated based on the physical limitations of the studied system and the ideal performance evaluation indicators IAE^*_{step} and IAE^*_{ss} can be calculated.
  Then the cost function that needs to be minimized is defined. The considered cost function is:

$$f(IAE_{step}, IAE_{ss}) = w_{step} \cdot \frac{IAE_{step}}{IAE^*_{step}} + w_{ss} \cdot \frac{IAE_{ss}}{IAE^*_{ss}} \quad (19)$$

  In (19), IAE^*_{step} and IAE^*_{ss} are used as normalization factors and the design weights w_{step} and w_{ss} can be chosen according to the controller design goals of the application. For the present study equal weight factors ($w_{step} = w_{ss} = 0.5$) are chosen for the transient and the steady state performance.
- At step 2, after choosing the gains, the step transient simulation is executed and the resulting overshoot is checked against the maximum overshoot requirement. The overshoot requirement acts as a design constraint. If the overshoot is higher than the maximum allowed one, new gains are chosen and a new simulation is executed. If the overshoot is within the limits, the algorithm continues to step 3.
- At step 3, the algorithm executes the steady state simulation, where the noise models for the current and voltage measurements are inserted, as previously described. The average switching frequency $\bar{f}_{window}$ is calculated based on (13) and the algorithm checks if the $\bar{f}^{max}_{window}$ constraint is violated. If it is violated, a new controller design is chosen and the algorithm returns to step 2.
- At step 4, the performance indicator factors IAE_{step} and IAE_{ss} as well as the respective cost function can be calculated based on (15), (16) and (19). The solution is then stored and the algorithm chooses new gains and returns to step 2.
- At step 5, after all described steps have been executed for all the gain combinations, the algorithm chooses the optimum point which corresponds to the controller design that results in the minimum value for the cost function $f(IAE_{step}, IAE_{ss})$.

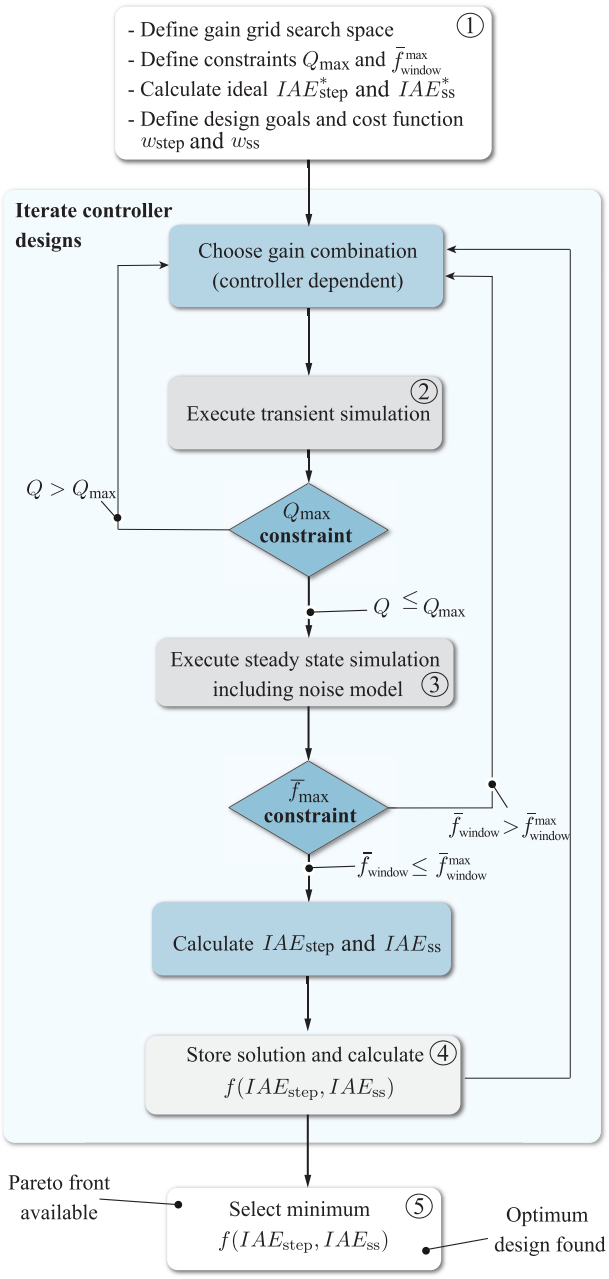

FIGURE 7. Flowchart of the optimization procedure for every controller structure.

IV. OPTIMIZATION RESULTS AND COMPARATIVE EVALUATION

The exemplary system in Fig. 1 is used as a test-bench to assess the performance of the five control schemes. In Fig. 8, the investigated controller designs are plotted for each control structure. The performance ratio pairs IAE^*_{step}/IAE_{step} and IAE^*_{ss}/IAE_{ss} for each controller design are depicted. An ideal controller would be the one which achieves a performance

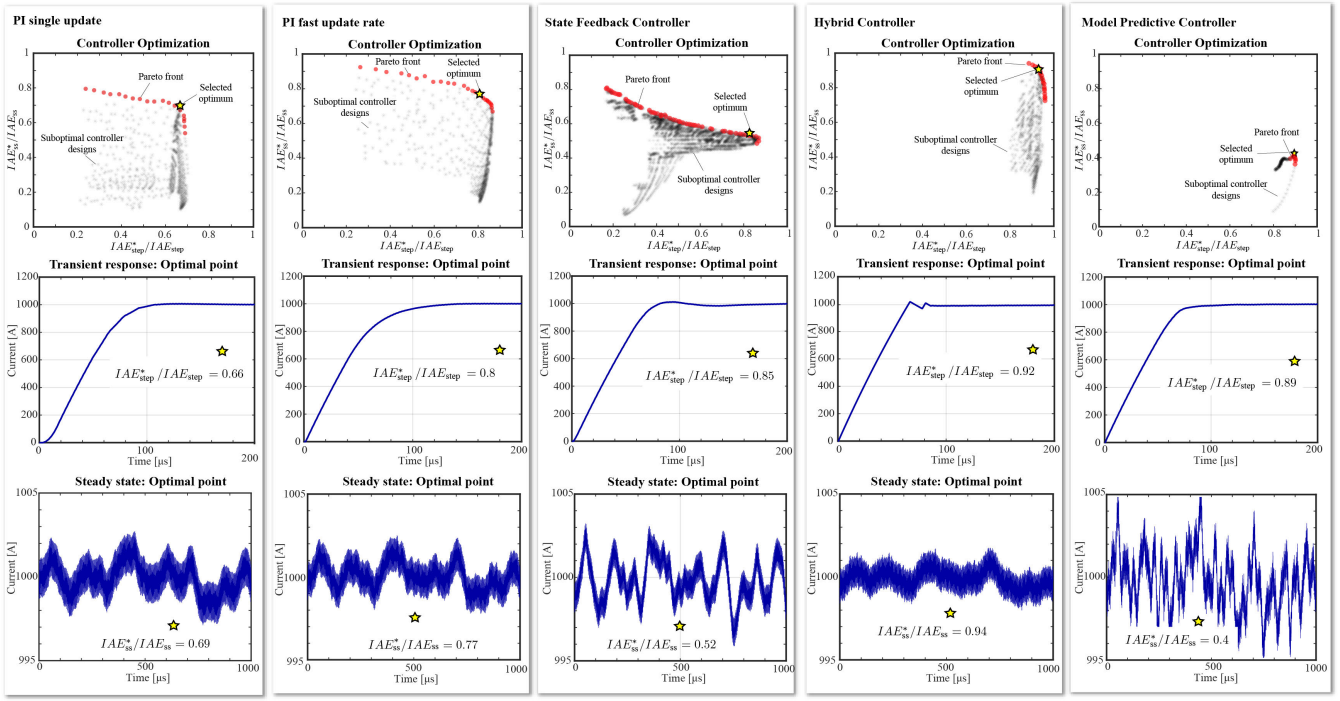

FIGURE 8. Results of the optimization procedure for all the control structures. For each control structure all the investigated controller designs are plotted based on their performance pairs (IAE^*_{step}/IAE_{step}, IAE^*_{ss}/IAE_{ss}). The closer the pair is to the ideal pair (1,1), the better the performance of the controller. The Pareto-front for each of the investigated structures is also plotted and the optimum point is highlighted. The transient and the steady state performance of each optimum point is also shown.

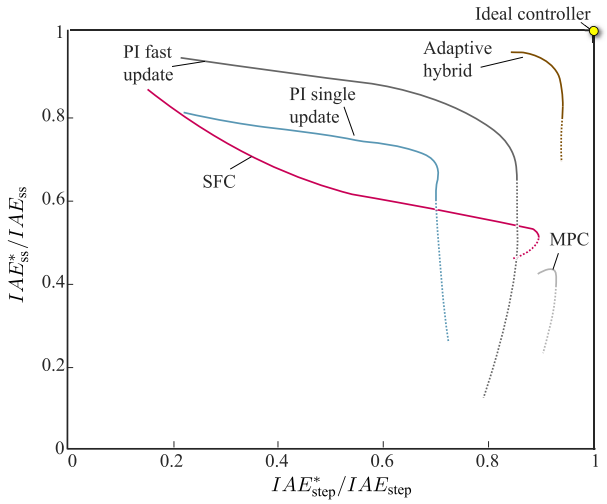

FIGURE 9. Comparison of the pareto fronts of the investigated controllers for step transients followed by a flattop.

ratio pair of (1,1). The resulting Pareto-front is highlighted in red for each controller structure and the chosen optimum design point is noted in the figure. The transient response as well as the steady state response with the inserted noise for the chosen optimum design are also shown in Fig. 8.

Initially, the PI controller with a single update per period is compared to the PI with fast update rate. Based on the extracted Pareto fronts it can be seen that the PI with fast update results in both a faster transient response (i.e. higher IAE^*_{step}/IAE_{step}) as well as a slightly better steady state performance (i.e. higher IAE^*_{ss}/IAE_{ss}). This is an immediate result of the fact that with a faster update rate a more aggressive implementation of the controller is possible (i.e. higher control gains) without violating the overshoot constraint. Furthermore, the power switching stage is allowed to switch multiple times per switching period resulting in a lower delay of the modulator and a faster response, which is especially beneficial for large signal transients.

Based on the results, one of the major findings is that a high sampling frequency combined with a faster execution rate can lead to a PI control implementation with a significantly better performance. In this study, the optimum chosen point for an update rate that is 16 times faster than the switching frequency results in an 18% increase of the transient performance, and an 11% increase of the steady state performance compared to the benchmark implementation for step reference currents. As already mentioned one downside of the faster update rate is the need to allow a possible temporary increase of the switching frequency (explained in Section III-C), as well as the need for a high performing control platform. Nevertheless, the SFC and the hybrid controller are studied only for the case of fast update rates in the upcoming results, due to this finding.

Regarding the SFC, it can be observed that the selected optimum point has a higher transient performance than the PI structure, and in general the maximum transient performance

that can be achieved is higher, as design points with a transient performance ratio of up to 0.9 can be achieved. However, the steady state performance of the controller is significantly worse. This can be attributed to the feedback of the total converter current $i_{\text{con, obs}}$, which in this case contains the added noise of all the individual current measurements $i_{\text{L,i}}$. Less aggressive designs (with a lower w_{icon}) can achieve a more satisfactory steady state performance ratio (up to approximately 0.8 in Fig. 8), but the transient response is then compromised. All in all, it can be concluded that with measurement noise the trade-off between steady state and transient performance achievable with the SFC is inferior to the trade-off achievable with a PI structure, as long as the implementation of the SFC does not include a compensation/model of the relevant time delays, or additional conditioning of the measured values.

The hybrid controller offers, as expected, the best transient performance, which is also near the optimal for step current references. In fact, the increased ripple and overshoot due to the hysteretic modulation strategy and the need to return to interleaving is the reason that the response is not time optimal (transient ratio $IAE^*_{\text{step}}/IAE_{\text{step}}$ is below 1). The use of the hysteretic controller during step transients, allows for a less aggressive controller design for steady state, leading to a high performance at flattop, too. As shown later, this less aggressive control design has a detrimental effect on the control performance, when the reference current is not a step, and the PI mode (with low gains) of the hybrid controller is used throughout the transient [23].

The transient performance of the MPC is almost as good as the achieved performance of the hybrid controller. As expected, the gain of the offset integrator does not play a significant role in the ratio $IAE^*_{\text{step}}/IAE_{\text{step}}$, as it is not enabled until the converter current is close to the reference (within 5% explained in Section IIE). Interestingly, the MPC implementation suffers from a pronounced ripple at flattop in the presence of noise, exhibiting by far the worst performance among the investigated schemes. The result suggests that the presence of noise in the measurements has a particularly detrimental effect on the reference tracking performance of the MPC.

Fig. 10 shows the transient performance of the optimized controllers in a single comparative graph, and Table 2 summarizes the performance evaluation indicators of the investigated controllers, operating under the conditions used during the optimization.

Table 3 gives a more complete overview of the comparative performance of the simulated controllers for different operating scenarios. In Table 3 the *IAE* performance indicator of the benchmark case (i.e. the PI with single update) is divided by the *IAE* performance of the respective controller. As a result a ratio higher than one corresponds to a higher performance compared to the benchmark case. Since the PI with single update is the benchmark, all case-scenarios exhibit a performance ratio of 1. Five different case-scenarios are simulated, based on additional current waveforms that need to be generated when the current source operates as a P-HiL test bench:

- **Case 1:** 1kA amplitude sine wave reference with 100Hz frequency.
- **Case 2:** 1kA amplitude sine wave reference with 400Hz frequency.
- **Case 3:** 1kA amplitude step response with a resistive load of 0.3Ω.
- **Case 4:** 1kA amplitude step response with a resistive load of 0.4Ω.
- **Case 5:** 1kA triangular waveform with 800Hz frequency.

In all simulations the noise models described in (17)-(18) are included. In the case of scenarios 1 and 2, the adaptive hybrid controller uses its average control mode (PI with fast update), since the hysteretic controller is not enabled for non-step transients. The performance difference compared to the PI with fast update arises from the different optimized gains. The less aggressive gains used for the hybrid controller to achieve a good steady state performance, have a detrimental effect on its performance following sinusoidal references. It can be also seen that the adaptive hybrid provides again the best performance in the scenarios following a step reference current.

Furthermore, the PI with a fast update rate is consistently significantly better than the benchmark case by more than 10%, and is not significantly influenced by the change of operating conditions. On the other hand, the SFC shows a superior performance compared to the benchmark in following sinusoidal waveforms, but its performance for changing operating conditions in step references is severely affected. In case 4 in particular where the resistive load is doubled compared to the optimized case, the SFC shows 38% lower performance rating compared to the benchmark controller, indicating that new gains have to be found and the controller needs to be re-tuned.

More importantly, the MPC shows its performance benefits when following sinusoidal references, where it is by far the best choice. Moreover, its performance in step transients does not seem to be affected by load changes. Overall the analysis indicates that the MPC is the better choice for following arbitrary references with different loads, among the different investigated schemes. However, its poor performance during flattop make it a rather sub-optimal choice for step transients, where high flattop accuracy is required.

TABLE 2. Performance summary of optimized control structures, for the operating conditions used during the optimization procedure.

Controller	$\frac{IAE^*_{\text{step}}}{IAE_{\text{step}}}$	$\frac{IAE^*_{\text{ss}}}{IAE_{\text{ss}}}$	$Q_{\max}$
PI single update	0.66	0.69	0.7%
PI fast update	0.8	0.77	0.15%
State feedback	0.85	0.52	1.25%
Adaptive hybrid	0.92	0.94	2%
Model Predictive	0.89	0.41	0.36%

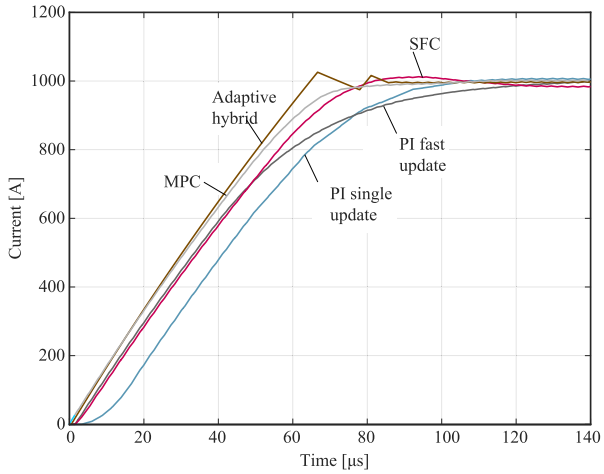

FIGURE 10. Comparative simulations depicting the transient response of the chosen optimal designs for each control structure following a step reference current.

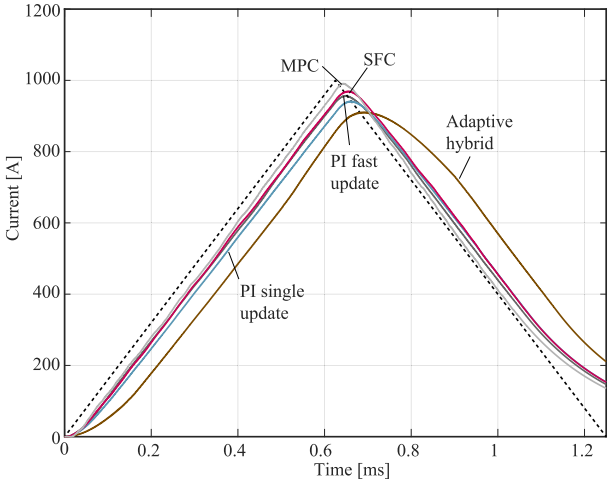

FIGURE 11. Comparative simulations depicting the transient response of the chosen optimal designs for each control structure following triangular reference current (case scenario 5).

TABLE 3. Evaluation of performance of the optimized controllers for different operating case-scenarios.

Controller	Case 1	Case 2	Case 3	Case 4	Case 5
PI single update	1	1	1	1	1
PI fast update	1.19	1.28	1.16	1.1	1.3
State feedback	1.16	1.16	0.89	0.62	1.41
Adaptive hybrid	0.49	0.45	1.29	1.28	0.49
Model Predictive	2.19	2.20	1.19	1.15	1.9

Case scenario 5 includes a triangular reference current with a frequency of 800Hz and an amplitude of 1kA. This corresponds to a current gradient of approximately 1.6A/μs, which is challenging for the converter during step-down due to the low control margin when the voltage is close to 0V, as can be seen in Fig. 11. It can be noted that the controllers demonstrate a big difference in their performance compared to the benchmark case demonstrating in practice their bandwidth. Once again the best performer is the MPC followed by

TABLE 4. Parameters of the experimental measurements.

Quantity	Symbol	Value
Upper DC-link capacitor voltage	V_1	600V
Lower DC-link capacitor voltage	V_2	50V
Module inductance	L_{i}	240μH
Output capacitance	C_{out}	3μF
Damping resistance	R_{ss}	5Ω
Module switching frequency	f_{sw}	60.096kHz
Current/Voltage sampling frequency	f_{sample}	960kHz
FPGA main clock frequency	f_{FPGA}	100MHz
Interlocking time	t_{dead}	500ns
Analog signal delay	T_{sense}	3μs
Load resistance	R_{load}	0.2Ω
Load inductance	L_{load}	5μH

the SFC and the PI controller with the fast update rate. It is observed that simply executing the PI controller faster results in a 30% reduction of the error compared to the benchmark case. Furthermore, the conservatively tuned PI controller of the adaptive hybrid scheme, which is the reason for its high flattop stability performance in step references, shows again a poor performance following transients. The performance of the investigated controllers to case scenario 5 is also shown for completeness in Fig. 11.

V. EXPERIMENTAL RESULTS

In order to validate the findings, the most promising controllers have been implemented and tested on a prototype high power 6-phase interleaved DC-DC converter. The multi-phase prototype converter is shown in Fig. 12 and a single buck module is shown in Fig. 13.

The multi-phase prototype system can deliver a peak current of up to 1.5kA for a duration of at least 10ms and 1kA of continuous current. Each buck module is water-cooled, with potted inductor cores for thermal management reasons, and features the latest generation of SiC-module devices. The prototype system fulfills the specifications of a variety of applications, that require the generation of arbitrary current waveforms, including a test-bench for Power Hardware-in-the-Loop simulations [9].

Each buck module is equipped with a separate current measurement board that features also an on-board CPLD to communicate with the local ADC. The current sensor IC is based on the anisotropic magneto-resistive effect and has a wide bandwidth (DC-500kHz), followed by an analog stage for reducing the switching noise and conditioning the signal to an appropriate range, so that it can be converted with high resolution by the ADC (approx. 100mA per LSB, full measurement range $\pm$300A) [44]. The current/voltage measurements of all the modules are sampled and collected locally on the CPLD, and then they are communicated serially through the USB-C type connections shown in Fig. 12 to the master controller. The communication link is operated at 60MHz and results in a total sampling frequency of 0.96MSps, which corresponds to approximately 16 samples per switching period. This allows the implementation of controllers with a faster execution rate, as previously described. The master controller

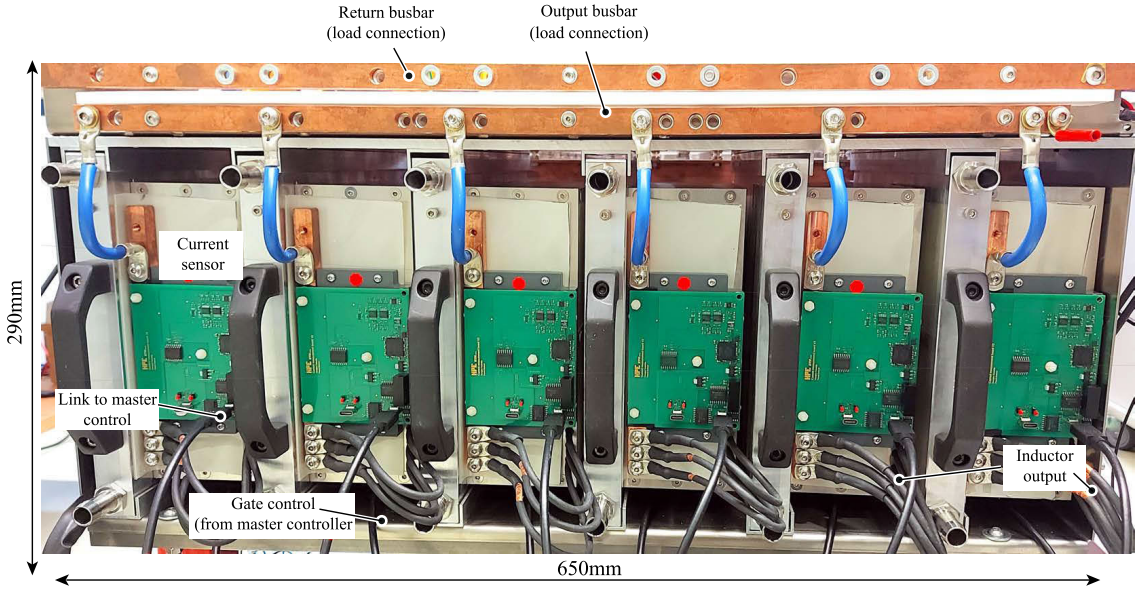

FIGURE 12. Picture of the prototype high power 6-phase interleaved buck-type converter with a peak current capability of 1.5kA and a nominal current of 1kA.

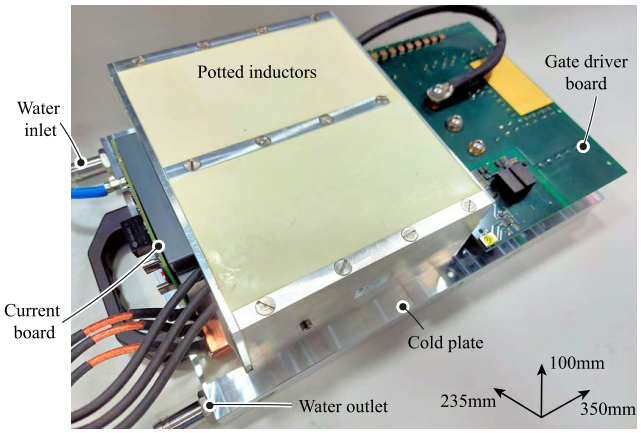

FIGURE 13. Picture of the full SiC-based buck module of the interleaved DC-DC converter with potted inductor core.

comprises a powerful Altera Cyclone IV FPGA (115k logic element units), in order to provide a design flexibility and the ability to fit high performing controller designs. The controller samples all the measurements with the same clock, synchronizes them, and controls the modules by providing the gate signals through the appropriate interfaces (also shown in Fig. 12).

Similarly to the current measurement, the voltage measurements are also stored locally on a CPLD and are communicated serially to the master controller, where they are conditioned and synchronized. The output voltage measurement comprises a compensated RC voltage divider and an active filter stage with a 400kHz bandwidth, and runs with a 0.96MSps sampling frequency. The input voltage levels V_1 and V_2 are sampled with a 0.1MSPs frequency as their dynamics are relatively slow, due to the big size of the input capacitor bank used in the prototype system (not shown in the pictures). The following measurements use the parameters and measurement probes listed in Table 4. The total input DC link voltage is set to 650V and the maximum output current used is 400A.

Fig. 14 shows the performance of the investigated and implemented control structures with a step response of 400A, followed by a flattop. The module currents as well as the total current can be seen during the transient response, and the figure depicts as well a closer look into the flattop performance. All in all, the controllers behave as expected. The PI with a fast update rate shows a faster response time compared to the benchmark PI implementation as is also pronounced in Fig. 15, where the transient responses of the different controllers are plotted in a single graph. The adaptive hybrid controller shows the best transient performance and manages to return to steady state smoothly, demonstrating a small ripple due to the loss of interleaving in the first cycles after the transient. Optimal interleaving is achieved one switching cycle later than in the simulated case shown in Fig 8. The MPC shows also excellent transient performance, which is near time-optimal too, but results in an increased ripple around the reference point, caused by the noise of the current measurements.

At this point it should be mentioned, that the step response of Fig. 15 cannot be directly compared to the one shown in Fig. 10 due to the difference in the reference current. The different reference current is the reason for the slower response of the two PI control schemes (compared to the response achieved in Fig. 10), as their duty ratio at the beginning of the transient is significantly lower than 1. This results in a much slower response compared to the adaptive hybrid and the MPC schemes, where a near optimal response

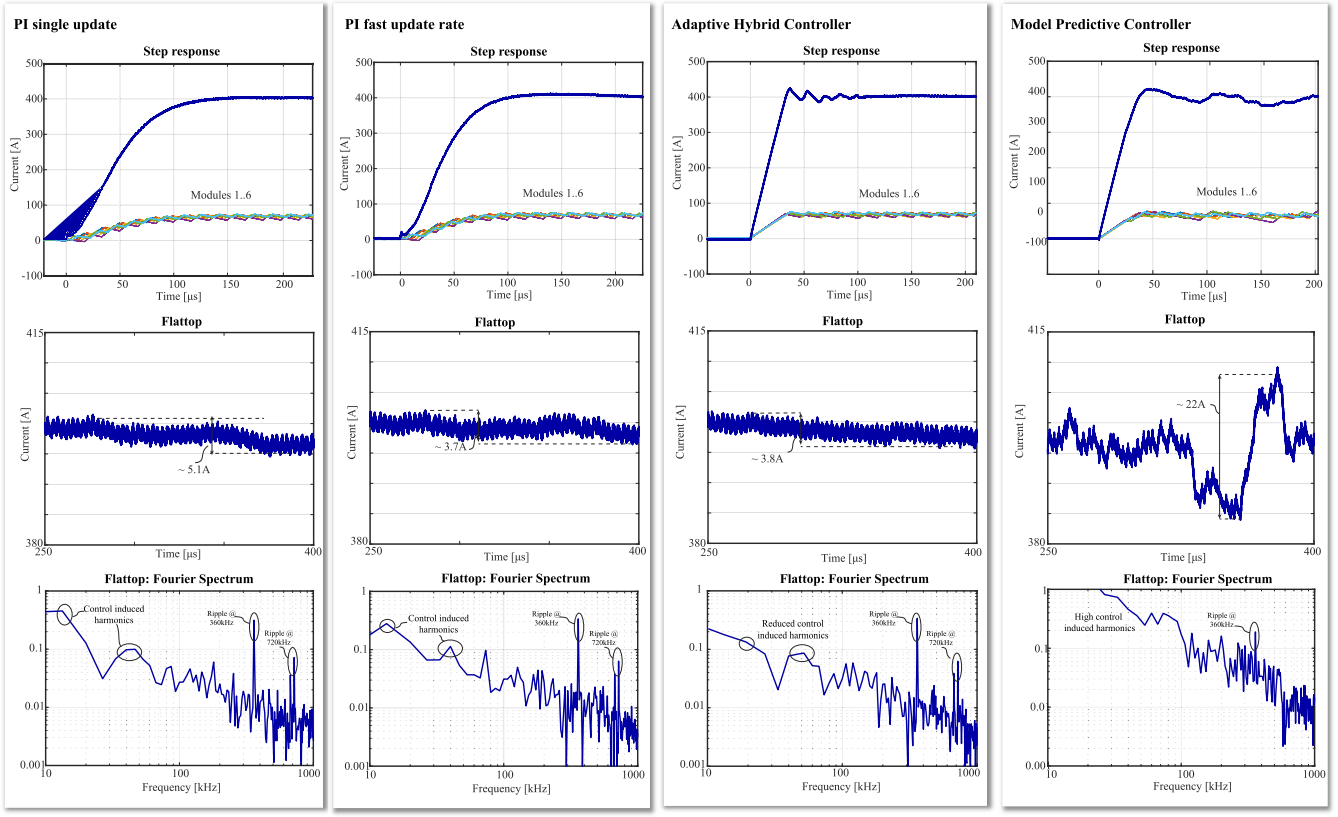

FIGURE 14. Experimental results of 400A step response transient obtained with the presented hardware prototype system and the different investigated control structures.

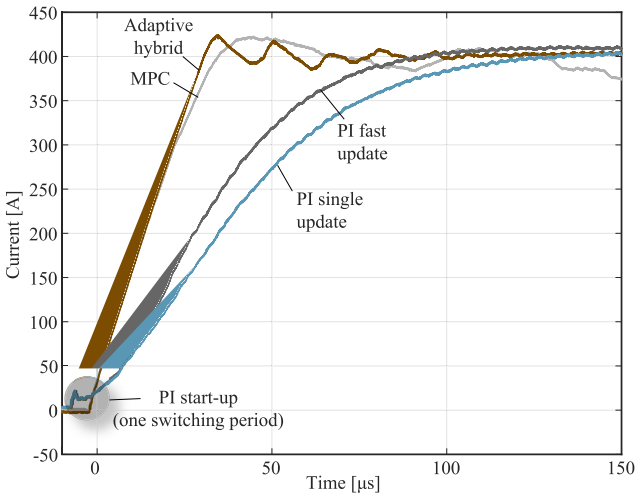

FIGURE 15. Comparative experimental results depicting the 400A step response of the chosen optimal designs for each control structure.

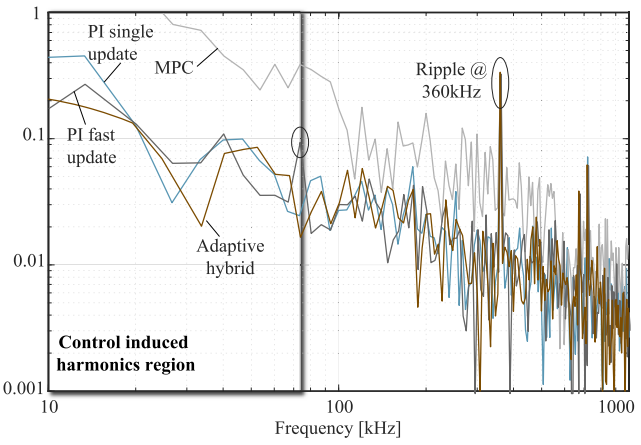

FIGURE 16. Comparative experimental results depicting the resulting Fourier spectrum of the flattop for each control structure.

is achieved regardless of the reference current. The PI controllers have a start-up phase at the beginning of the transient, that lasts for one switching period.

In Figure 15 it can also be seen, that the adaptive hybrid controller reaches the reference only slightly faster than the MPC since both appear to be near time-optimal. Due to the sub-optimal interleaving when operating in the hysteretic mode and the non-ideal measurements, the increased current ripple persists for two additional switching periods, while the adaptations during the hysteretic mode reduce but do not eliminate the current ripple. This causes extra disturbances that are not visible in the simulations. Nevertheless, once the hysteretic mode is disabled the controller returns to PI mode, the phase-shifting controller ensures optimal interleaving.

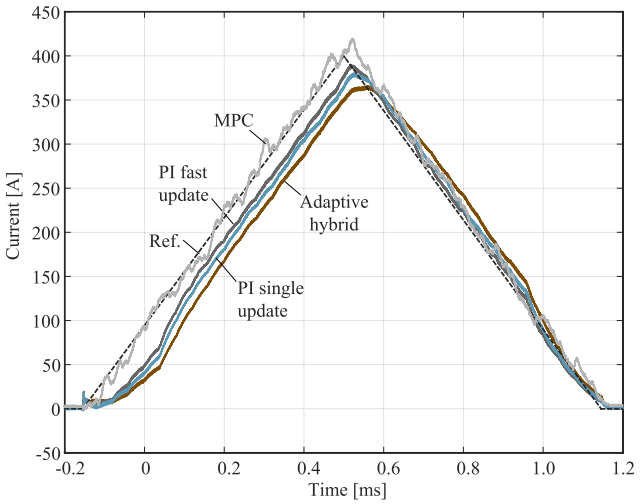

FIGURE 17. Comparative experimental results of the chosen optimal designs following a 400A triangular reference current.

Regarding steady state performance, the experimental results show similar tendencies compared to the outcomes of the simulation analysis. Notably, the MPC suffers from high disturbances that are caused by the noisy current measurements and result in an increased current ripple around the reference point. This behavior is mainly attributed to the fact that the MPC mainly acts on the instantaneous current and not on the result of a moving average filter like the rest of the controllers during steady state. The rest of the controllers show a good performance during flattop, that could be improved if the noise of the measurements is reduced. During the compared 150μs flattop, the PI with the fast update rate and the adaptive hybrid controller show in total approximately 3.7A current ripple around the reference point, which is mainly attributed to the offset correction. In fact, the adaptive hybrid controller shows reduced low frequency harmonics during the demonstrated operating time interval as can be deduced based on its Fourier spectrum at harmonic frequencies below 60kHz. The converter does not generate sub-harmonics in this region, and therefore the additional current frequencies arise due to the actions of the controller.

Fig. 16 shows the resulting Fourier spectrum of the flattop for the different control structures. It is verified that the MPC results in the highest amplitude for low frequency harmonics and that the adaptive hybrid results in the lowest amplitude for most of the frequencies lower than 60kHz. The 60kHz range is taken as a reference, since harmonics above this frequency could be generated naturally also due to sub-optimal interleaving or inductance mismatches between the phases.

Finally, Fig. 17 shows experimental results with the optimized control schemes following a triangular reference with an amplitude of 400A. The result highlights the superior performance of the MPC in following arbitrary references, as it results in an excellent tracking performance. However, it results again in the highest ripple, due to the presence of noise in the current measurement and its more aggressive nature. At this point it should be clarified that the impact of noise is pronounced in the experiments compared to the simulations, as it is not the same for the different phases and occurs at different time instances (mainly induced because of the switching actions which are interleaved). This results in disturbances in the individual duty ratios which causes the converter system to lose interleaving and result in an increased ripple (ripple currents are added instead of cancelled out). Furthermore, Fig. 17 highlights once again the advantage of the PI with the fast update rate over the benchmark implementation and shows that the non-aggressive tuning of the adaptive hybrid controller, which resulted in the best steady state performance during a step transient, is insufficient if high tracking accuracy is required.

VI. CONCLUSION

Overall, the main conclusions of the study are summarized hereby:

- Pareto-front optimizations of the different schemes showed that the adaptive hybrid controller has the ability to perform close to the ideal controller when following step transients.
- The PI controller with a fast update rate results in an increased performance of at least 10% compared to the conventional PI controller implementation with a single update rate. This performance increase comes at the expense of higher computational power and increased complexity.
- The SFC and MPC schemes can be tuned to achieve a higher dynamic potential compared to the PI controller. However, they both exhibit a worse steady state performance, which hinders their applicability in systems requiring high flattop accuracy.
- The adaptive hybrid controller achieves the best performance in step transients, since the hysteretic controller ensures a near optimal transient response, and the PI controller can be tuned to minimize the disturbances introduced by noise during flattop.
- The MPC scheme is the only one that manages to match the dynamic performance of the adaptive hybrid controller in step transients, but its flattop performance is severely affected by noise in the feedback loop.
- Overall the MPC shows consistently the best transient response when following arbitrary (non-step) reference currents. Its aggressive nature however hinders its ability to handle measurement noise and severely impacts its performance. As a result further signal conditioning (e.g. Kalman filter, digital filters) might further increase its performance.
- Experimental measurements have verified the results of the analysis and subsequently the modelling.

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