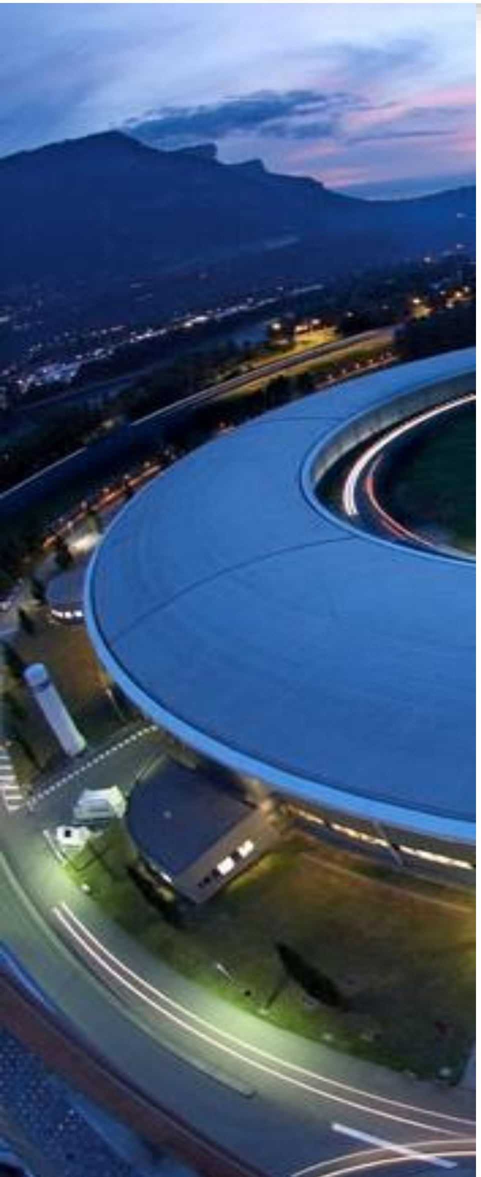


Characterization results of the first small pixel high rate (SPHIRD) photon counting hybrid pixel detector prototypes

D. Magalhães, P. Fajardo, P. Gryboś, R. Kleczek, P. Kmon, P. Otfinowski and M. Ruat

24th iWoRiD - 2023

The SPHIRD Project

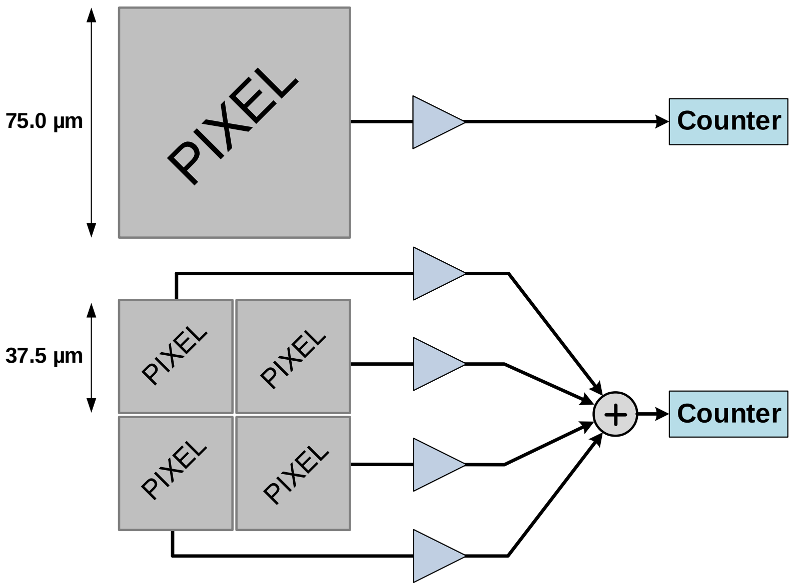
Small Pixel, High Rate Detector

SPHIRD: A photon counting hybrid pixel detector with

- **High flux** capabilities (very high **count-rate)**

> ×30 the state-of-the-art

- ✓ Fast front-end analog electronics (×2-3)
- ✓ Pile-up compensation methods (×3-5)
- ✓ 2×2 pixel binning (×4)



- Small pixels for optimum use of **intense coherent beams**

- Designed to operate with **high-Z compound semiconductors**
  - ➢ to increase radiation hardness
  - ➢ to reach high energies: optimised in the 15 - 30 keV range, usable in a wider range
  - ➢ to minimize parallax effects (important with small pixels)

More about the context tomorrow @ 16:20 (Talk by P. Fajardo)

The SPHIRD Project

Target Goals and Strategies

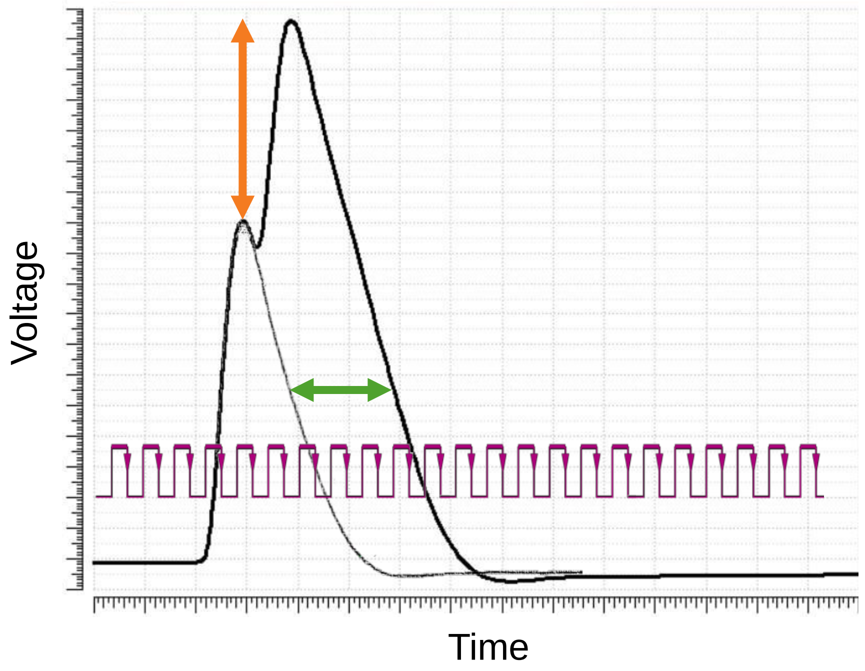
Count-rate @ 10% pile-up	>15 Mcps; >60 Mcps after binning
Pixel pitch	< 50 µm
Energy Range	10 – 35 keV
Frame rate	> 10 kHz

Main technical choices:

- Readout electronics designed for electron collection, Si and high-Z sensors
- TSMC 40 nm CMOS technology
- Fast Charge Sensitive Amplifier design with short output pulses
- Explore **pile-up compensation** and **sub-pixel relocation** schemes in the pixel logic

Pulse processing techniques
Pile-up Compensation

- **STDC**: **ST**andar**D** **C**ounting mode, with faster CSA and readout chain
- **VDIS**: **V**oltage **DIS**crimination mode, use of extra discriminators to detect pile-up in the pulse amplitude
- **TDIS**: **T**ime **DIS**crimination mode, use of extra discriminators to detect pile-up in the pulse width
- **FPHC**: **F**ractional **PH**oton **C**ounting mode, use of an asynchronous clock to measure the duration of the hits (based on ToT techniques)

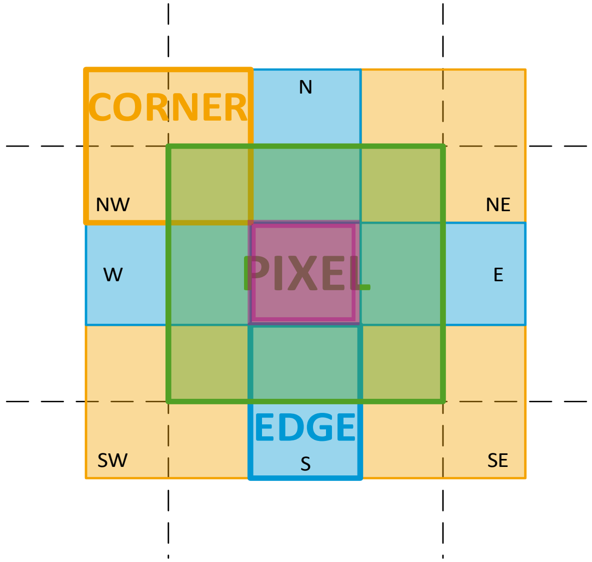


The techniques are based on similar strategies adopted in the community
(P. Grybos *et al*, 10.1109/TNS.2007.914018; M. Andrä *et al*, 10.1016/j.nima.2018.11.026; T. Loeliger *et al*, 10.1109/NSSMIC.2012.6551180)

Pulse processing techniques

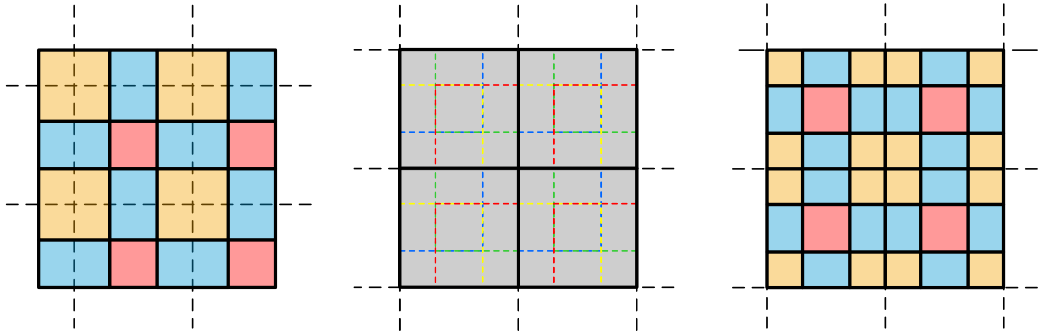
Subpixel relocation

- Analyze coincidence pulses (charge sharing events) between neighbor pixels to decide on:
  - **PIXEL** allocation (**arbitration algorithm**)
  - Relocation of the X-ray hit within boundary regions:
    - **CORNER** regions (NW, NE, SE, SW)
    - **EDGE** regions (N, S, E, W)
    - **CENTER** region



- Combine the pixel and region location information to register the hit into a matrix of 2×2 or 3×3 subpixels

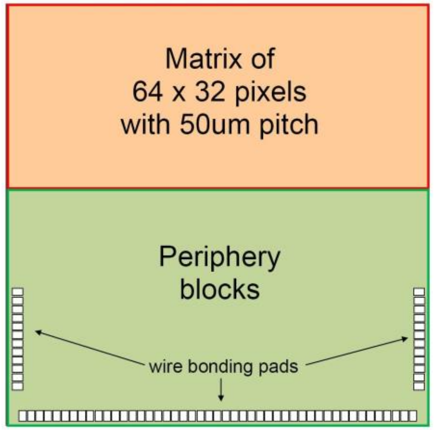
- Requirements:
  - Large number of **counters** in the pixel
  - Uniformization of the effective subpixel areas



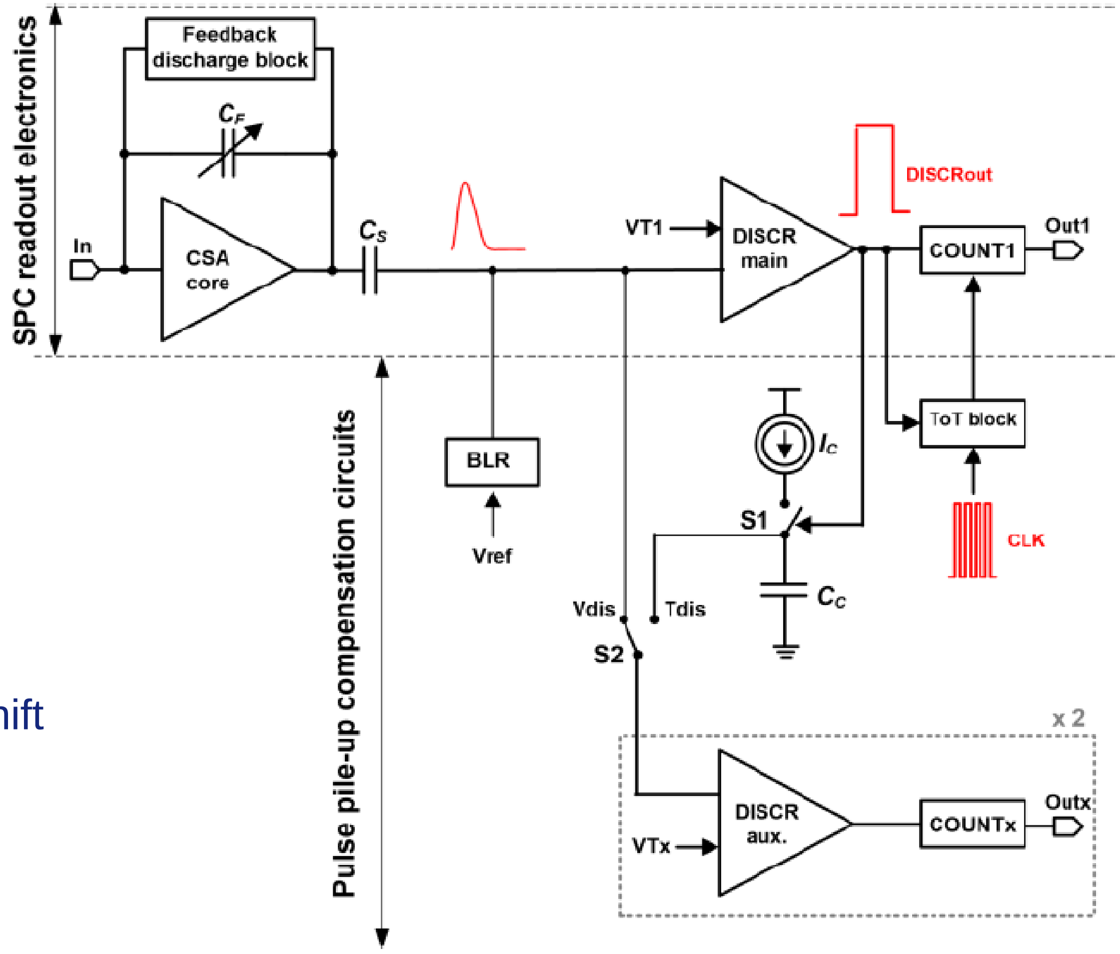
2×2 relocation (asymmetric) | 2×2 relocation (overlapping) | 3×3 relocation

First ASIC Fabrication Run

Test ASIC Design v1.0



- 32 x 64 pixels of 50 µm pitch = 1.6 x 3.2 mm
- CSA based on the Krummenacher structure
- Baseline Restorer circuit to mitigate the DC baseline shift
- 3 discriminators (2 operating in voltage or time mode)
- 32 bits counter, can be split in up to 3 shorter counters



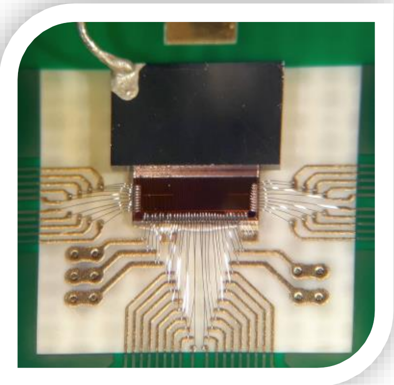
P. Grybos *et al*, 10.1109/TCSII.2023.3267859

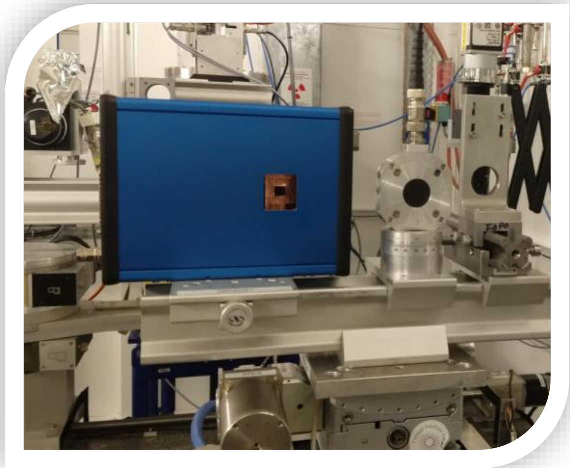
First ASIC Fabrication Run

Sphird Test Prototypes

First assemblies arrived in May 2022

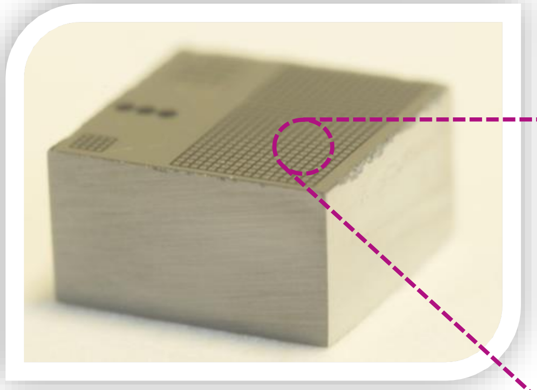
- NI RT FlexRIO readout
- 200 MHz clock

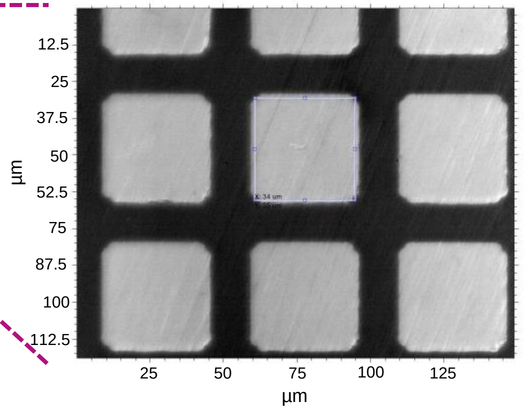




- Foreseen sensors (electron collection):
  - Silicon : 400 µm thick , 50 µm pitch
    - ➢ 12 assemblies successfully bonded
  - CdTe : 1 mm thick, 50 and 100 µm pitch
  - *High-flux* CZT : 2 mm thick, 50 and 100 µm pitch

in bonding process





Courtesy of DUE2LAB

Characterization Results

- CSA Performance
- Count Rate Capabilities
- Pixel Relocation Schemes

All experiments were performed at beamline BM05 @ ESRF.

Many thanks to Phillip Cook and all the BM05 staff for their support

Characterization Results

Performance of the CSA, pencil beam and full field beam

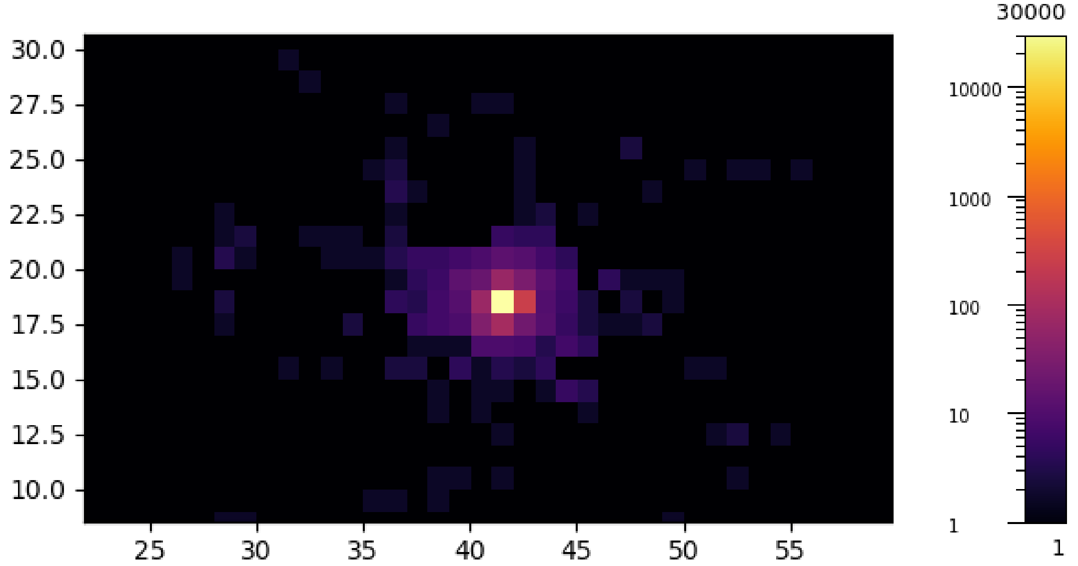
Experimental conditions:

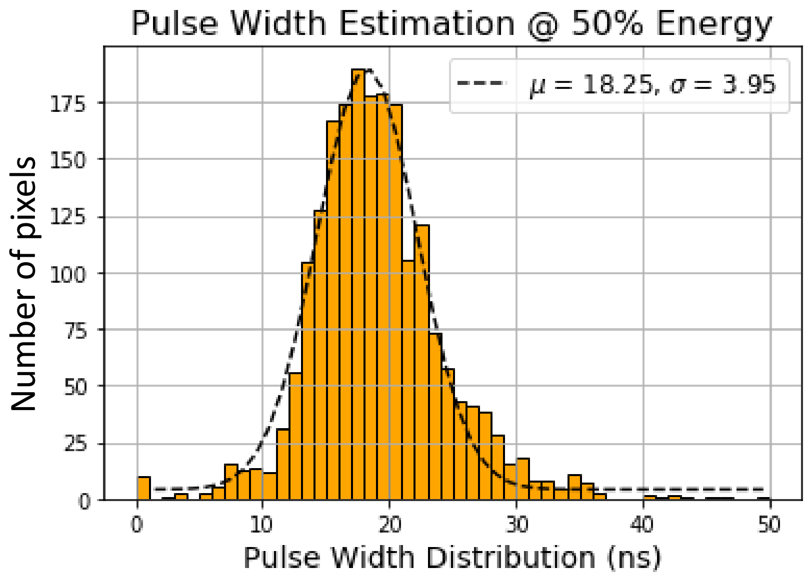
- 16 keV monochromatic beam, 16-bunch mode
- -200V sensor Bias Voltage, Si sensor

Estimations of the CSA response in nominal conditions

- Gain and noise: pencil beam (≈7x5µm) at the center of the pixel
- Pulse width: FPHC mode, fullfield irradiation of the whole matrix

Gain	0.026 ± 0.001 LSB/e^-
Noise @ 16 keV	179±15 e^-
Avg. pulse width @ 50%E	18±4 ns



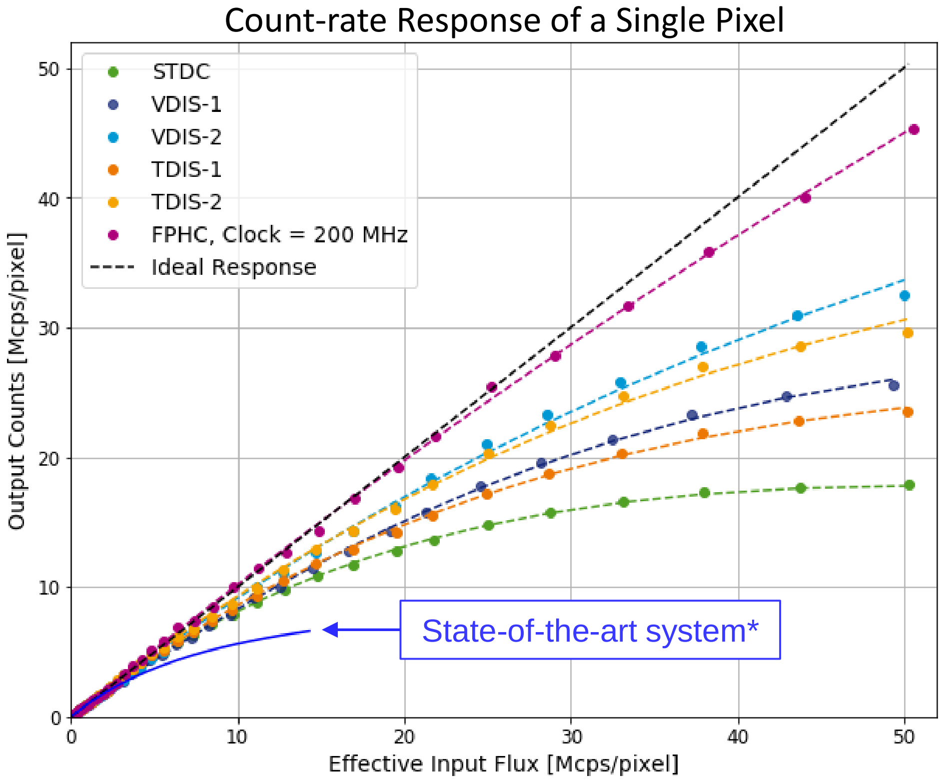


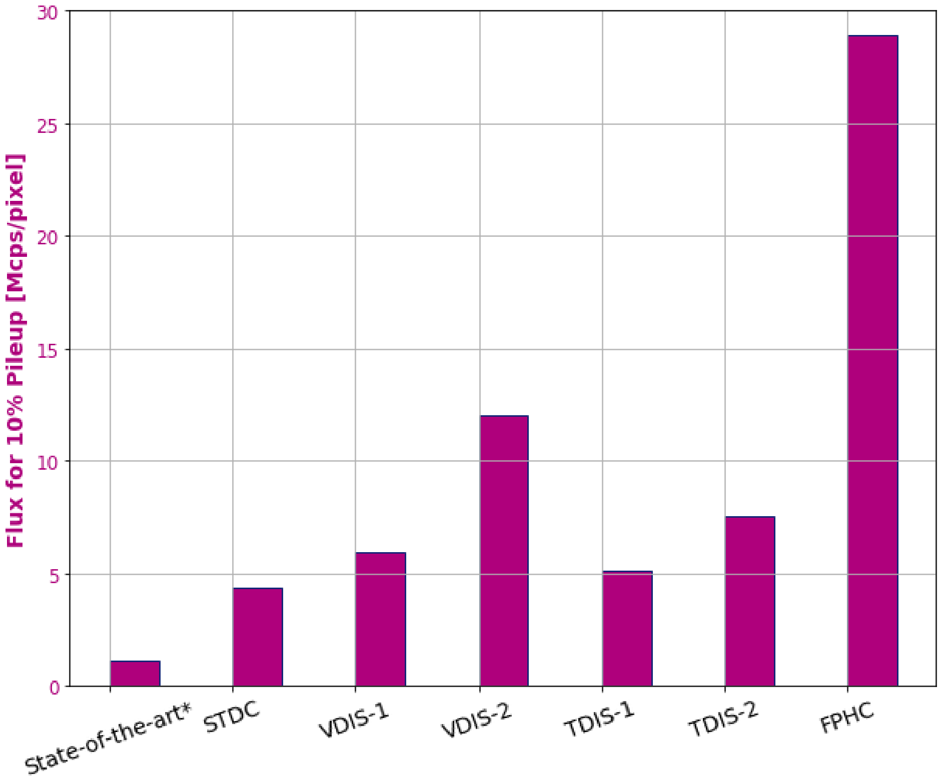
Characterization Results
Count-rate Capabilities, direct beam

Experimental conditions:

- 15 keV monochromatic beam, multi-bunch mode, scan of the flux with Al filters
- Direct beam defined with slits, 1.0x0.5 mm (20x10 pixels)

Impact on the SNR² also investigated
→ Check poster P1.25 (D. Magalhães)





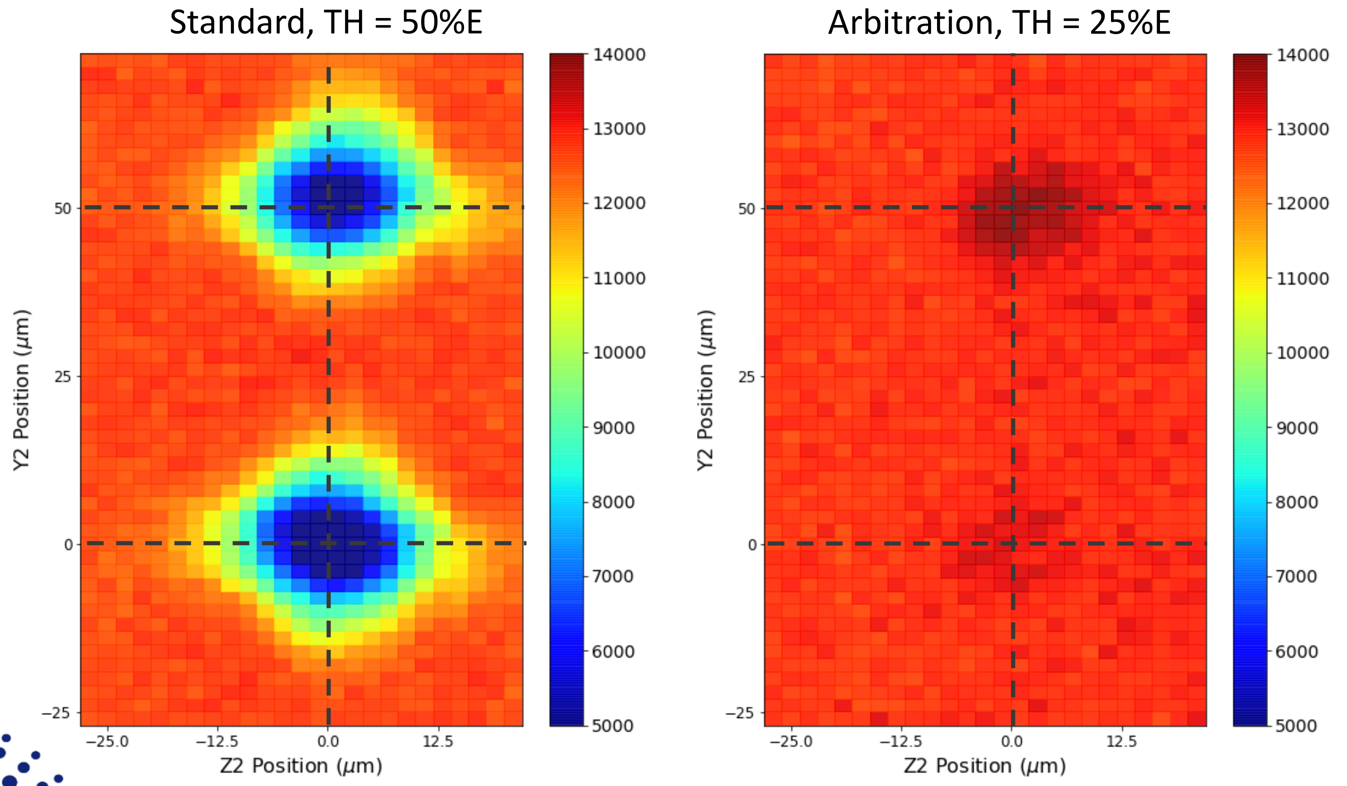
* T. Donath *et al*, 10.1107/S160057752300454X

Characterization Results

Arbitration Algorithm functionality, pencil beam scans

Experimental conditions:

- 16 keV monochromatic beam, 16-bunch mode
- Data from pencil beam scans of the corners, beam ≈ 7x5 µm:



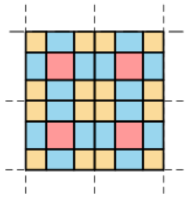
- Behavior at the corners measured for 50µm pitch:
  - Count losses in Standard mode: **7.79%**
  - Arbitration overcounting: **0.13%**

➢ Estimated behavior for 37.5µm pitch:
  - Count losses in Standard mode: **13.85%**

➢ These results and simulations will be used to decide on the pixel pitch for the final system

Characterization Results

Sub-pixel Relocation – 3x3 subpixels, pencil beam scans



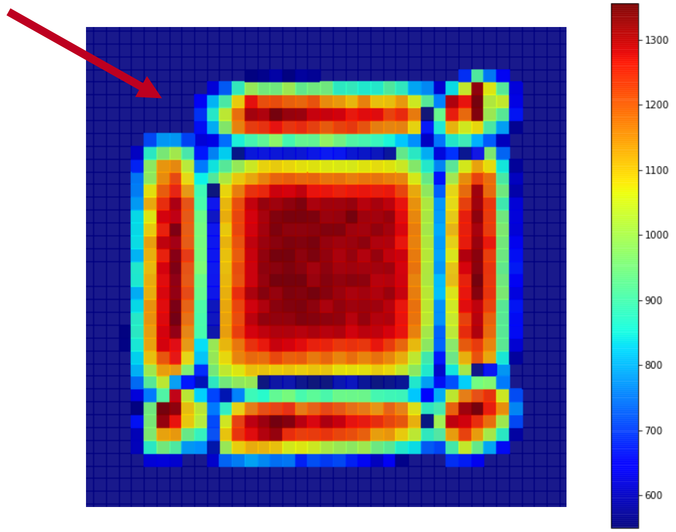
Experimental conditions:

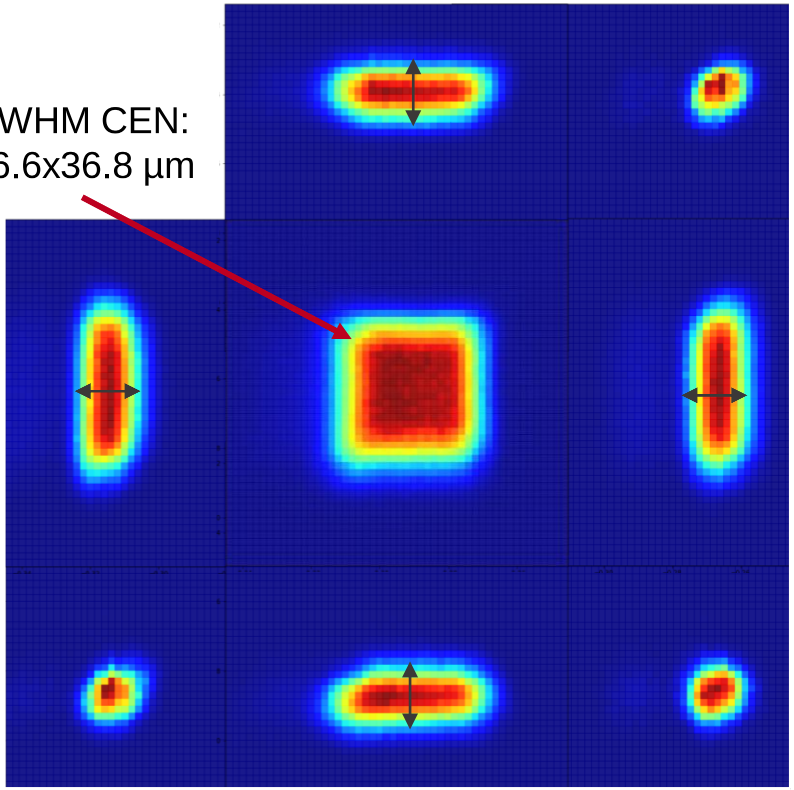
- 16 keV monochromatic beam, 16-bunch mode
- Data from pencil beam scans, beam ≈ 7x5 µm, TH 25%E

3x3: Counters to all edges, center and corners

- North-west corner counter is faulty and was not used

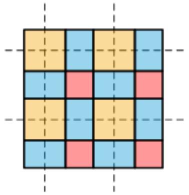
- Symmetric division of the pixel





Characterization Results

Sub-pixel Relocation – 2x2 subpixels, pencil beam scans



2×2 relocation

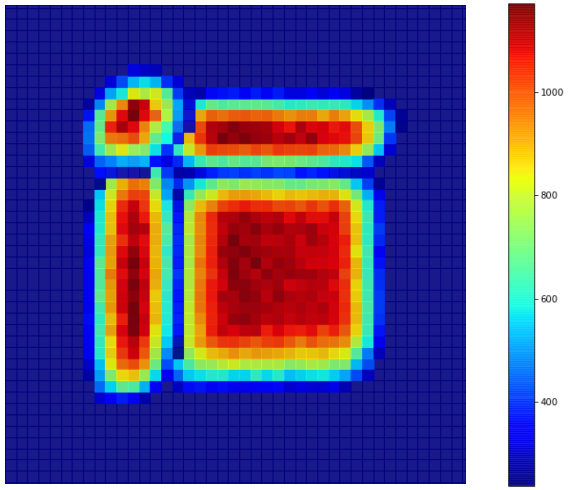
Experimental conditions:

- 16 keV monochromatic beam, 16-bunch mode
- Data from pencil beam scans, beam ≈ 7x5 µm, TH 25%E

2x2: Counters for the Vertical Edge, Horizontal Edge, and Center

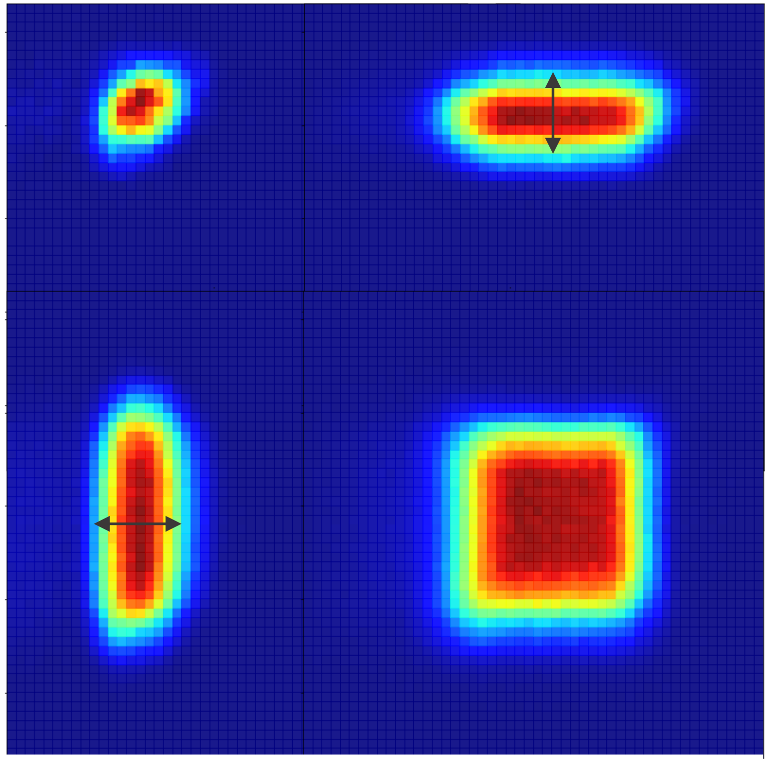
- CORNER is obtained by summing 3 corner counters
- North-west counter is faulty and was not used

- Asymmetric division of the pixel



FWHM CORNER: 13.8x13.4 µm

FWHM H-Edge: 13.96 µm

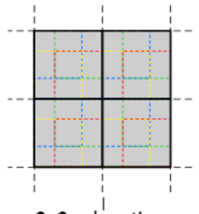


FWHM V-Edge: 14.5 µm

FWHM CEN: 36.6x36.8 µm

Characterization Results

Sub-pixel Relocation – 2x2 subpixels overlapping, pencil beam scans

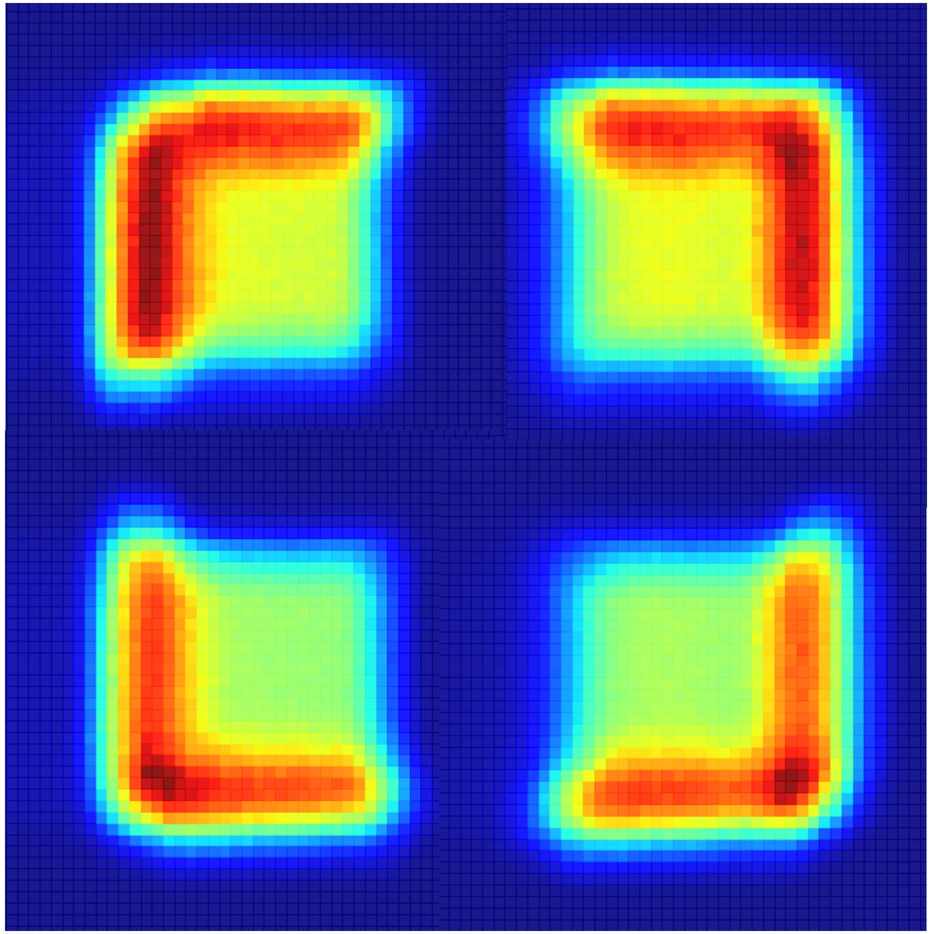


Experimental conditions:

- 16 keV monochromatic beam, 16-bunch mode
- Data from pencil beam scans, beam ≈ 7x5 µm, TH 25%E

2x2 Overlap: 4 counters for 4 symmetric subpixels

- Subpixels obtained by relocating information from the 3x3 mode
- Now done in post-processing
  - ➢ If in the pixel logic, would spare counters (and **pixel area**)



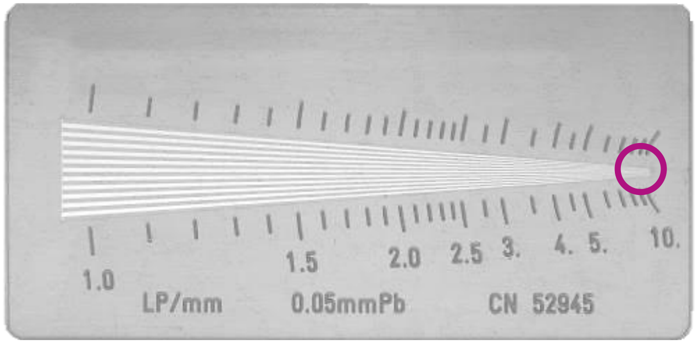
Note: a scenario with smaller pixels and thicker sensors should improve the uniformity of the subpixel shapes in all modes

Characterization Results

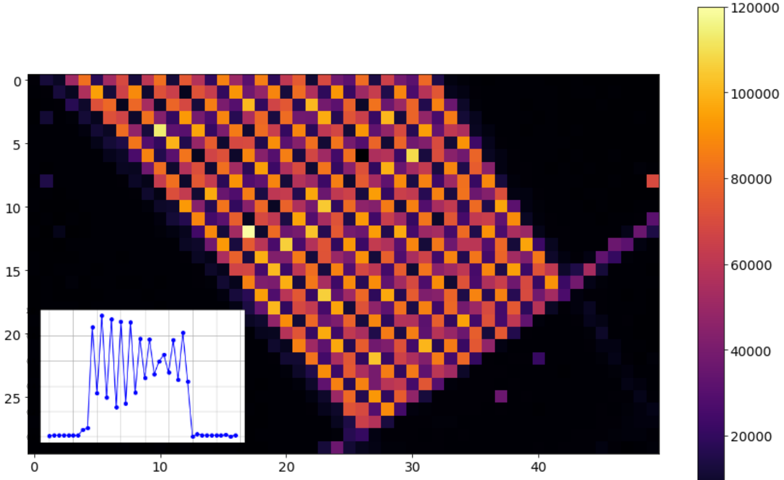
Sub-pixel Relocation performance, full field illumination

Experimental conditions:

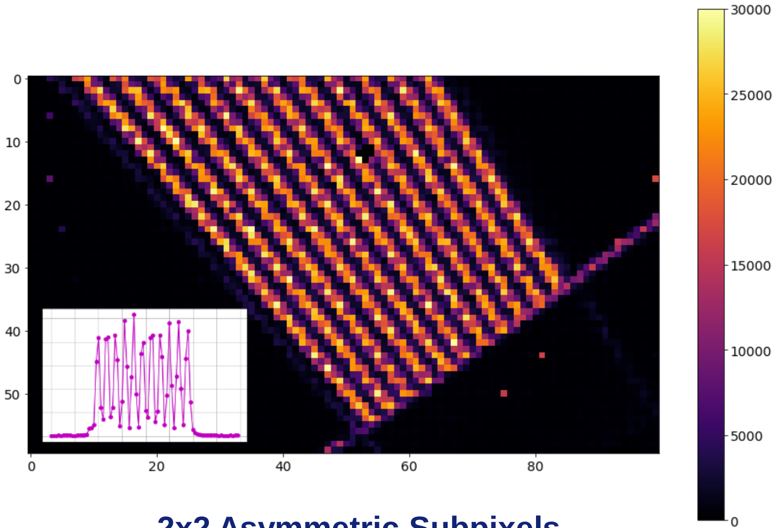
- 16 keV monochromatic beam, 16-bunch mode
- Full-field images of a pattern with the 3 allocation modes
- 0.5 second acquisitions, TH = 25%E
- Results shown here were taken using the **10 lp/mm** region



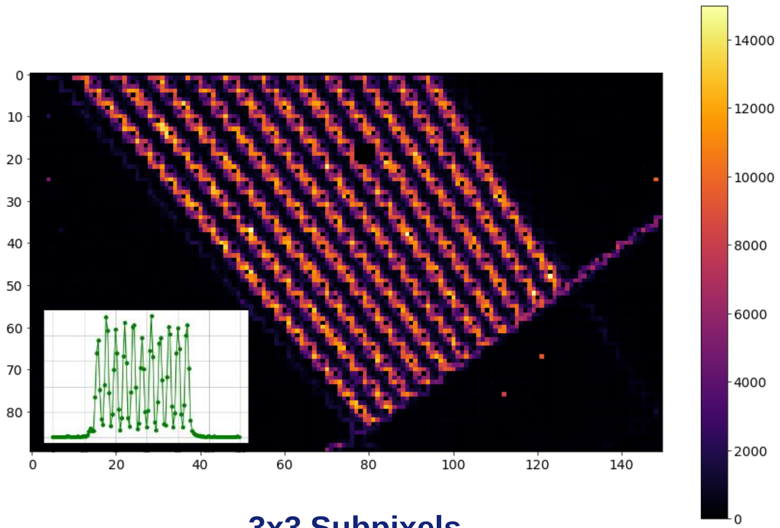
- Raw images (no post-processing for pixel uniformization)



Arbitration



2x2 Asymmetric Subpixels



3x3 Subpixels

Conclusions and Outlook

The methods investigated in SPHIRD work and results are very encouraging

- Count-rate capabilities exceed the current state-of-the-art systems
- Pixel relocation circuitry works as expected

Main technical issues:

- Large mismatch between pixels, in pulse amplitude (gain) and width
- Severe difficulties to bond 50 µm CdTe/CZT sensors on MPW chips

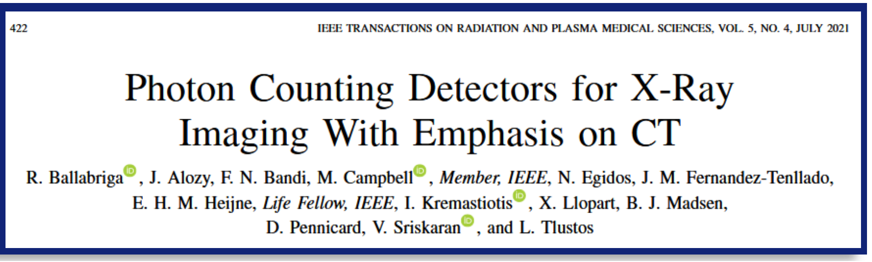
Next steps:

- Test the performance of CdTe and CZT assemblies
- Second test ASIC under development (submitted this summer):
  - Some architecture improvements, better pixel matching and trimming capabilities (pixel equalization)
  - Commercial high-speed data serializer for fast readout

Thank you!

Backup Slides

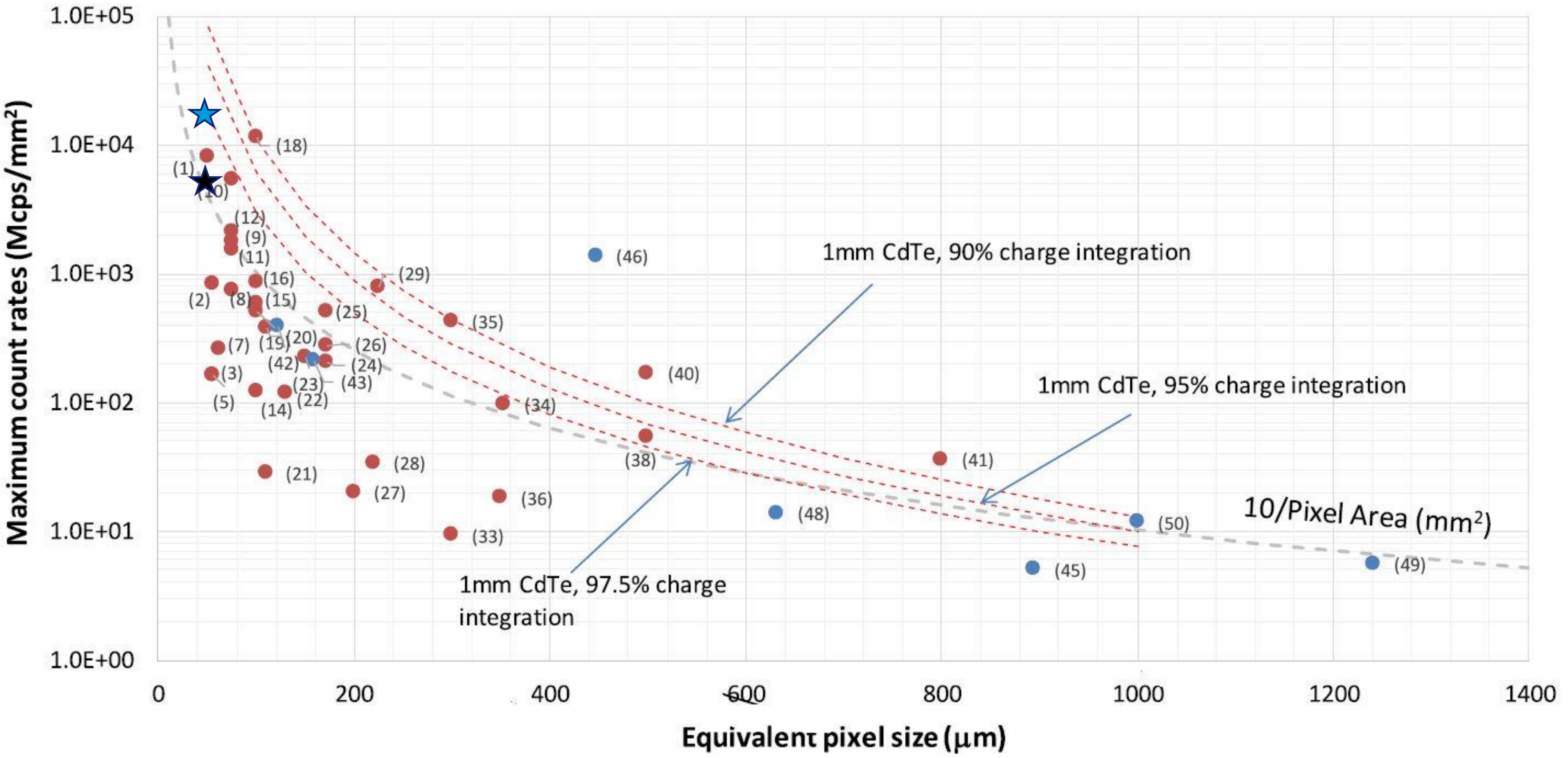
Comparison



422 IEEE TRANSACTIONS ON RADIATION AND PLASMA MEDICAL SCIENCES, VOL. 5, NO. 4, JULY 2021

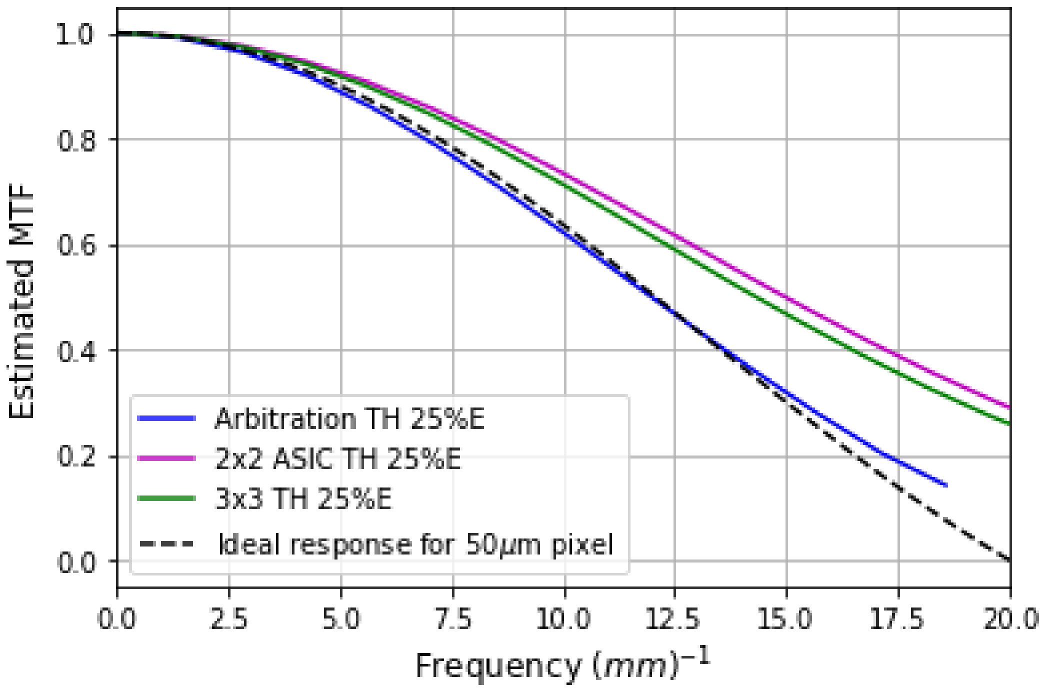
Photon Counting Detectors for X-Ray Imaging With Emphasis on CT

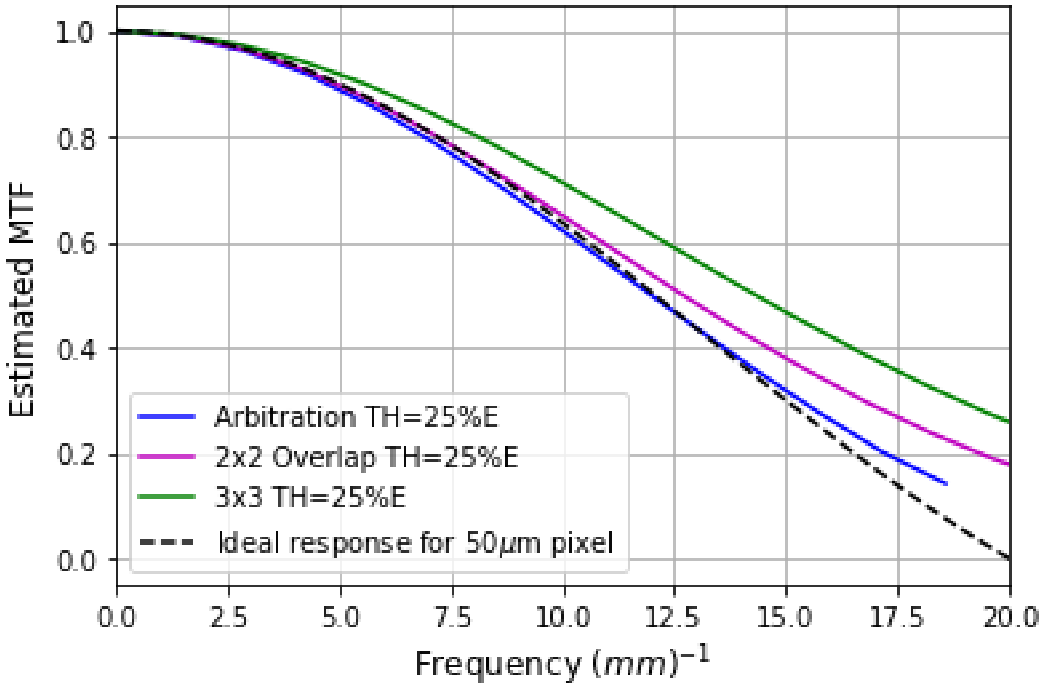
R. Ballabriga, J. Alozy, F. N. Bandi, M. Campbell, *Member, IEEE*, N. Egidos, J. M. Fernandez-Tenllado, E. H. M. Heijne, *Life Fellow, IEEE*, I. Kremastiotis, X. Llopart, B. J. Madsen, D. Pennicard, V. Sriskaran, and L. Tlustos



MTF – Preliminary Results

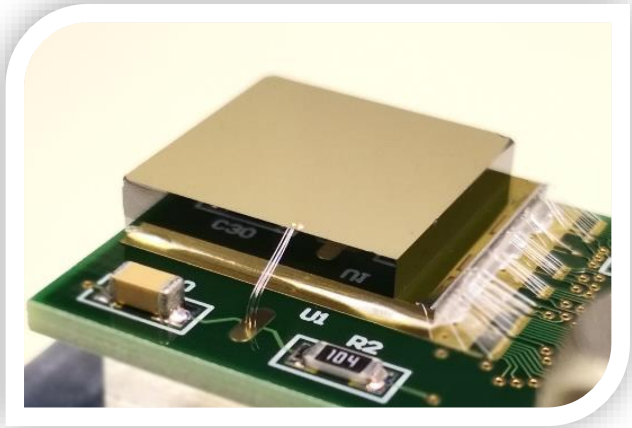
- No post-processing to correct the different pixel sizes in the matrix applied
- Slanted edge technique
- ESF curve fitted with an ERF function

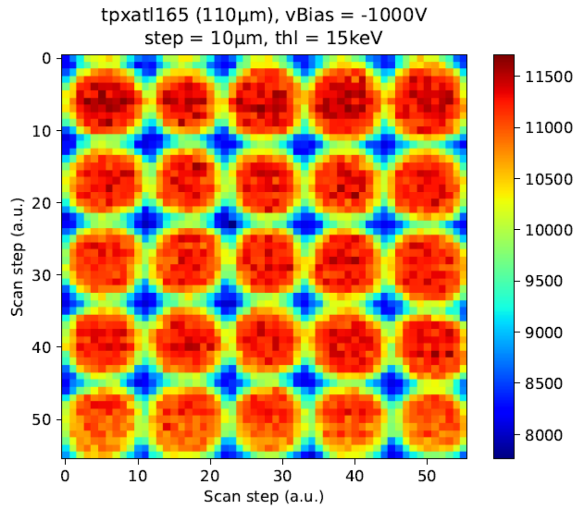


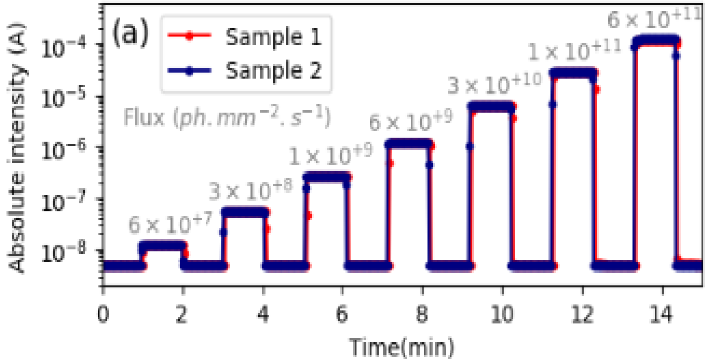


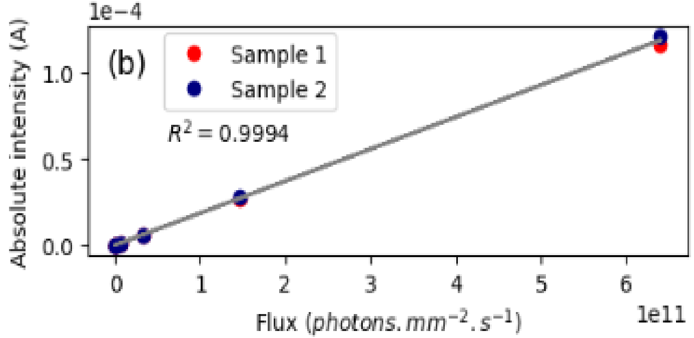
CZT Response

- Tests with 1mm and 2mm thick sensor bonded to a Timepix2 ASIC
- Promising uniformity of the electric field:
  - S. Tsigaridas *et al* (2021), [10.3390/s21092932](https://doi.org/10.3390/s21092932)
- Also promising response to high flux (HF-CZT):
  - O. Baussens *et al* (2022), [10.1088/1748-0221/17/11/C11008](https://doi.org/10.1088/1748-0221/17/11/C11008)





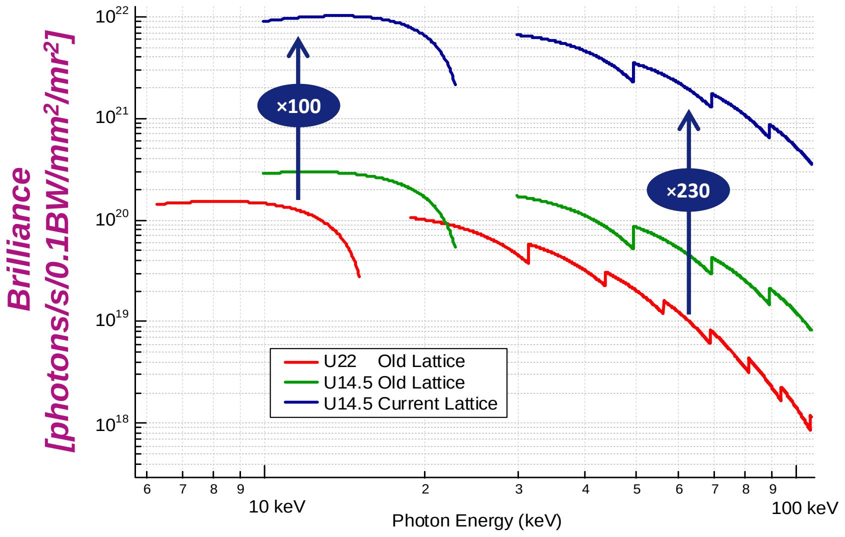


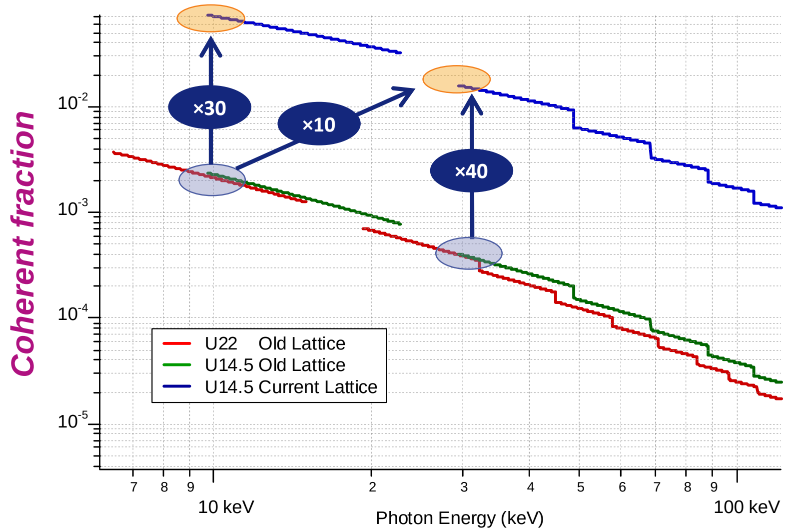


Linearity up to
$6{\times}10^9$ 20 keV ph/sec/100µm pixel

The SPHIRD Project

Motivation





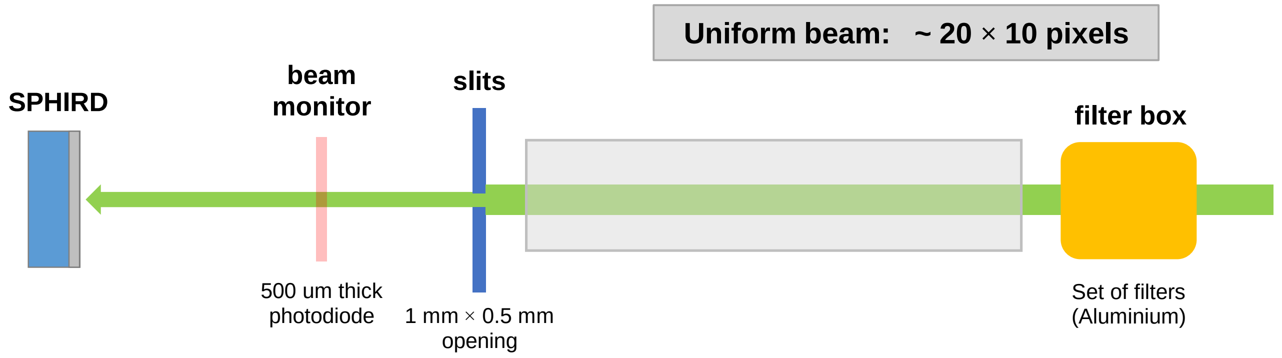
ESRF-EBS:

- Higher photon fluxes, meaning **shorter exposure times**
- Increase of the **coherent** fraction of the beam enables coherent diffraction techniques at high energy: need for **higher angular resolution**
- Push of many experiments towards **higher energy ranges**

→ Demand for fast detectors coping with high fluxes and high frame rates, able to operate at high energies

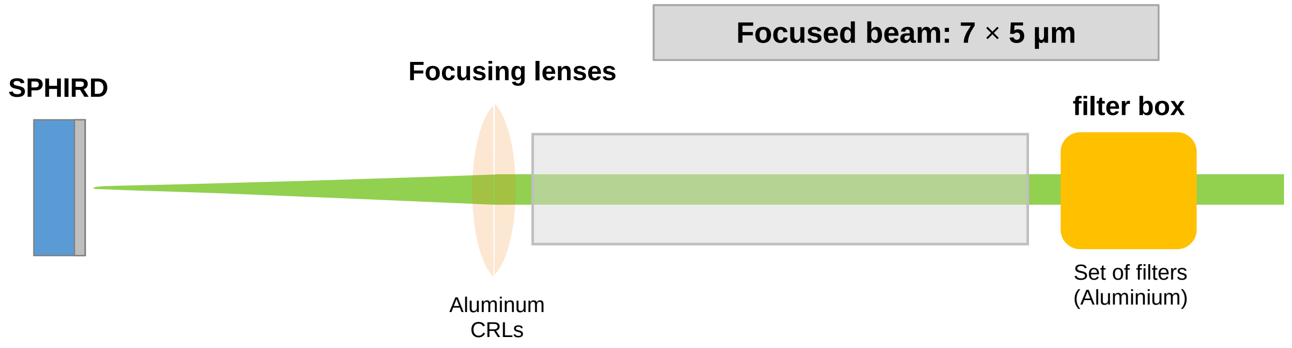
Experimental Setups

1)



Multilayer Monochromator
X-ray beam: 15 keV

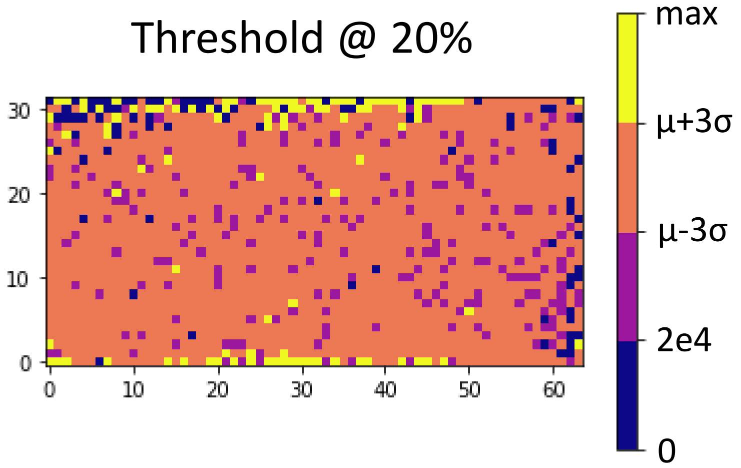
2)

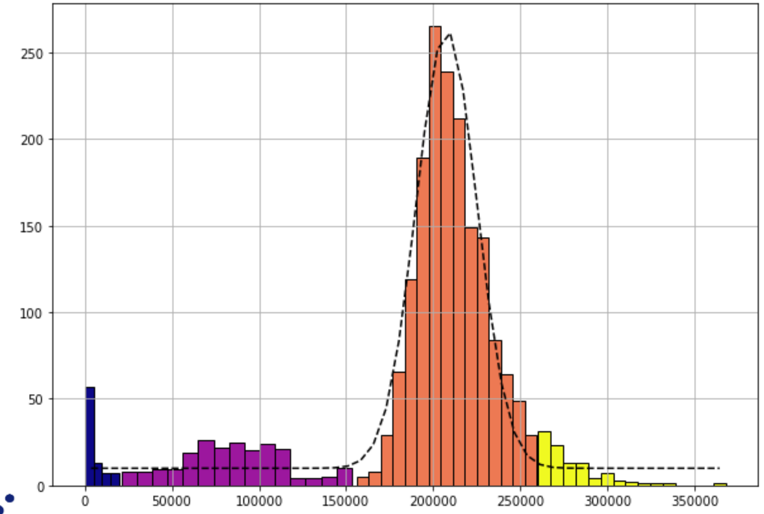


Si Monochromator
X-ray beam: 16 keV

ACF Si Assembly
Full-field images, HV = -200V

Threshold @ 20%





@Threshold = 20% | 50%:

Active pixels(ct > 1): 99.95% | 95.9%
Gaussian pixels: 80.57% | 81.45%

Threshold @ 50%