ePixUHR-35kHz: a read-out ASIC for tender X-ray imaging at LCLS-II with 35 kHz frame-rate

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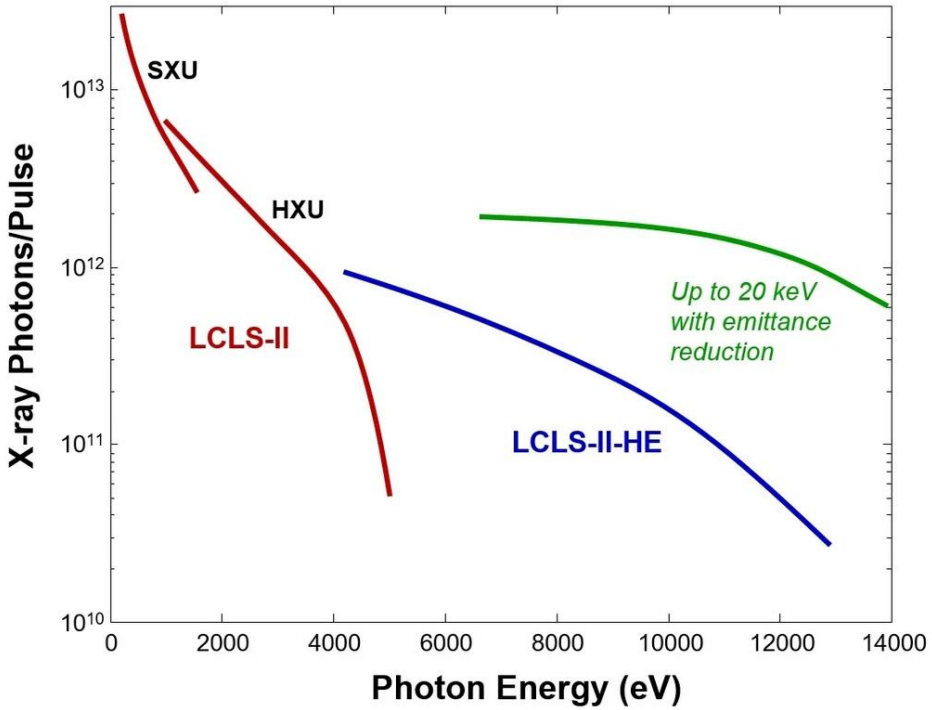
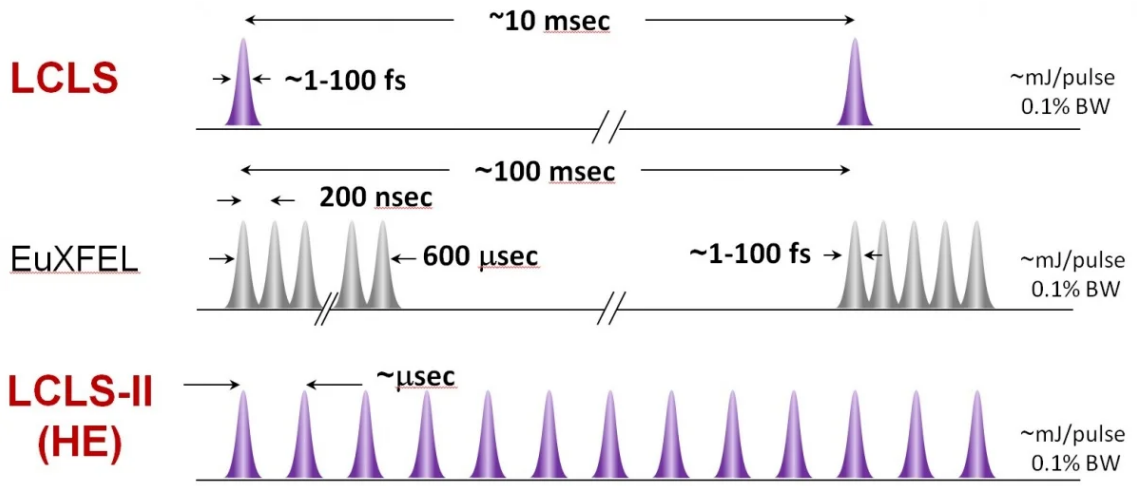
LCLS-II & LCLS-II-HE: revolutionary tools for X-ray science

- LCLS-II will be the first XFEL to be based on continuous-wave superconducting accelerator technology
- Continuous repetition rate of 1 MHz, with photon energies between 250 eV and 12 keV





SLAC long-term X-ray detector development plan

Bigger, Faster, Higher resolution and Higher Energies

With goals built into projects progressively meeting science priorities and requirements

ePixUHR$_{35kHz}$ (2019-2027)

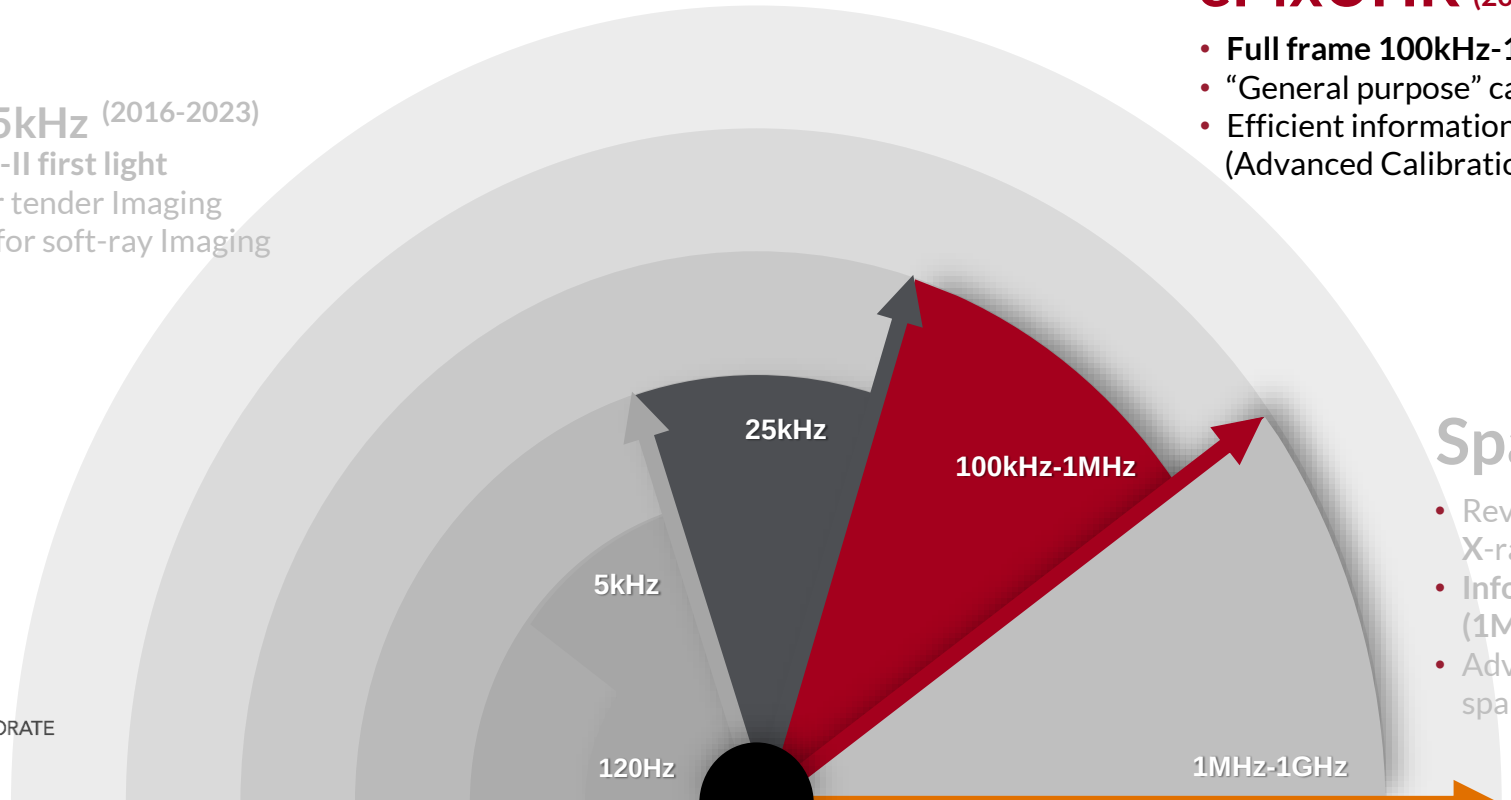
- **Full frame 35kHz for HE first light**
- Sensors for hard X-rays

ePixUHR (2019-2029)

- **Full frame 100kHz-1MHz**
- "General purpose" cameras
- Efficient information extraction (Advanced Calibration / Edge-ML)

ePixHR$_{5kHz}$ (2016-2023)

- **5kHz for LCLS-II first light**
- ePixHR10k for tender Imaging
- ePixHR250M for soft-ray Imaging



SparkPix (2020-2027)

- Revolutionary Experiment Specific X-ray Cameras
- **Information extraction at full rate (1MHz CW, 3GHz burst)**
- Advanced features (triggering, sparsification, zero suppression etc.)

ePix (2013-2018)

- In use at LCLS

Methodology towards higher frame rates

- Large number of detectors to be designed & commissioned in next years at LCLS-II

- **Strategy:**
  - Top-down approach: focus is on delivering detectors systems to meet LCLS-II science program
  - Modularity, following the success story of the ePix family

  - **Sensors:**
    - Sensors compatible with different detectors (pitch, polarity, *etc.*)
  - **ASICs:**
    - CMOS 130 nm node selected: cost-effective, availability & good analog performance
    - "Overhead" of IP blocks development & prototyping (communication, biasing, control, etc.) is spread over multiple projects / fabrication runs
  - **FPGA & readout cards:**
    - Common data protocols & slow-control interface
    - Common readout cards, mechanics, cooling strategies *etc.*.
    - Firmware & software are modular (and open-source!)

https://github.com/slaclab

SLAC Lab

A home for research-facilitating software developed at SLAC. For access requests: #comp-general / #github-slaclab in SLAC Slack

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ePixUHR-35 kHz ASIC: overview

Summary of main specifications

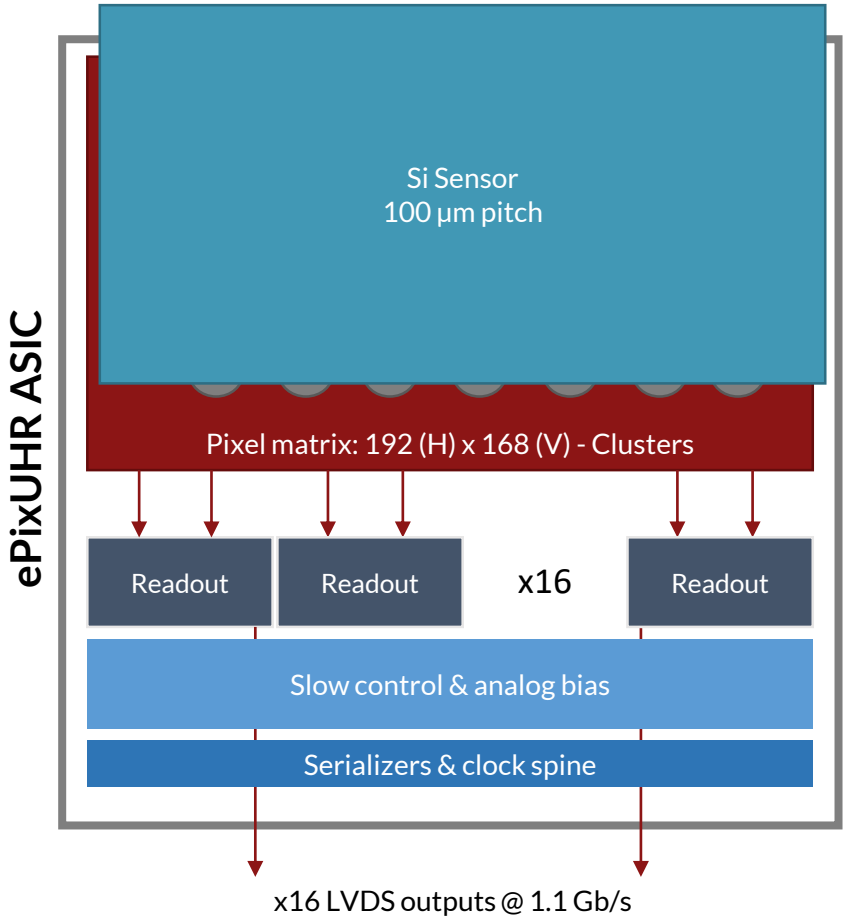
- **Noise:** <100 e^-, single-photon resolution at 4 keV
- **Dynamic range:** 10^4 @ 8keV
- **Size:** 192x168 pixels with 100 µm pitch,
  ~2x2cm^2, 3-side buttable (camera up to 4Mpix)
- **Frame-rate:** 35 kHz
  (pixel and ADC ready for 100kHz operation)

Goals of 1st prototype:

- Demonstrate path towards >25kHz detector on single ASIC
- Retire risks associated with TSV and 3D stacking
- Evaluate integration and performance at LCLS-II beamline

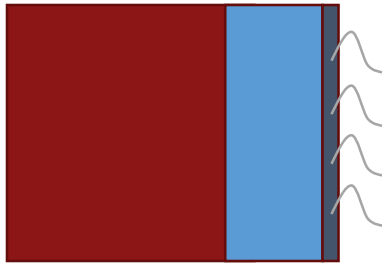
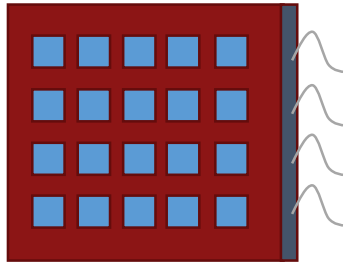
Goals of 2nd prototype:

- Optimize pixel front-end circuitry for 35 kHz operation

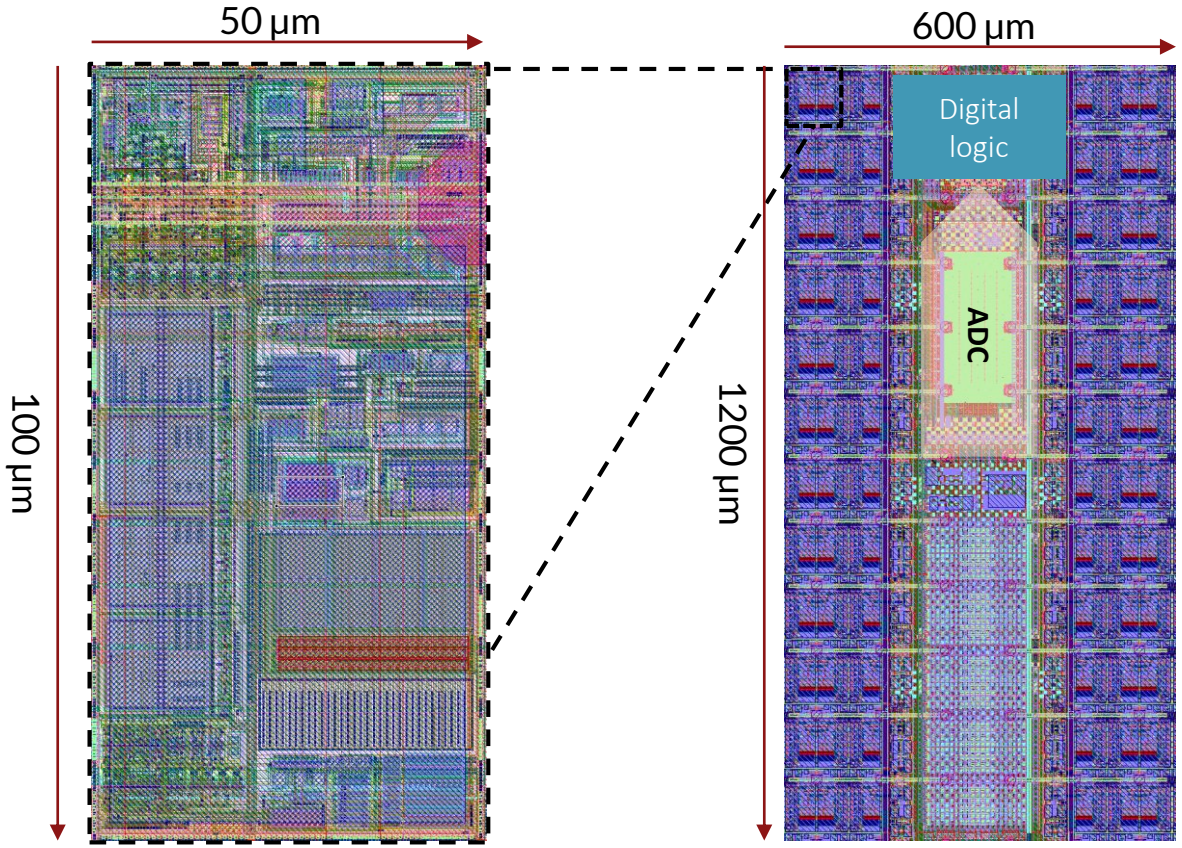


Architecture towards higher frame rates

Move A/D conversion closer to pixels and increase parallelism

	ePix	ePixHR	ePixUHR
Type of backend	Analog	Digital	Digital
A/D approach	Off-chip	Column-parallel	Cluster
Architecture	Analog Mux	1 MSPS Sigma-Delta ADC for each column	8 MSPS SAR ADC for 72-pixels cluster
Rate	1 kHz	7.5k Hz	100 kHz – 1 MHz
ASIC floorplan (top view) Pixel matrix ADCs Slow control & readout	 192 x 176	 192 x 144	 192 x 192

Pixel matrix architecture



Pixel

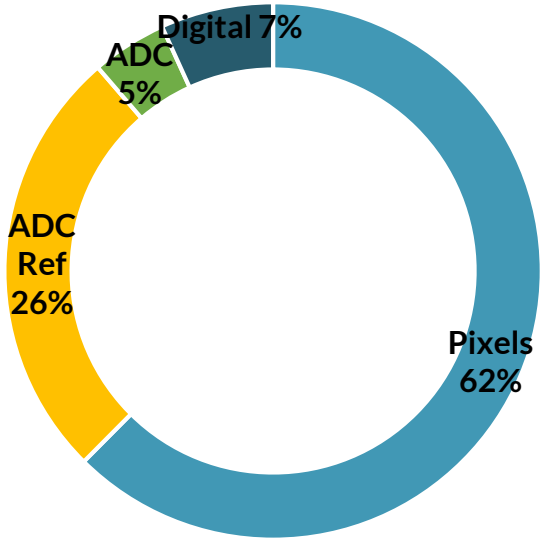
- Operates at 35 kHz – 1 MHz
- Si sensor: 100x100 µm^2
- ASIC: 50x100 µm^2

Cluster

- 72 pixels → 1 ADC @ 8 MSPS
- Digital logic for pixel configuration and readout

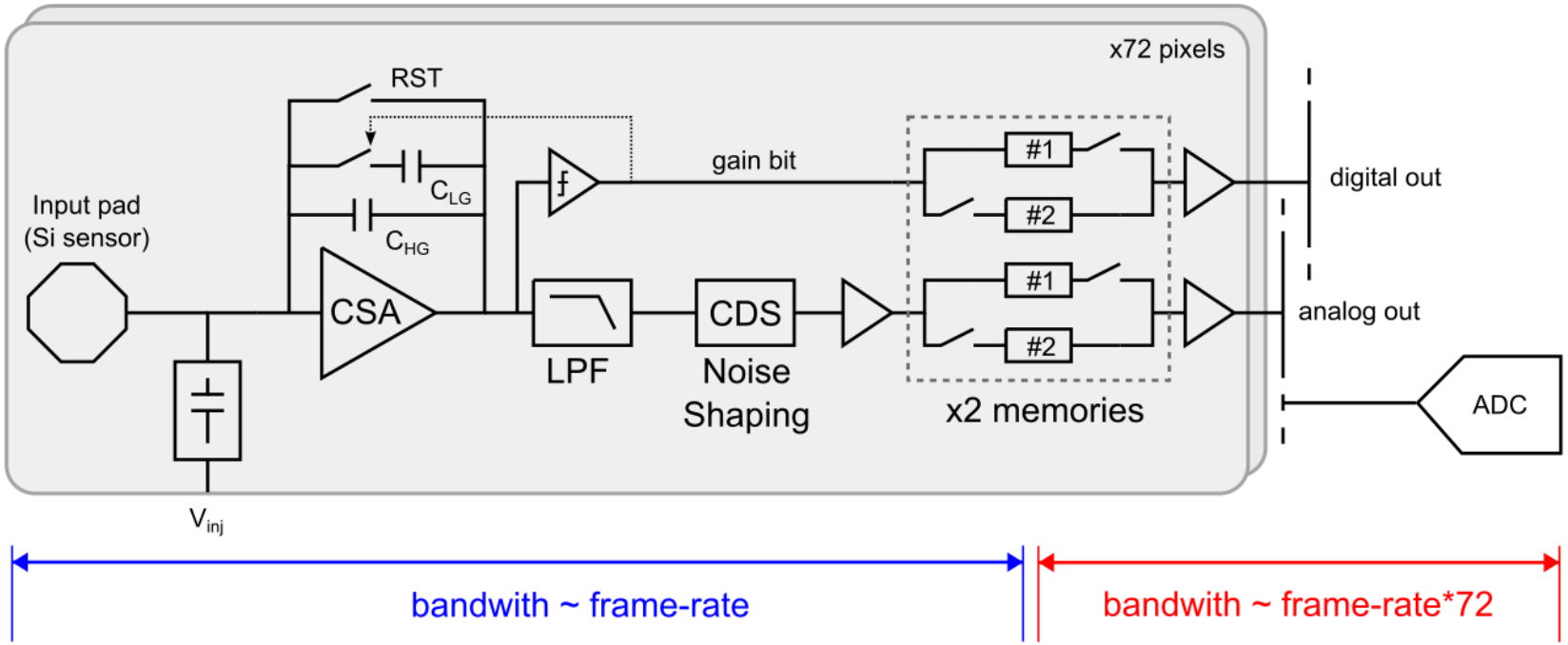
Tile to create pixel matrix: 192 x 156

- 14 clusters in vertical direction
- 16 clusters in horizontal



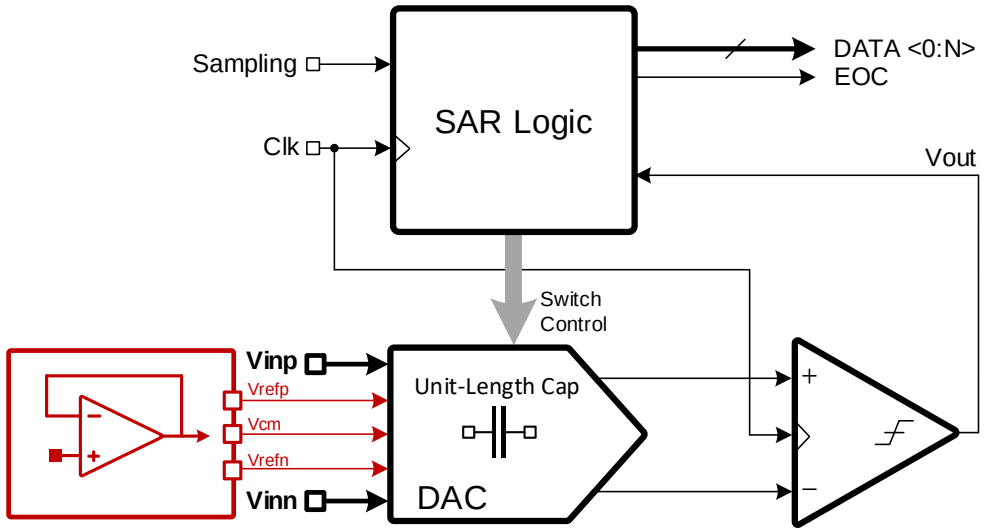
Power consumption of different blocks in matrix (power density: 0.94 W/cm^2)

Pixel analog front-end

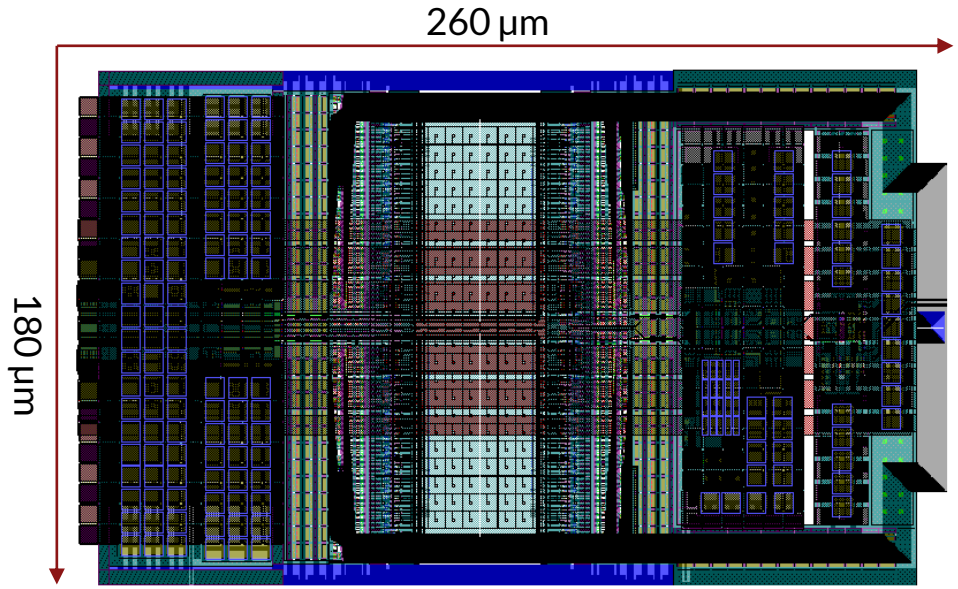


- **Challenge:** meet dynamic range and noise performance in a scaled CMOS tech with low supply voltage
- Auto-gain switching architecture adapted from previous ePix detectors:
  - each pixel switches from HG (or MG) to LG when input charge exceeds a programmable threshold
  - 'CompEn' feature = prevents incomplete settling at gain-switching point
- 'Correlated pre-charging' circuitry reduces noise after gain-switching [1]

Analog-to-Digital Converter



Simplified ADC block diagram

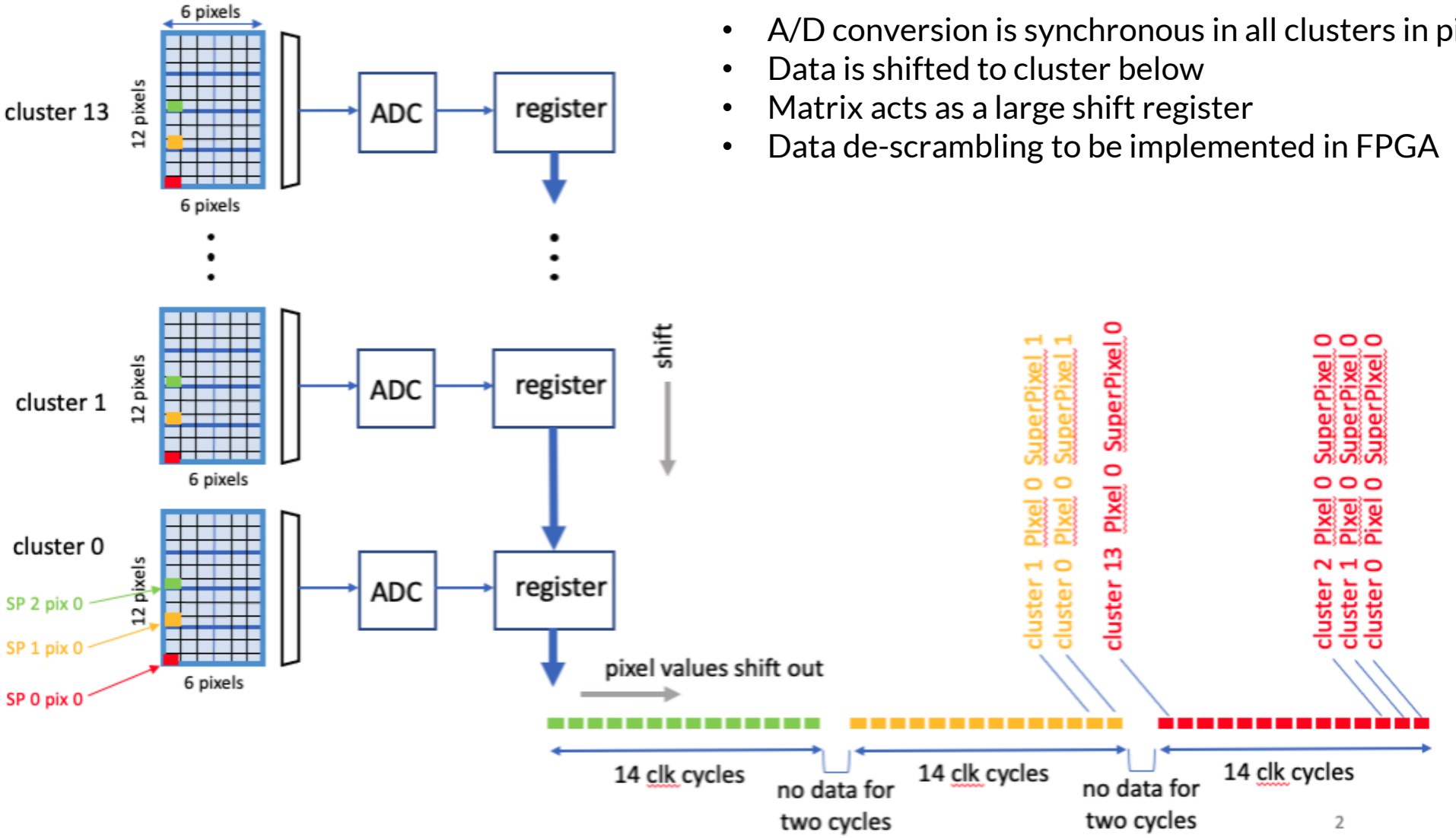


Layout of ADC

12b Differential Successive Approximation Register (SAR) architecture:

- Optimized switching scheme to reduce both area and power consumption (on ADC local reference buffers)
- Novel circuit to perform built-in single-ended to differential conversion
- Based on custom-designed MOM capacitors with differential metal strips [Harpe, JSSC'19]
- Total of 384 ADCs + local reference buffers operating synchronously in pixel matrix

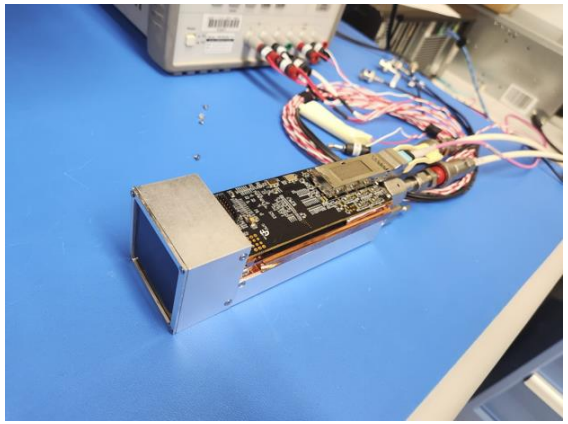
Moving data to the ASIC periphery



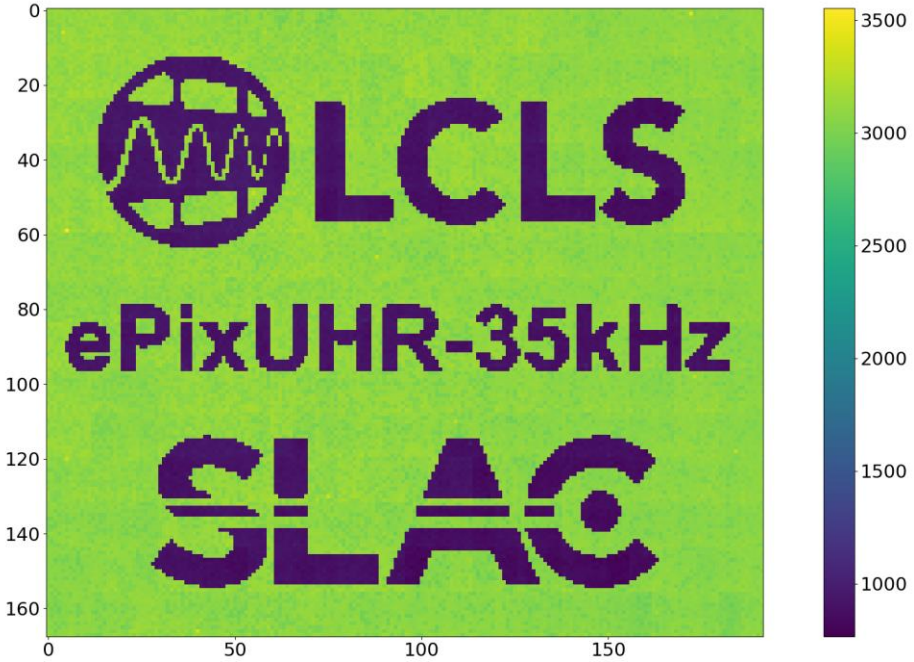
- A/D conversion is synchronous in all clusters in pixel matrix
- Data is shifted to cluster below
- Matrix acts as a large shift register
- Data de-scrambling to be implemented in FPGA

Results – prototype system

Prototyping carrier



Prototyping camera



Pixel matrix test-pattern obtained at a clock frequency of 35 kfps

- First prototype readout architecture is fully functional up to the target frame-rate of 35kHz
- ASIC has been assembled on prototype camera system with cooling block (no Si sensor yet)

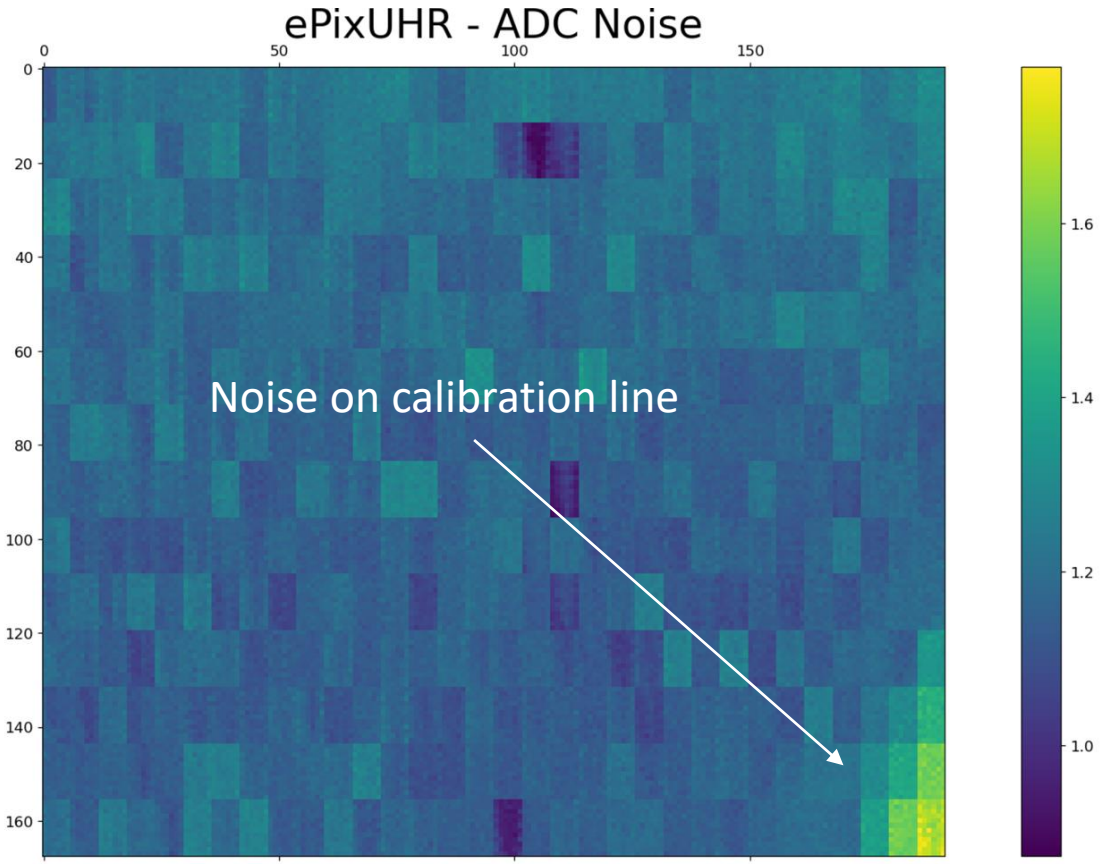
Results – ADC matrix (x384)

Preliminary

- ADC dynamic range: 650mV
- ADC resolution:
  - 12b during calibration (1 ADU = 150uV)
  - 11b during pixel readout (1b becomes gain bit)

- **Results:** no missing codes in any of the 384 ADCs, linearity better than 0.2% (limited by test setup)

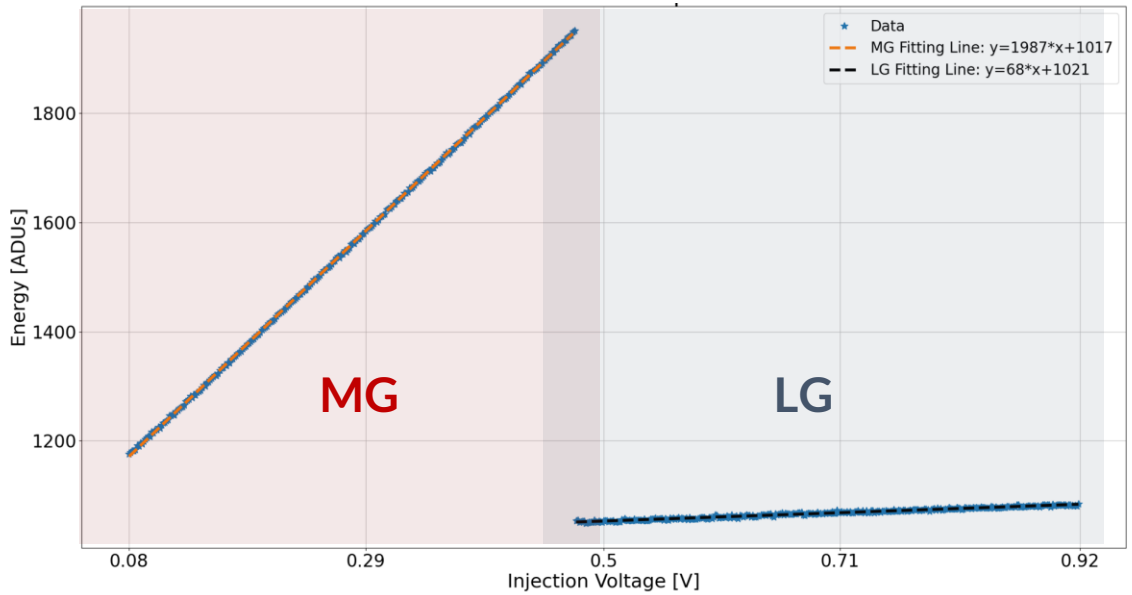
- Hard to evaluate ADC performance because of limitations in ASIC/test setup:
  - Can only test all ADCs simultaneously
  - Test voltage distributed across all matrix
  - Noise <1.2 ADUs (limited by test setup)



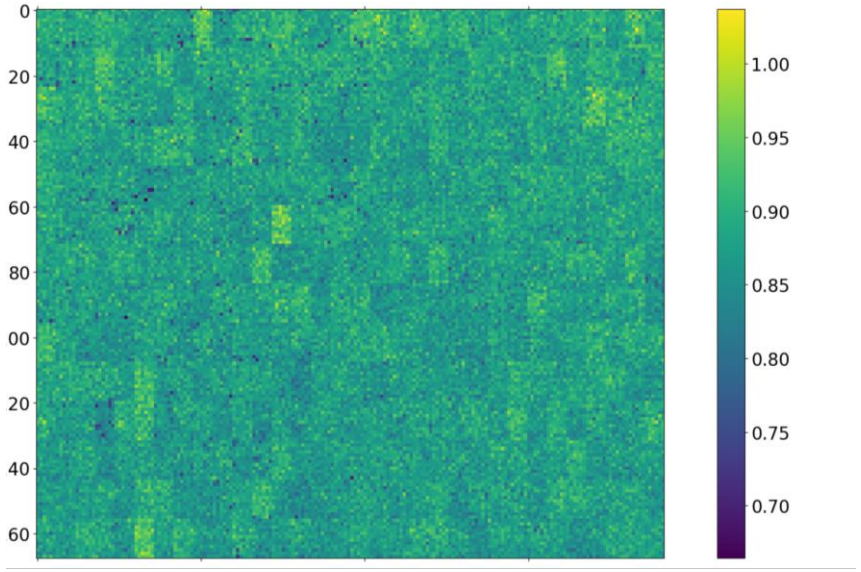
Results – Pixel response

Preliminary

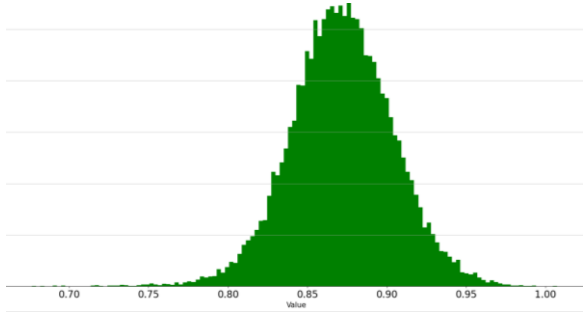
Response of full-readout chain with pixel injection circuitry, pixel configured in auto-gain switching mode



Noise map of pixels in High-Gain mode [ADUs]



Pixel noise distribution

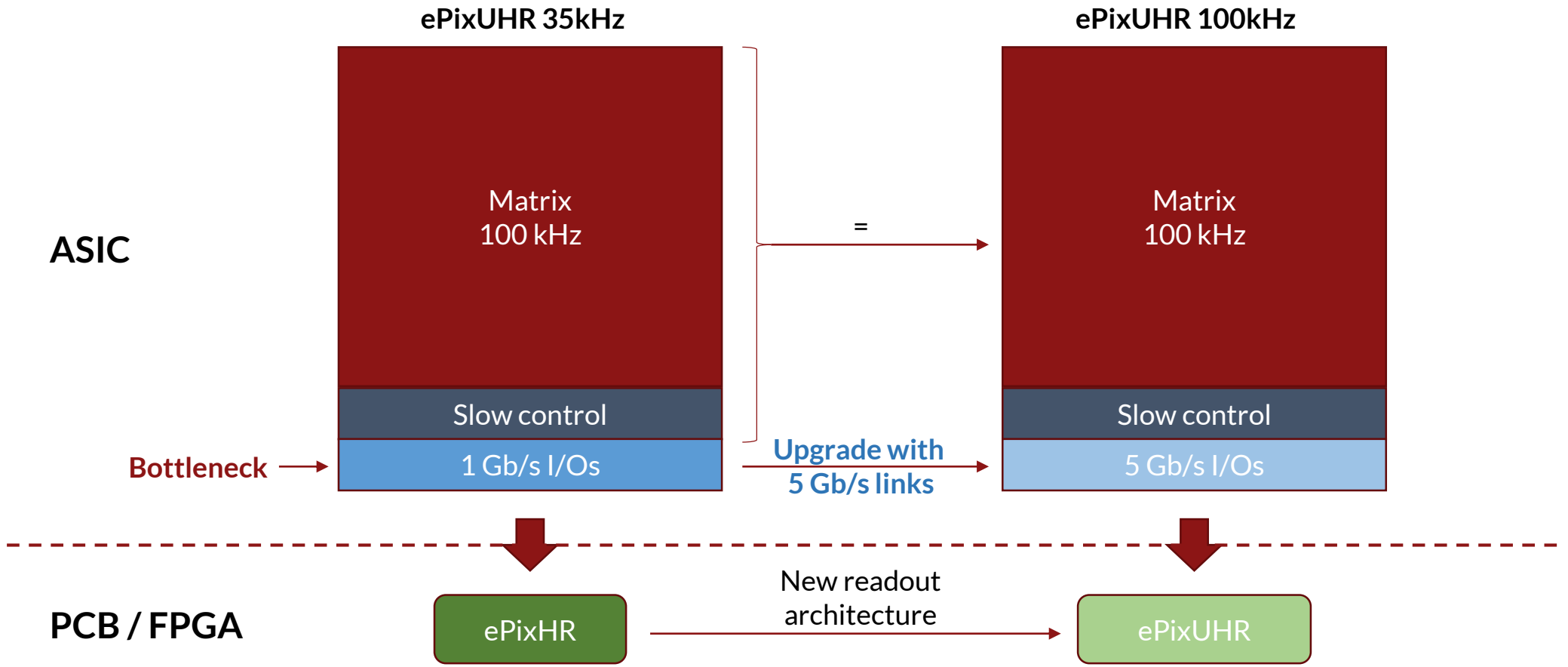


- Default setting: each pixel switches from HG/MG to LG
- 'Correlated pre-charging' reduces noise after gain-switching [1]
- 'CompEn' feature = prevents incomplete settling at gain-switching point

[1] L. Rota et al, *DOI 10.1088/1748-0221/14/12/C12014*

Towards ePixUHR-100kHz

- Current design will be upgraded with 5 Gb/s links (CML/SST) (2024)
- New FPGA readout architecture is currently being designed (2024)



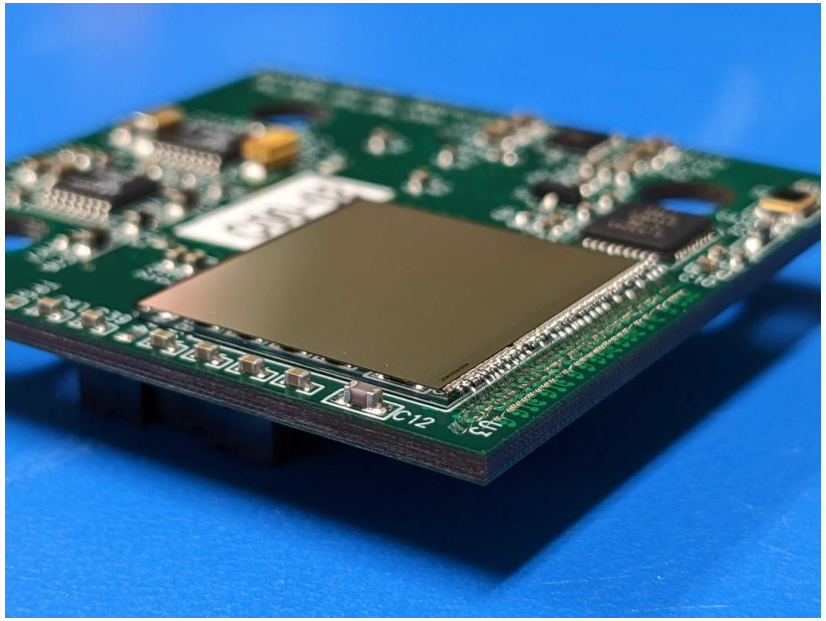
Summary

Summary

SLAC is developing a novel charge-integrating, high-frame rate ASIC for LCLS-II-HE

Status:

- Designed 1st prototype on CMOS 130 nm technology
- ASIC is functional at nominal frame-rate of 35 kfps
- Pixel tested with integration times as low as 400ns (1 MHz operation)

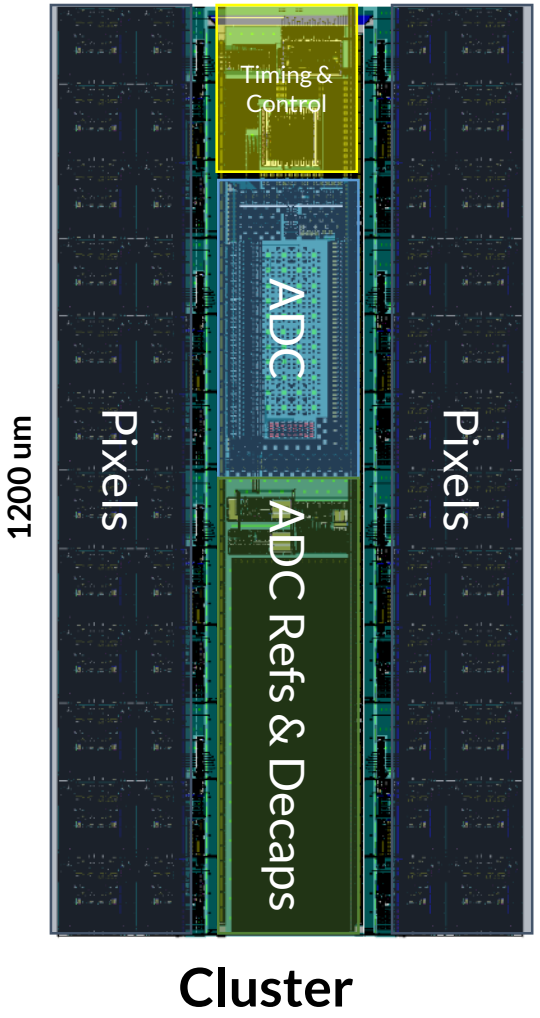


Next steps:

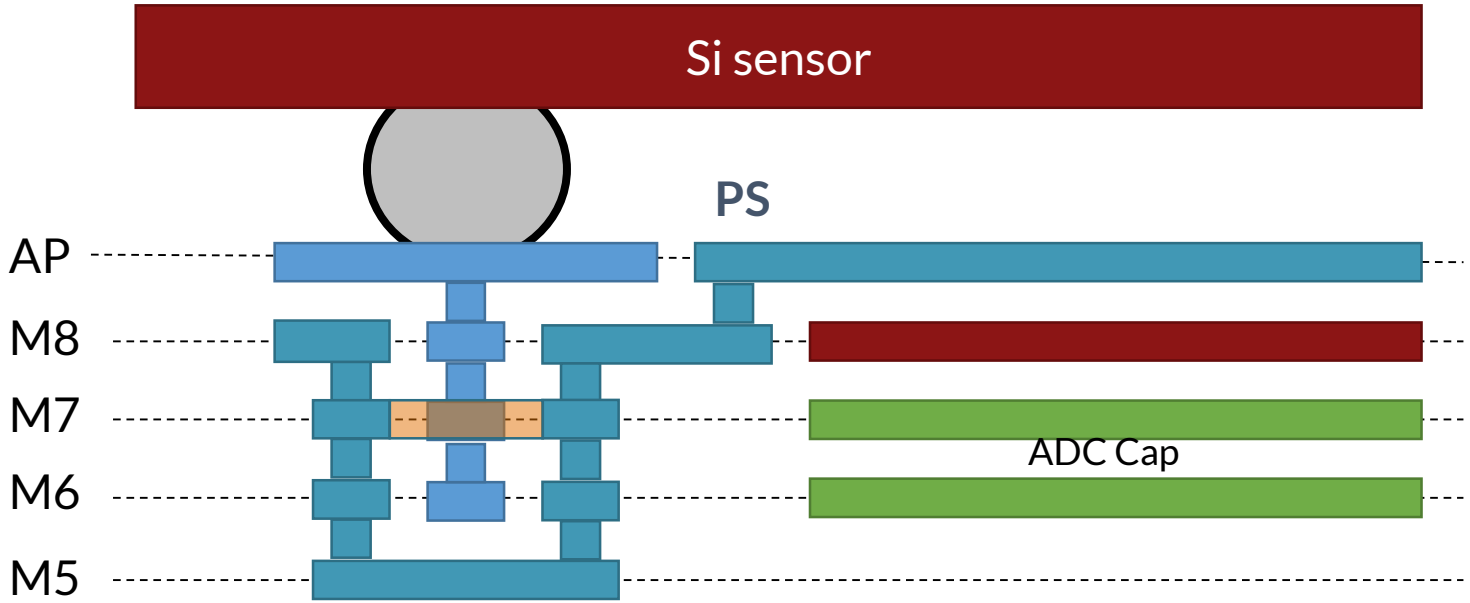
- Characterization performance with bonded Si sensor
- Integration with LCLS-II DAQ at beamline has started (with both emulated ASIC and real ASIC)
- **35 kHz:** 2nd iteration with optimized pixel performance in Q4 2023 / Q1 2024
- **100 kHz:** 1st prototype of ePixUHR-100kHz in mid Q2024

Backup slides

Cluster & pixel layout



- Distributed ADCs and dig. logic in matrix → pixel circuitry displaced
- Need to re-route from bump pad to pixel input
- Can be done on-ASIC → do not need special Si sensor
- Routing and shielding implemented in SparkPix-ED

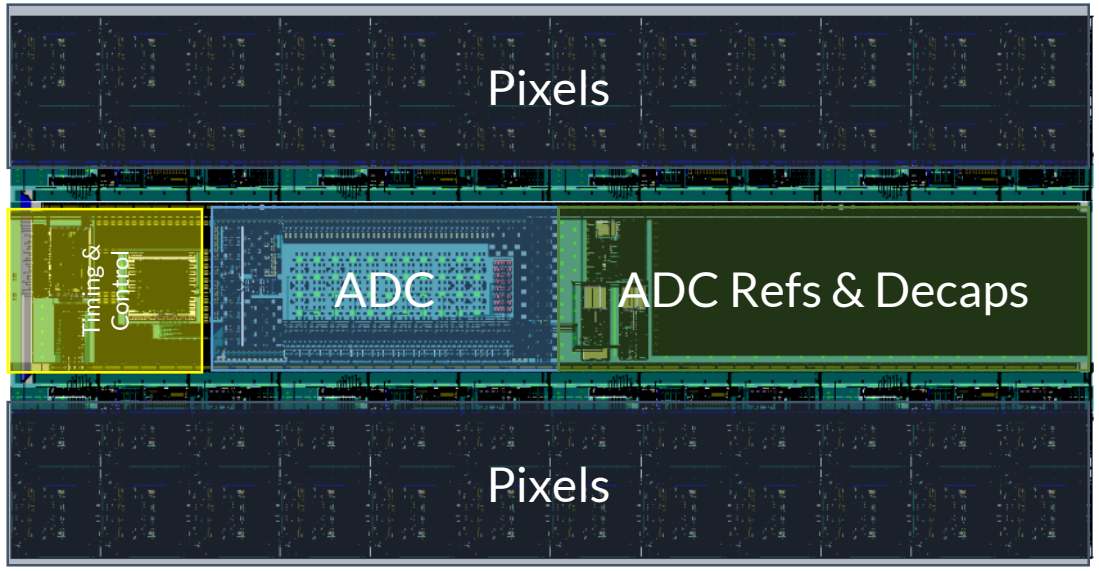


Cluster & pixel layout

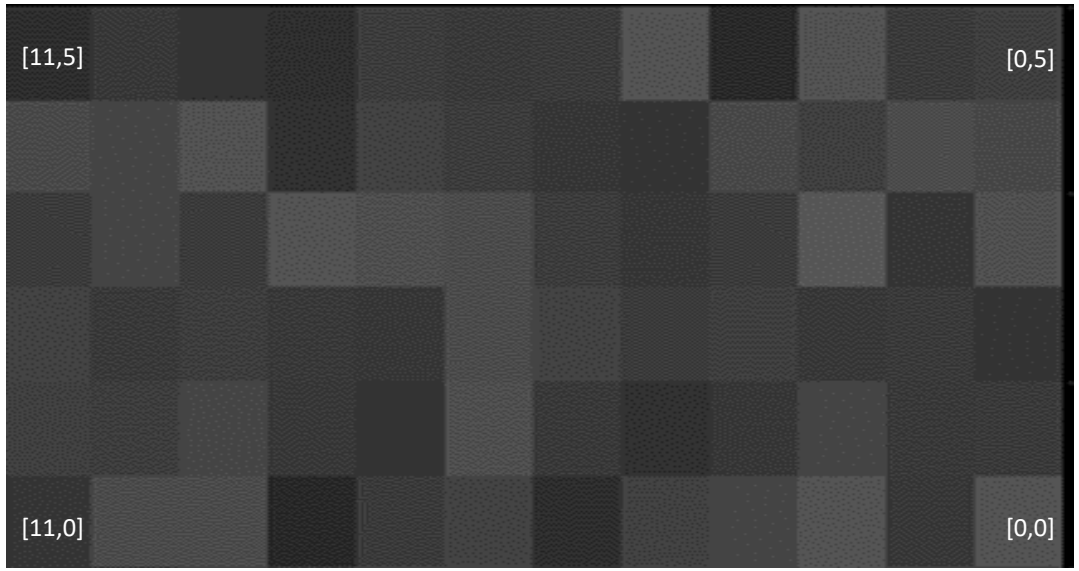
- Noise across pixel in a cluster is “uniform”: no visible difference between pixels above ADC and pixel above “analog” front-end

→ Shielding + RDL of bump connections on ASIC demonstrated

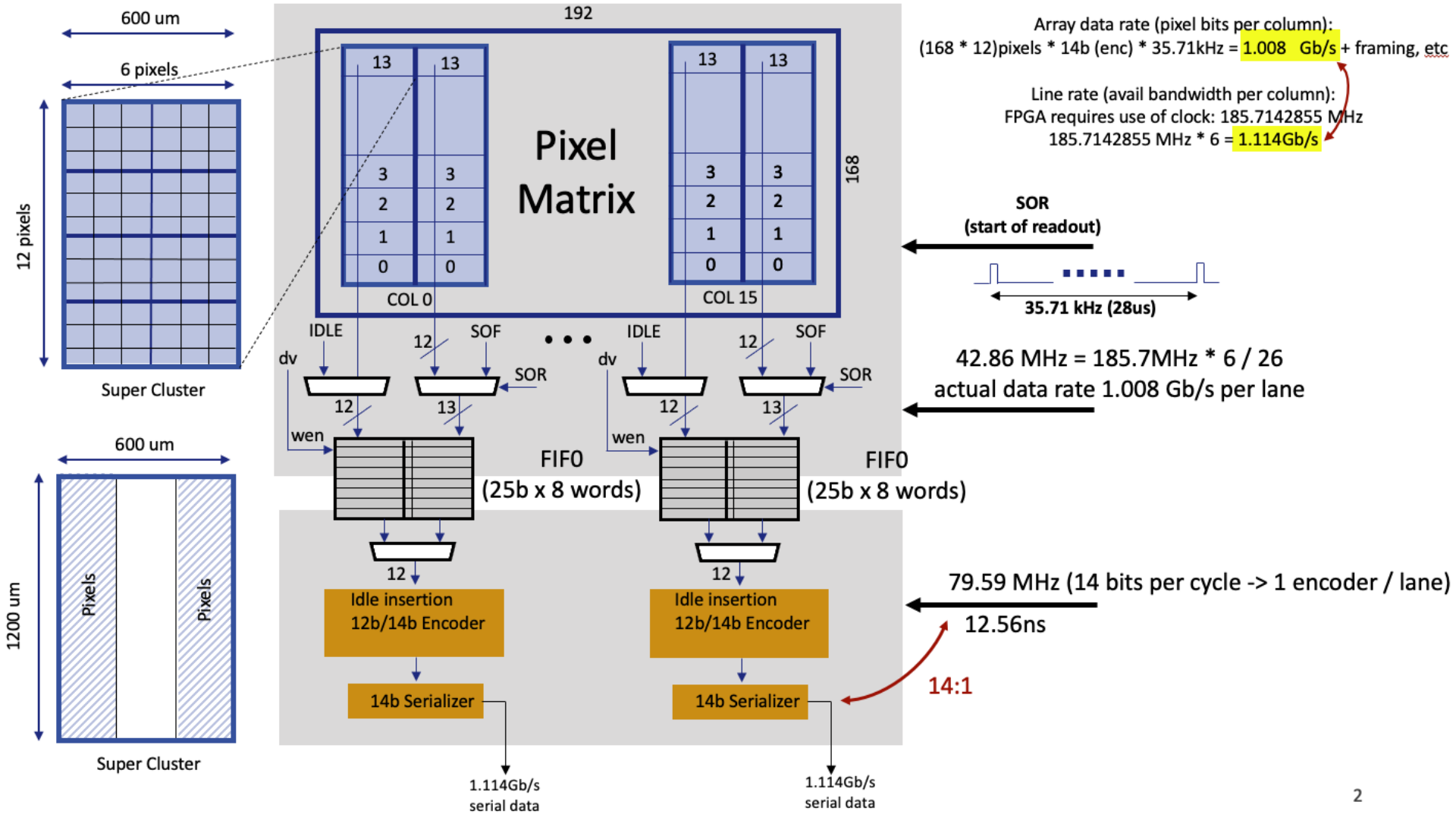
Cluster Layout



Cluster Noise Map

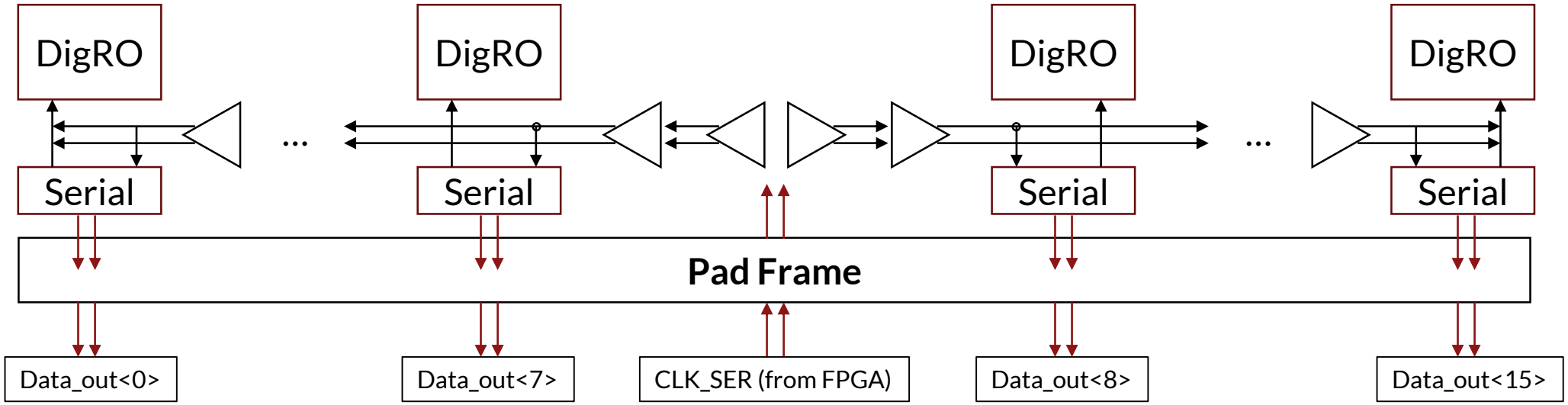


ePixUHR digital readout logic



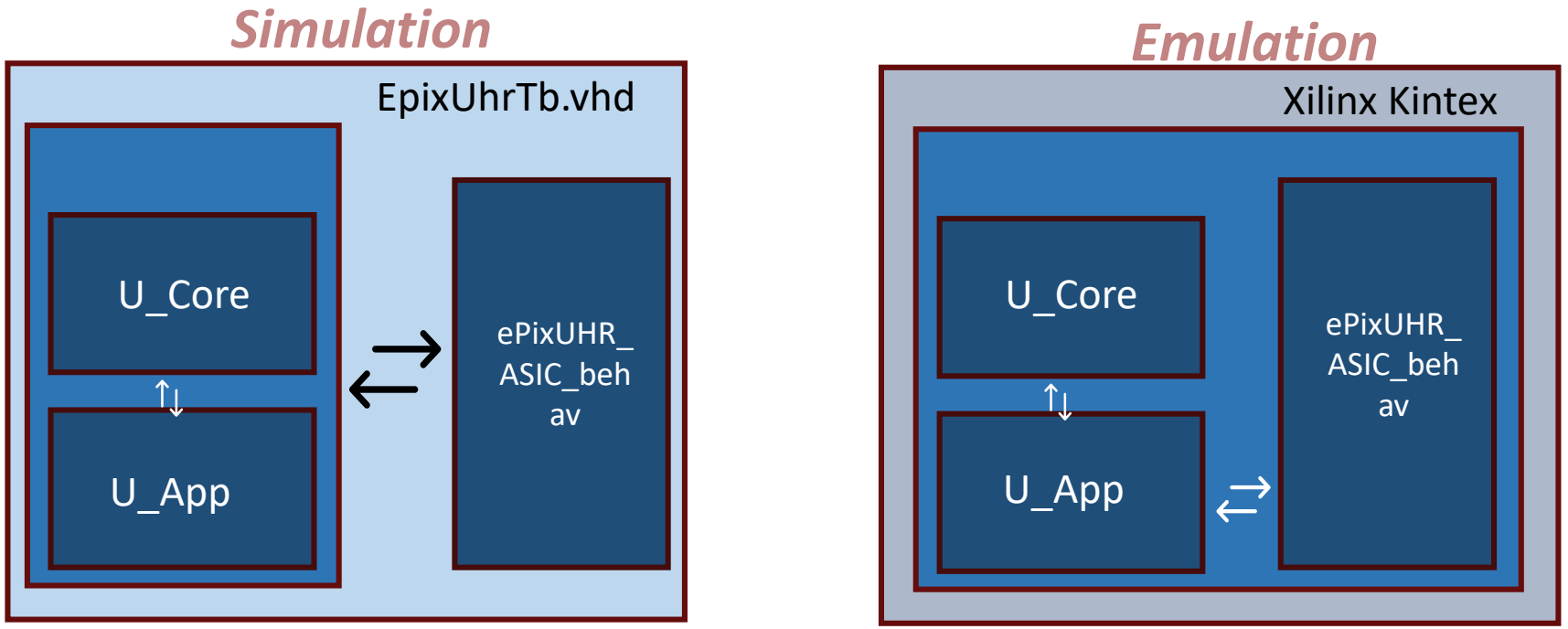
Clock distribution and serializer

- Digital balcony with data path split into multiple identical blocks (DigRO)
- Clock is generated by FPGA or external PLL
- CMOS clock spine with duty-cycle re-generation circuit
- Serializers generate local lock for each DigRO, skew is handled in FPGA
- Fully functional up to >1.1 Gbps with forced air cooling



ASIC-FPGA codesign

- Having a behavioral model of the ASIC allows us to **speed up the firmware/software design** of the camera.
  - Ease the testing and verification of the ASIC logic before the tape-out.
  - Development of FW/SW and integration with DAQ can now run in parallel to the ASIC fabrication.
- We target the **emulation of the ASIC inside the FPGA** (done for Fabulous, and under progress for ePixUHR).



Methodology: co-design

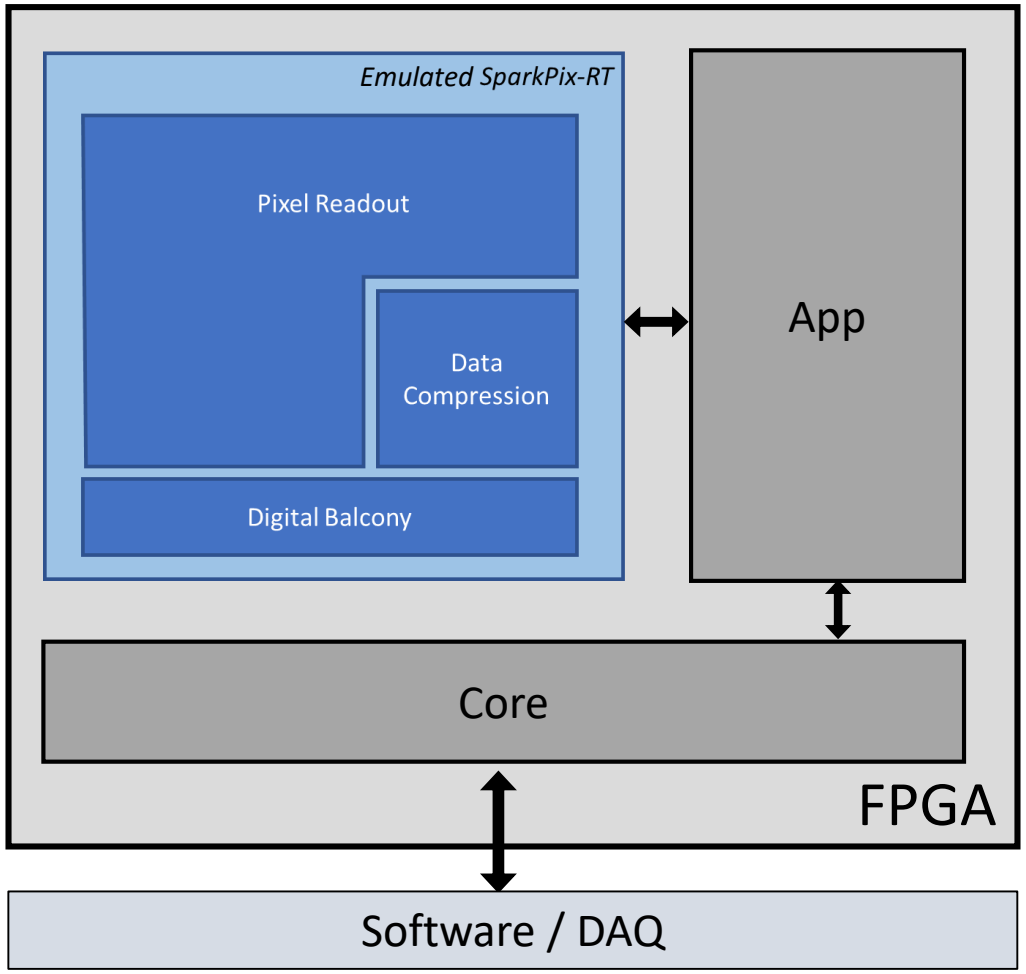
- Data reduction on-ASIC → must ensure data quality and integrity after reconstruction
- Industry-standard verification frameworks (UVM) are very powerful, ***but…***

We developed an agile verification frame-work:

- Development of ASIC and FPGA digital logic is done in parallel (not sequentially)
- Simulate full ASIC + FPGA + Software stack
- Verification code = Deployment code
- Enable emulation of ASIC within FPGA

Additional benefits:

- Integration with LCLS-II DAQ starts while ASIC in fab
- Enables design space exploration of heterogeneous architectures: co-design of detector



P. King, L. Ruckman, B. Reese, C. Bakalis, D. Doering – TID Electronics & EDGE Computing Systems, SLAC
*Ruckman, Larry, et al. "A Methodology for Digital ASIC, FPGA and Software Development and Verification." 2022 IEEE NSS/MIC