

X-ray Detectors for LCLS-II with real-time information extraction: the SparkPix family

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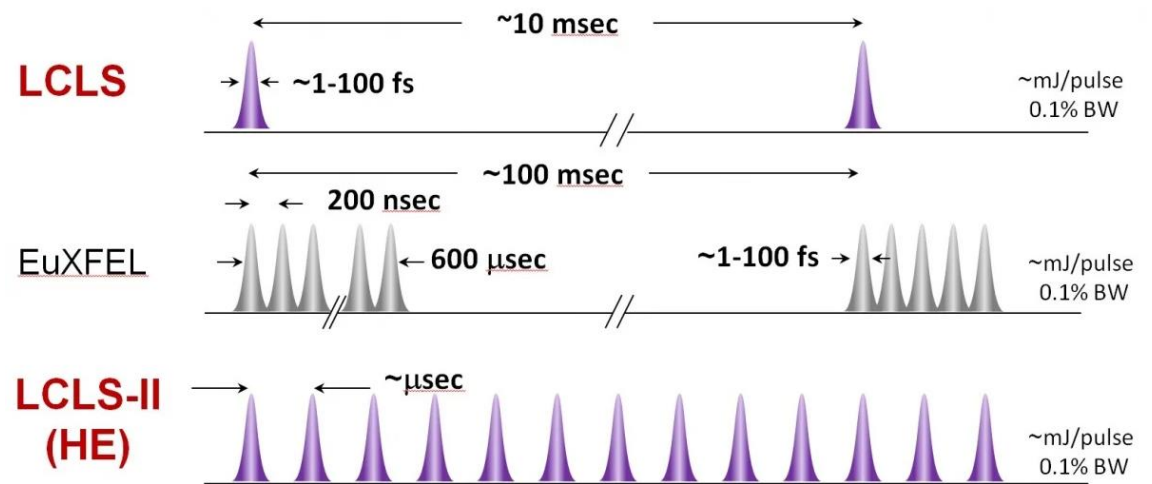
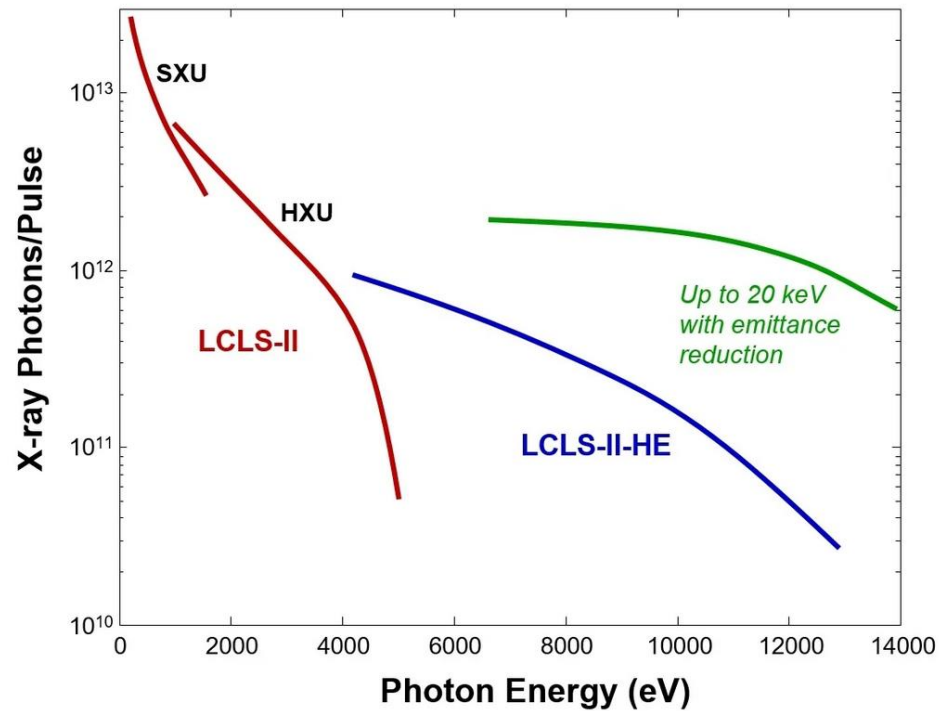
LCLS-II & LCLS-II-HE: revolutionary tools for X-ray science

- LCLS-II will be the first XFEL to be based on continuous-wave superconducting accelerator technology
- Continuous repetition rate of 1 MHz, with photon energies between 250 eV and 12 keV



LCLS-II & LCLS-II-HE: revolutionary tools for X-ray science

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LCLS-II: the data challenge



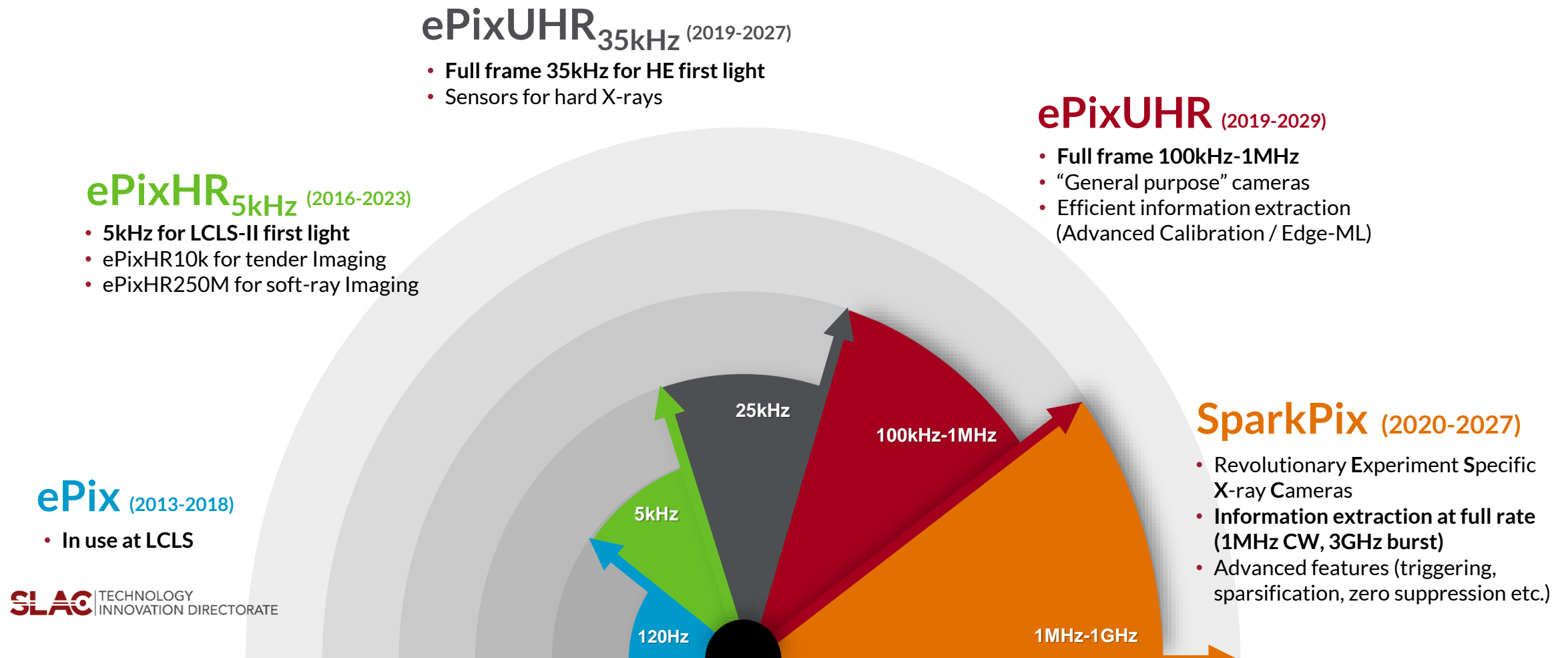
- Moving data through the detector layers (ASIC, FPGA, DAQ) is not the only challenge
- **Data analysis needed** during data collection:
 - Must be able to get **real-time feedback** and the quality of data-taking (~ 1 sec)
 - Must be able to get feedback about the quality of the acquired data with a latency lower (~ 1 min) than the typical lifetime of a measurement (~ 10 min)

On-the-fly data reduction: Data Reduction Pipeline starts in first detector layer with “intelligence” = ASIC

SLAC long-term X-ray detector development plan

Bigger, Faster, Higher resolution and Higher Energies

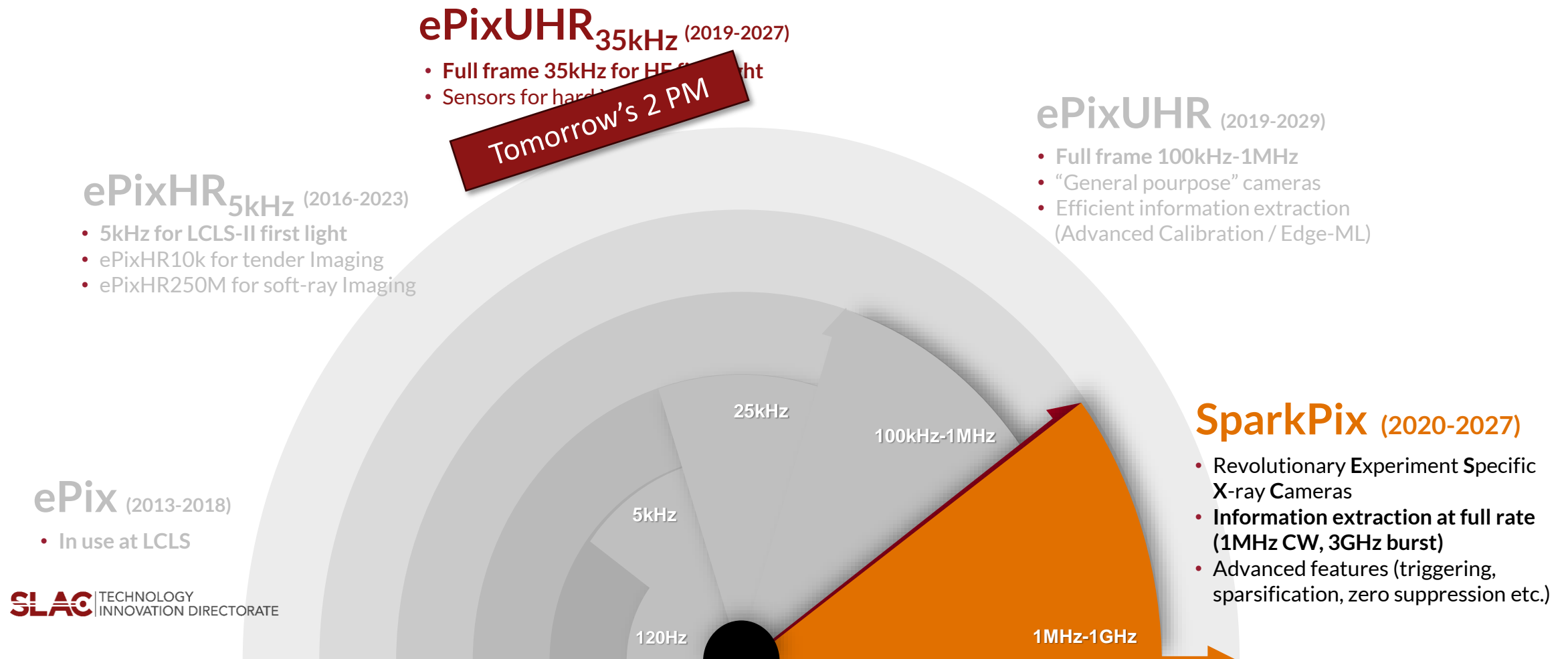
With goals built into projects progressively meeting science priorities and requirements



SLAC long-term X-ray detector development plan

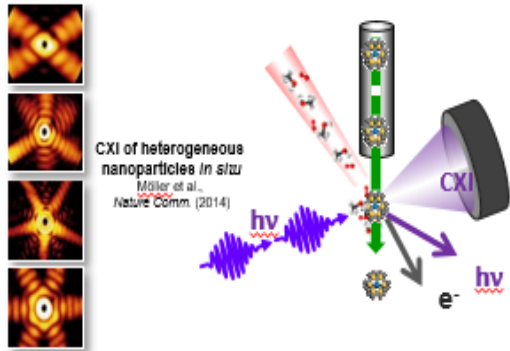
Bigger, Faster, Higher resolution and Higher Energies

With goals built into projects progressively meeting science priorities and requirements



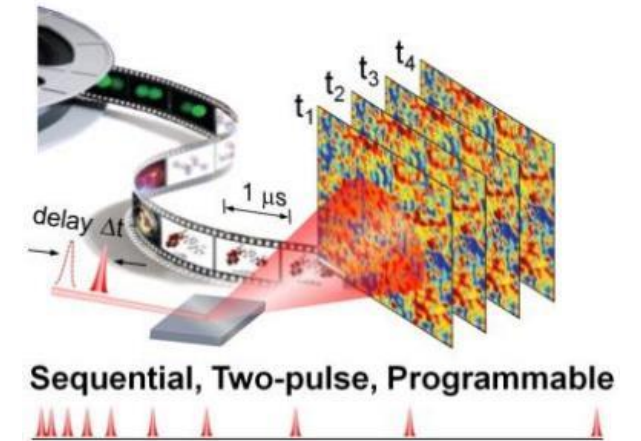
The science case for detectors: high-rate and versatility

Require full frame 100 kHz detectors



Imaging non-identical objects
e.g. Heterogeneity of functioning nano-catalysts

Require 1 MHz detectors Sparse Data

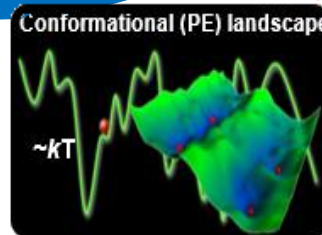
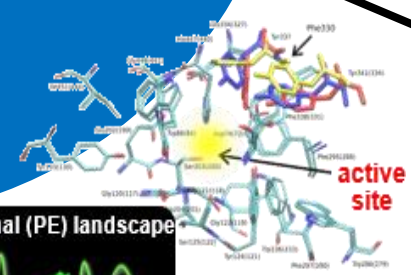


Stochastic Dynamics
e.g. Glass transition, charge fluctuations in quantum materials

“Rare Events”
e.g. Dynamic function of enzymes

XPCS, XSVS

Require 1 MHz detectors
Event Driven



SparkPix family

Four different pixel detectors in SparkPix family (currently):

	Front-end	Information extraction	Frame-rate
SparkPix-ED	energy	triggering	1 MHz / 100 kHz CW
SparkPix-RT	energy	data compression	100 kHz
SparkPix-S	energy	sparse readout	1 MHz
SparkPix-T	timing	sparse readout	1 MHz



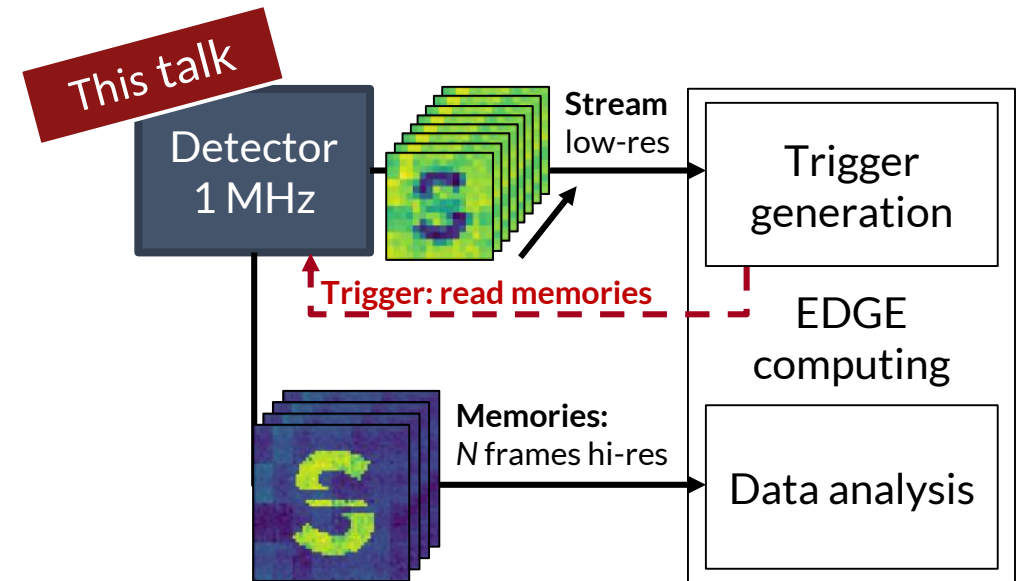
SparkPix-ED

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SparkPix-ED: science driver & concept

Rare events in X-ray scattering experiments

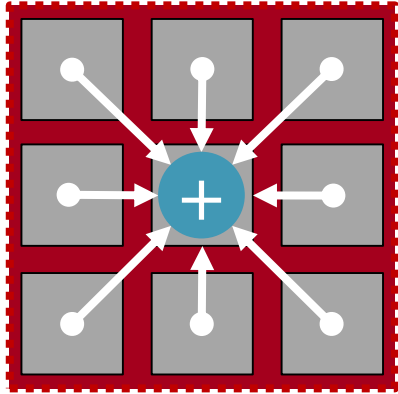
- **Science case:** capture interesting events happening at random, stochastic times that make their observation difficult
- **Requirements:** record N high-resolution images at closely spaced times around the rare event



Operation:

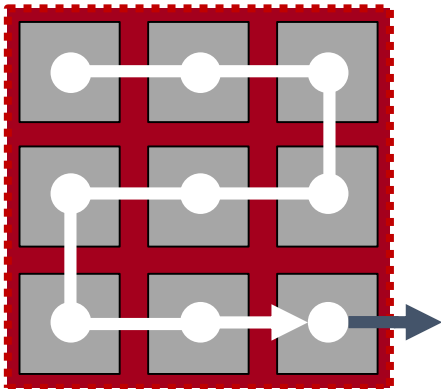
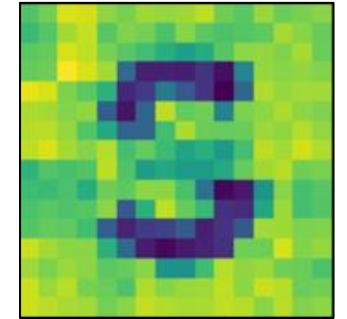
1. Low-resolution images are continuously sent to the EDGE computing layer @ 1 MHz
Meanwhile, N images are continuously recorded & stored in the detector in a ring-buffer
2. EDGE computing layer continuously analyzes data for rare events, then generated a trigger
3. The trigger starts the readout of the high-res N images recorded around the event of interest

MHz mode



Fast read-out to triggering layer: 1 MHz stream

- Sum signal of 9 pixels, resulting in a SuperPixel (SP) of $300 \times 300 \mu\text{m}^2$
- Sum operation reduces SNR by $\sqrt{9}$

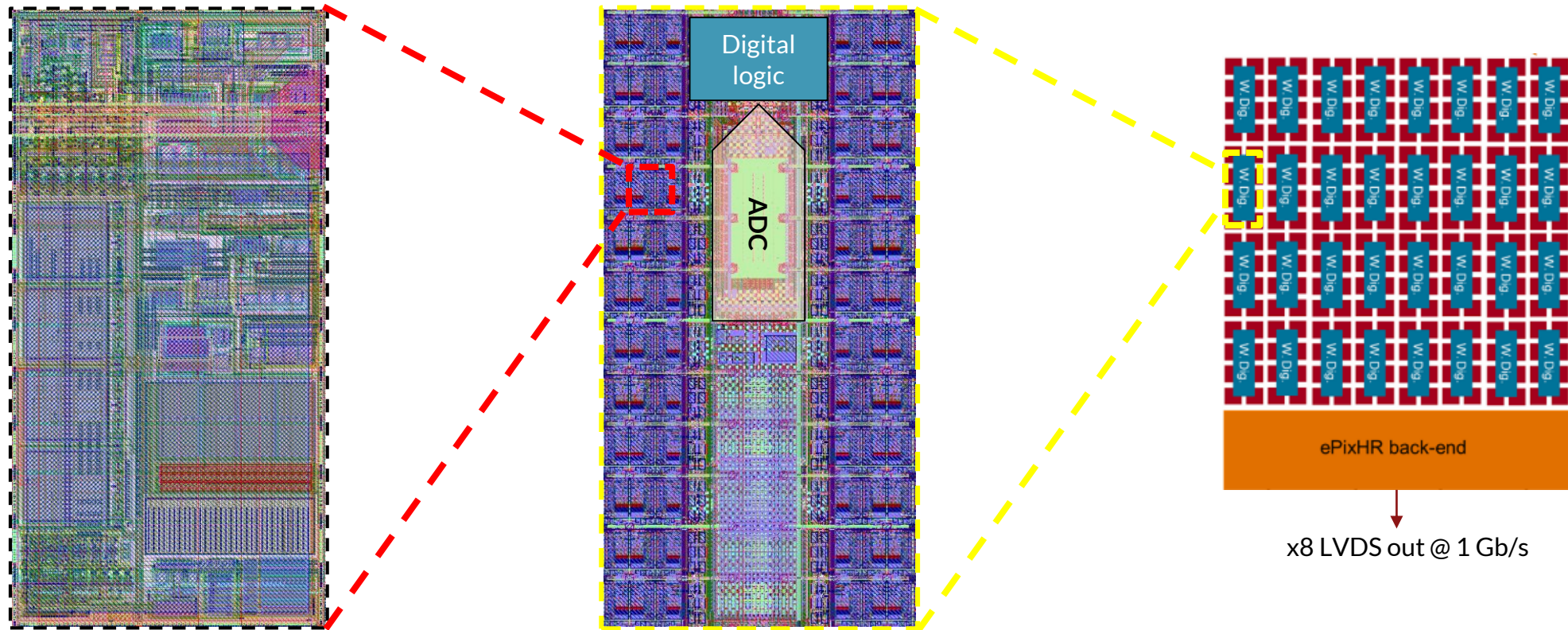


High-resolution read-out

- The ring-buffers in each pixel are read-out
- Read-out rate: $1 \text{ MHz} / (N * 9)$
- Read-out rate in 1st prototype: 25 kHz ($N=4$)
- Can be run in “CW imager” mode: 100 kHz



SparkPix-ED: overall architecture



Pixel

- Operates at 35 kHz -100 kHz
- Si sensor: 100x100 μm^2
- ASIC: 50x100 μm^2

Cluster

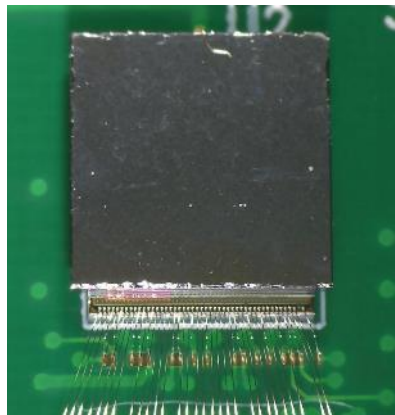
- 72 pixels \rightarrow 1 ADC @ 8 MSPS, 12b
- Digital logic for pixel configuration and readout

ASIC: 5x6 mm

Balcony includes:

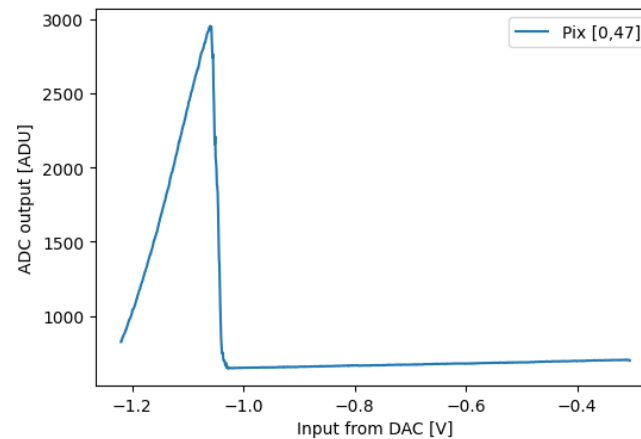
- Analog biasing
- Digital read-out logic
- Slow control/configuration

SparkPix-ED: overview of results from 1st prototype

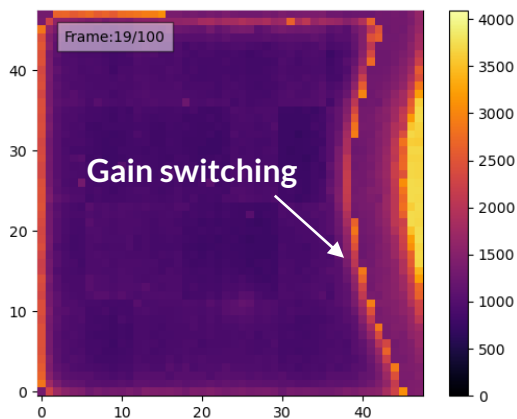
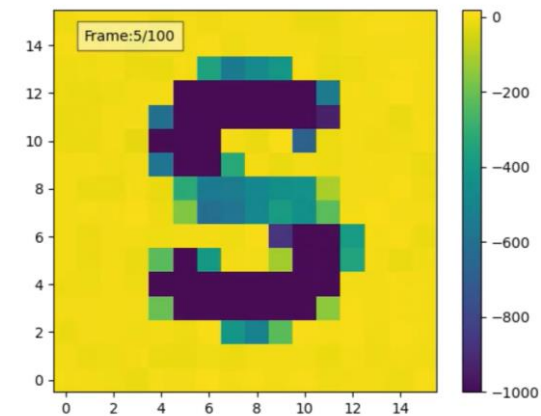


SparkPix-ED ASIC with 48x48 prototype Si sensor

Pixel response with charge injection

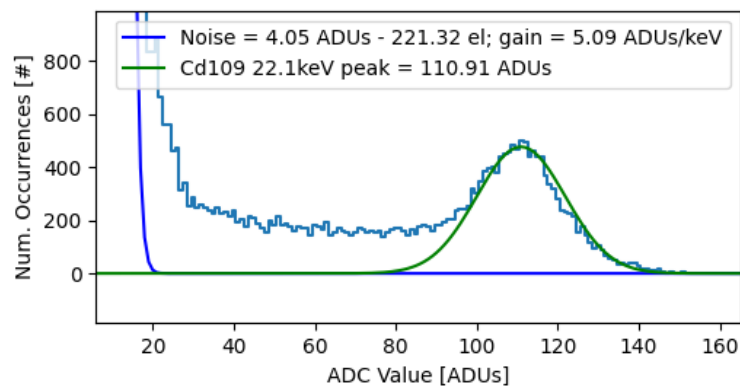


Sum: 1 MHz

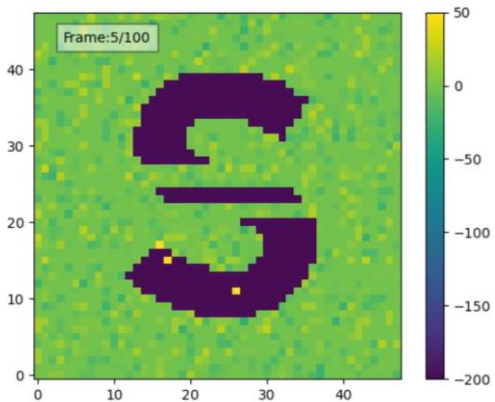


Illuminated with red laser from right side

Spectrum of Cd109 source (not calibrated, raw data).

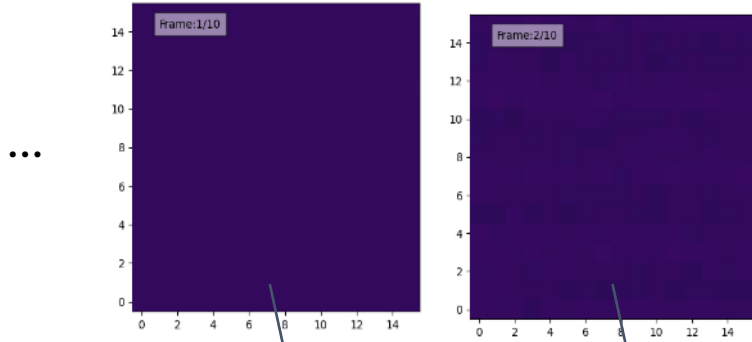


Hi-res: 0.1 MHz

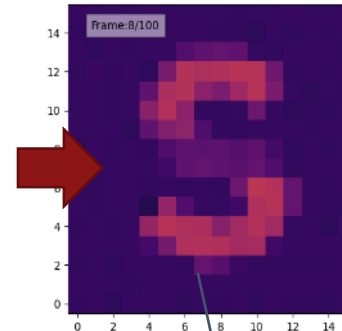


SparkPix-ED: fast trigger mode

ASIC



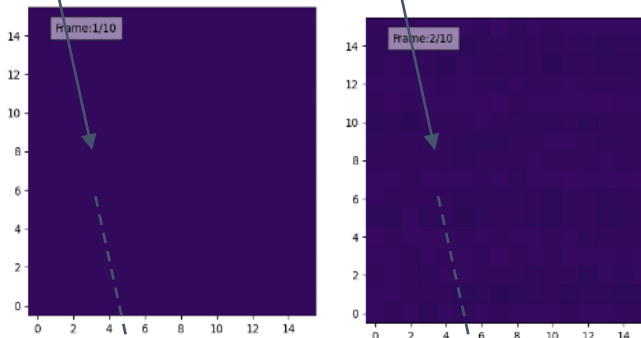
...
Inject at
frame 8



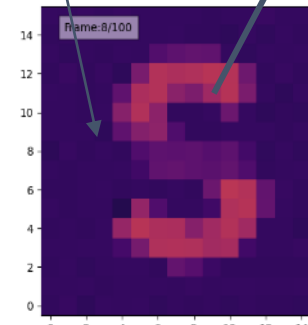
Switch to
memories
readout

FPGA

Trigger
condition:
>20 pixels in
low-gain

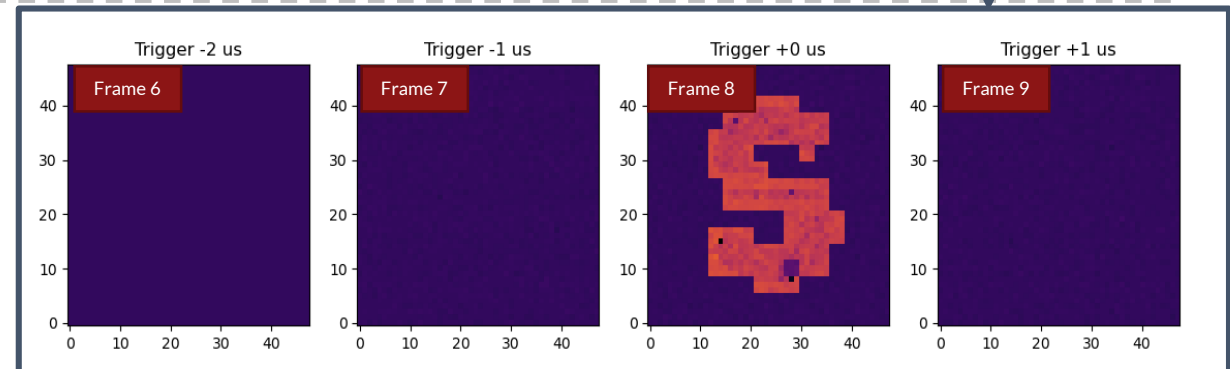


Triggered on
frame 8



DAQ

Fast images not stored
(data reduction)



SparkPix-RT

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SparkPix-RT: motivation

Next-gen photon science sources are facing a data deluge problem

LCLS-II: MHz readout with on-line data reduction

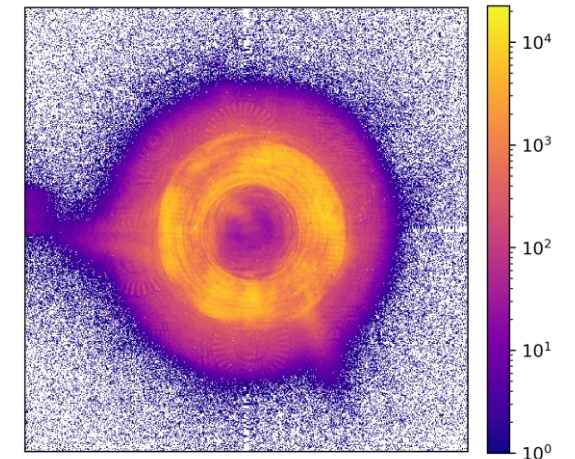
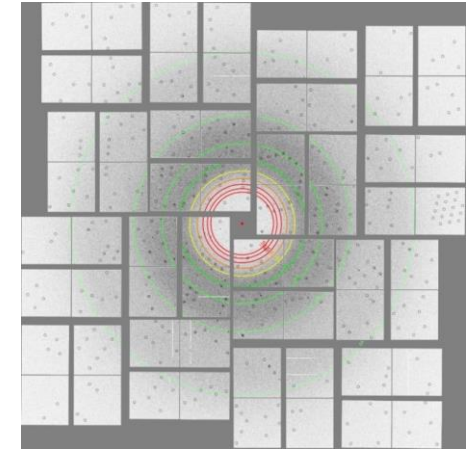
APS-U: Increases in brightness motivate the development of high-speed scanning microscopy instruments with rates approaching 1 MHz

Collaboration between Argonne & SLAC detector groups:

- SLAC is developing ePixUHR & SparkPix family: front-end, FPGA, etc...
- ANL studying techniques for data compression on-ASIC

Technical scope of SparkPix-RT project:

- Evaluate real-time compression in algorithms, in-ASIC
- Leverages modularity: front-end circuitry of ePixUHR/SparkPix-ED



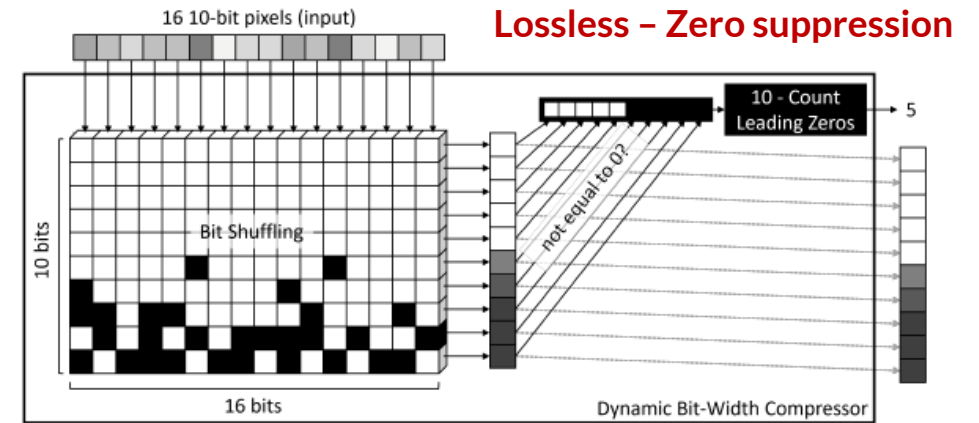
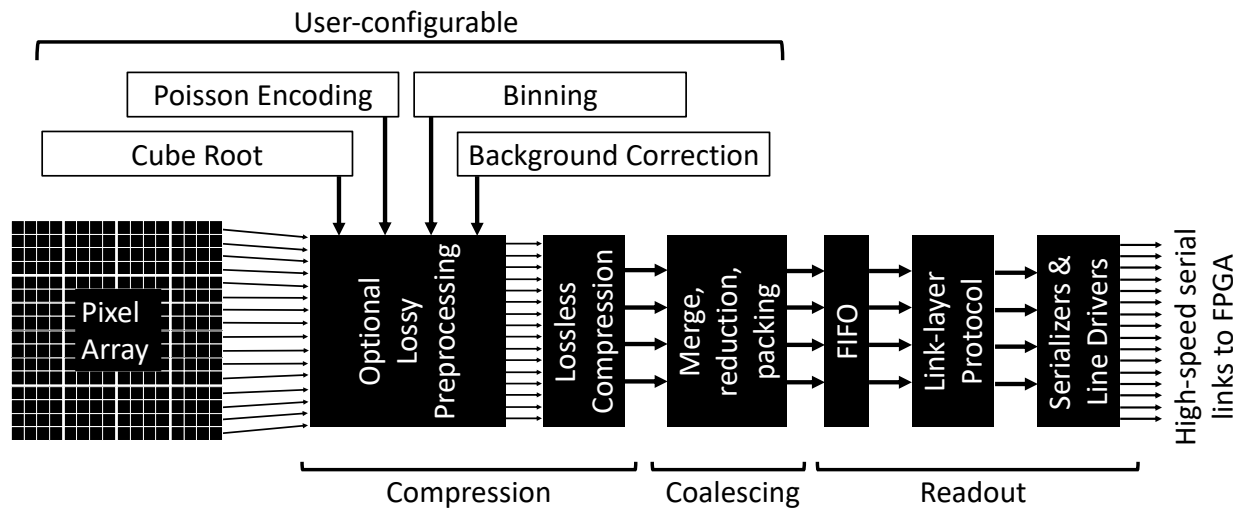
Examples of techniques that will benefit from MHz rate detector.

Top: diffraction pattern at LCLS

Bottom: ptychography image at APS

Compression algorithms

Initial Work – Compression performance on photon counting detector data



Pre-processing of data depends on the type of detector

- Photon counting: information is already quantized at pixel level
- Charge integrating: pre-processing is needed before compression → pedestal correction, thresholding, gain correction

We are exploring techniques for on-ASIC, real-time data calibration

Compression algorithms

Initial Work – Compression performance on photon counting detector data

Dataset Name	Lossless	Lossy	PNG	JP2 lossless	JP2 lossy q=90
	dynamic bitwidth	+ Poisson			
CNM APS HXN #1 [21]	9.98	13.62	8.45	12.98	20.31
CNM APS HXN #2 [21]	3.27	5.66	2.56	3.42	6.68
MAX IV NanoMAX [22]	5.26	7.74	4.16	5.18	19.22
NSLS-II HXN [23]	6.08	9.89	5.03	7.00	18.92
APS Velociprobe [24]	21.16	24.02	31.66	54.55	792.35

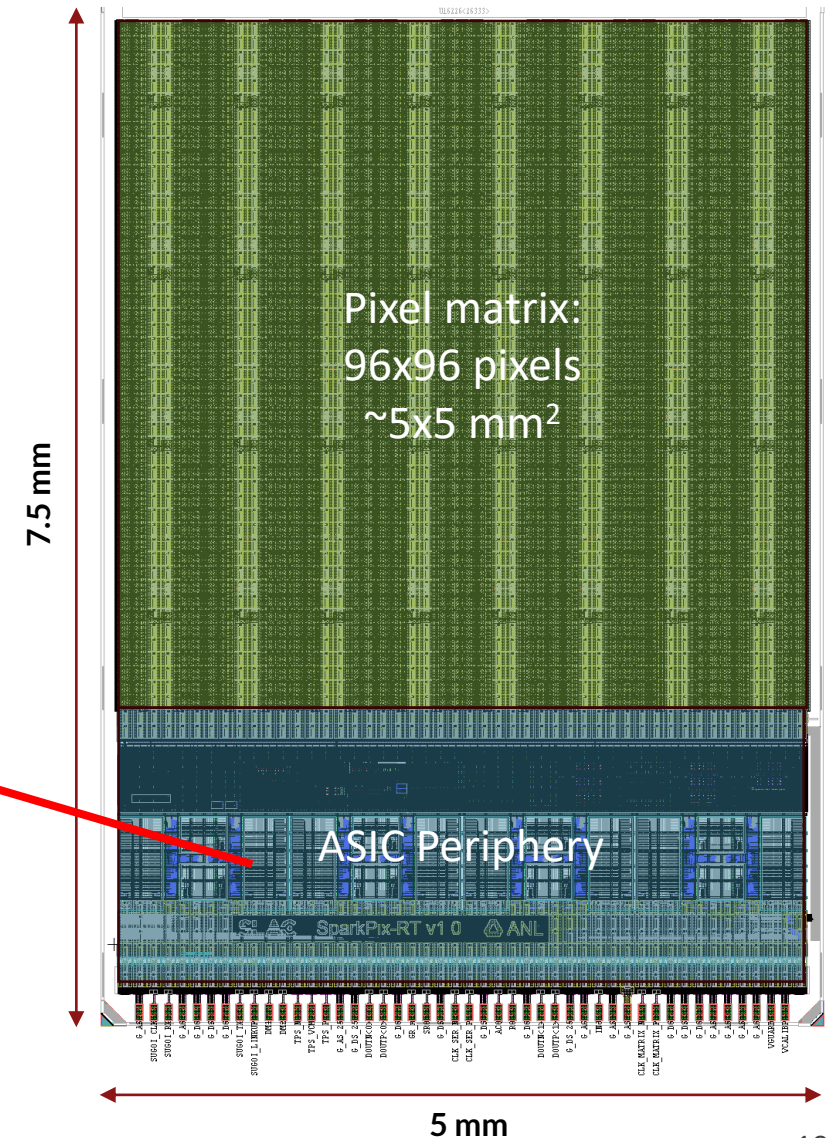
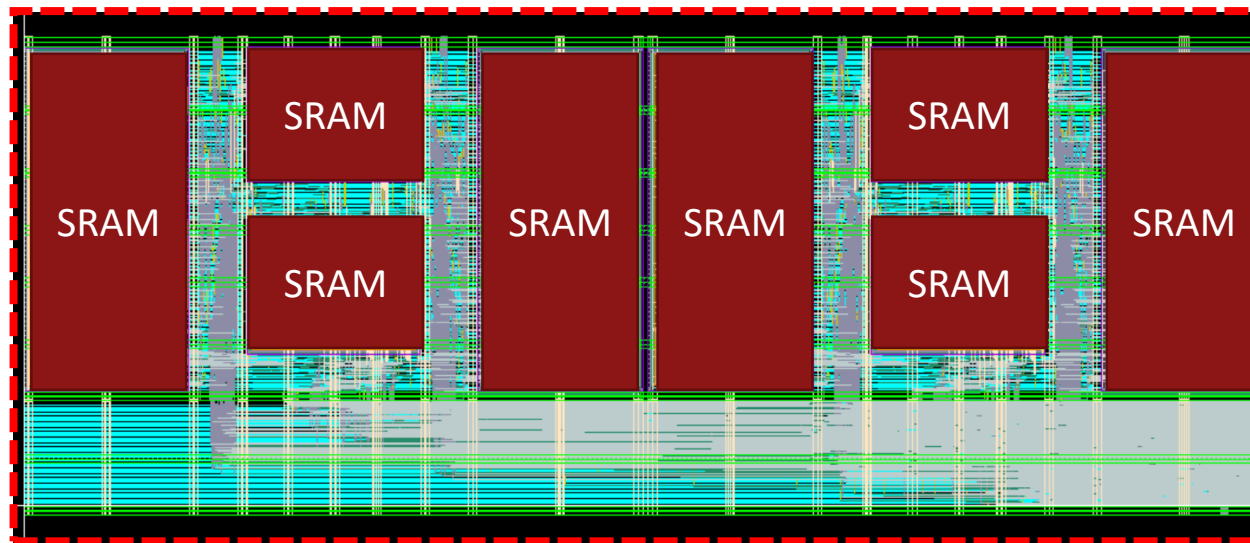
Table 1: Table of compression ratios with a selection of preprocessing methods and datasets.

- On photon counting detector data: lossless compression performs like more complicated compression methods such as PNG and JP2
- **Co-design is key:**
 - Performance of compression algorithms is evaluated on existing data from APS & LCLS
 - ... but also needs to adapt to the new ASIC front-end architecture

SparkPix-RT: status and next steps

- Digital logic implemented in periphery of ASIC
- 1st prototype (MPW) is now in-fab, expected delivery in Aug 2023
- Working towards a 100kHz, full-scale ($\sim 2 \times 2 \text{ cm}^2$) demonstrator

Layout of (half) compressor digital logic

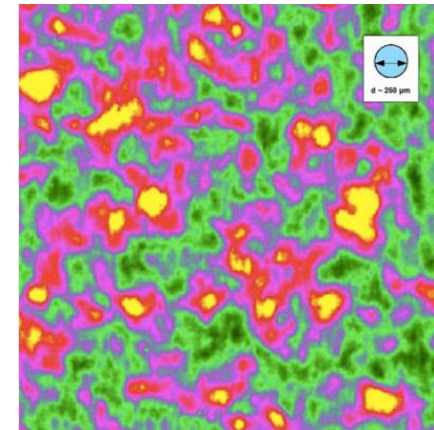


SparkPix-S

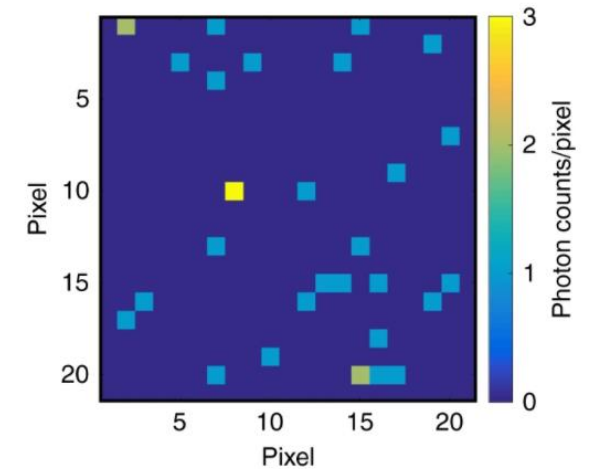
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SparkPix-S: science driver and detector needs

- X-ray Photon Correlation Spectroscopy (XPCS) and Speckle Visibility Spectroscopy (XSVS) will open new areas of science at LCLS-II:
 - Study spontaneous fluctuations at the atomic scale from microseconds down to the femtosecond timescale
 - Access stochastic fluctuations of matter on ultrafast timescales
- XPCS and XSVS experiments will benefit from a 2D integrating detector with:
 - Fine spatial resolution
 - Operating at 1 MHz, the max rate of LCLS-II
 - Discriminating between 0, 1, 2, 3... photons/pixel/frame
 - On-line data reduction through sparsified readout



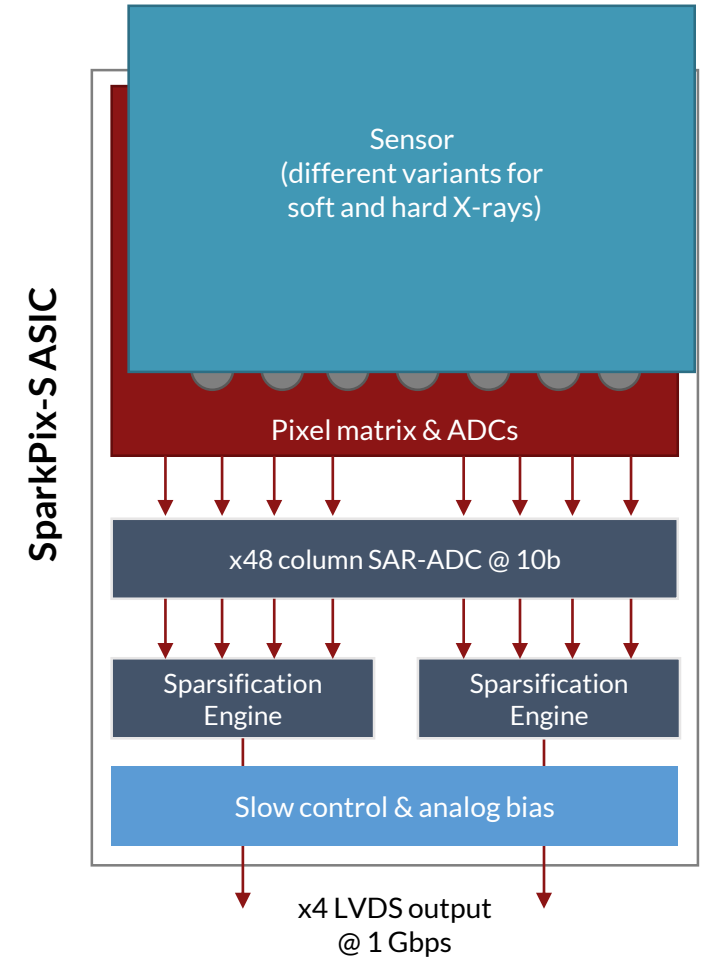
XPCS speckle pattern



Signal of photon events in a small region in a speckle pattern [1]

SparkPix-S: overview

- Goal is to meet the main requirements of XPCS/XSVS experiments in a single camera solution:
 - High-spatial resolution: 50um pixel pitch
 - High frame-rate: 1 MHz
 - Low-noise performance: $<60 e^-$ E.N.C.
 - Final camera size: 0.5 – 2 Mpix
- Designed to be **compatible with different sensors**:
 - 4 - 12 keV → Si sensor
 - 0.25 - 2 keV → future phase of the project (LGADs, MAPS)
- Moved away from “cluster” approach due to several reasons:
 - sparse readout, small pixel pitch (area, IR drop, routing)
- Column-parallel ADCs in periphery (adapted from ePixUHR)
- Sparsification digital engine from SparkPix-T (adapted)



Block diagram of SparkPix-S prototype (small scale)

SparkPix-S: pixel overview

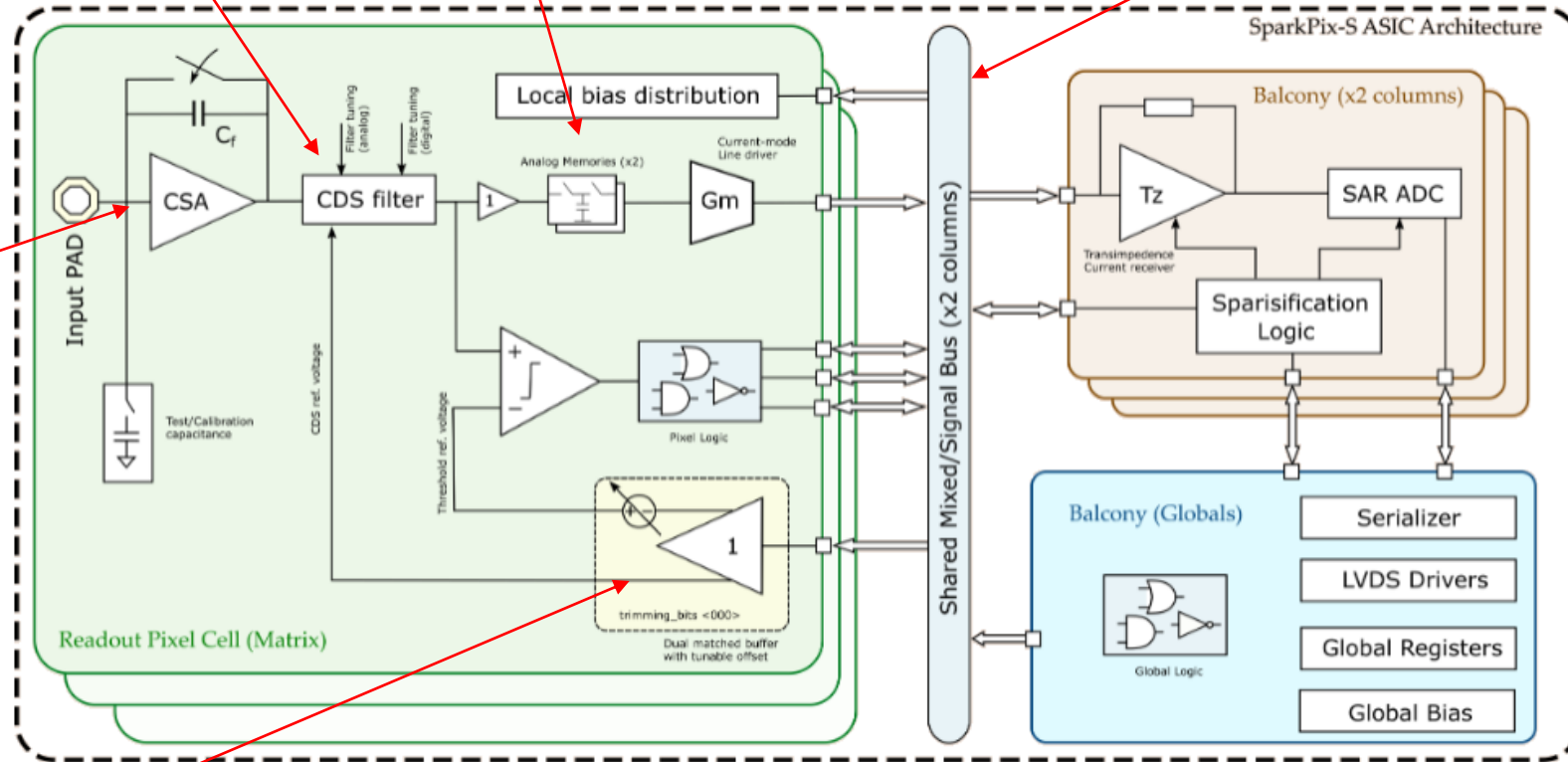
See F. Mele poster

Filter is programmable: trade frame-rate for better noise performance.

Integration and readout are pipelined using 2 analog memories.

Each pixel negotiates access to a bus shared every two columns.

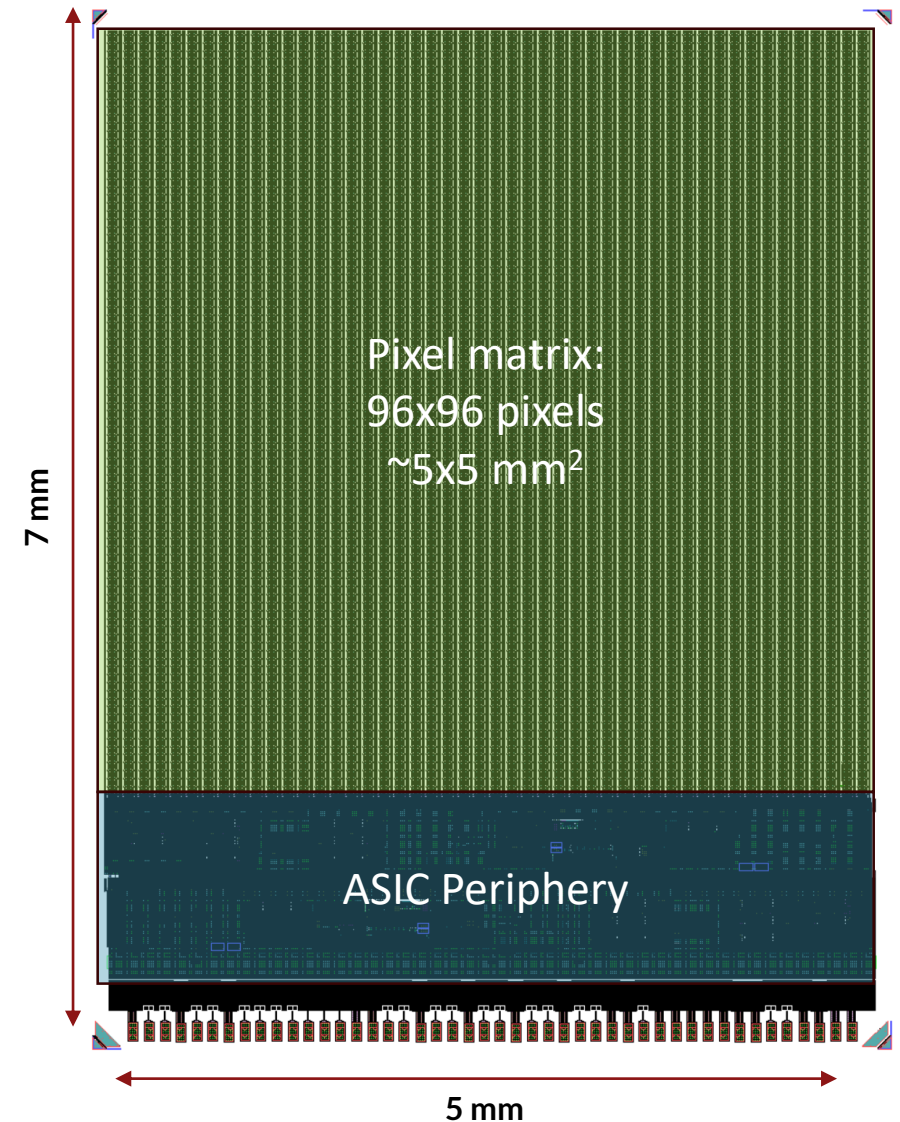
Fixed gain, dual supply, synchronous reset CSA.



Threshold generation strategy based on a matched buffers with tunable offset + auto-zeroed comparator.

SparkPix-S: status and next steps

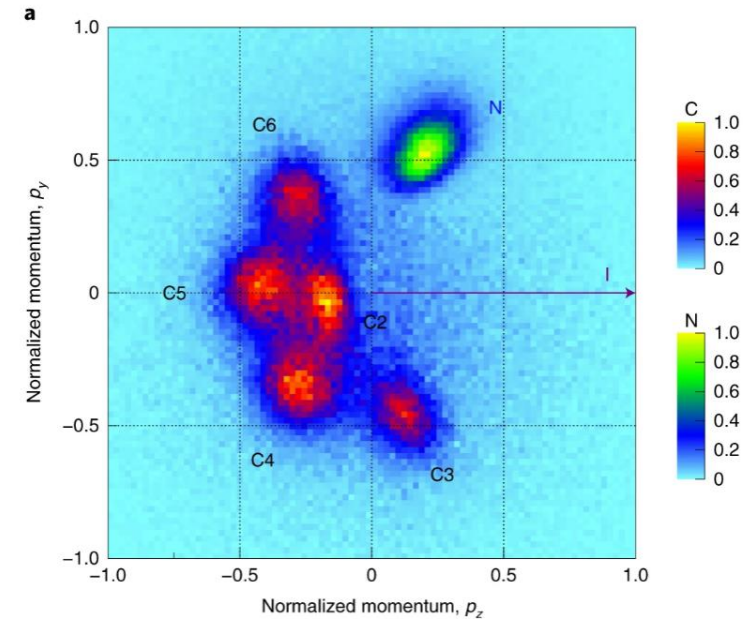
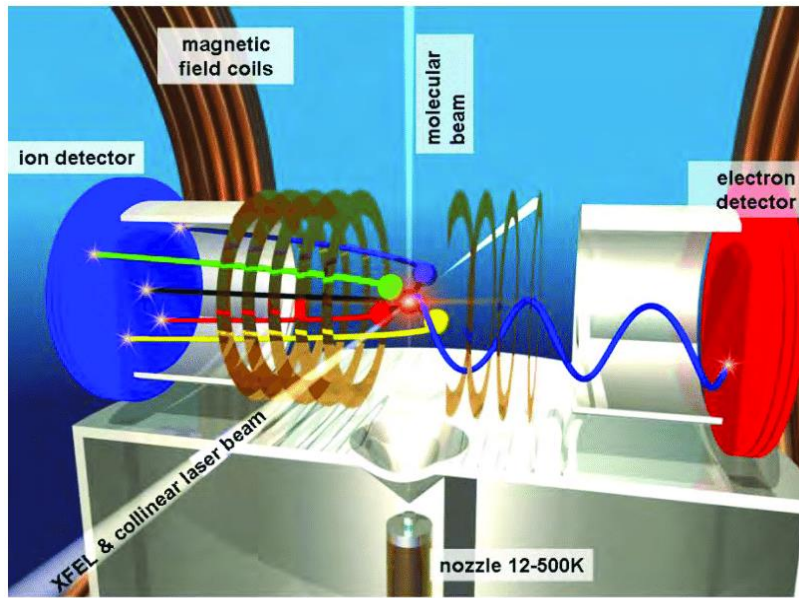
- **Simulated performance of first prototype:**
 - Noise: 50-55 e^-
 - Dynamic range: 50keV
 - Power consumption: 18 μ W/pixel @ 50 μ m pitch
- **Status:**
 - First MPW has been designed between July 2022 – May 2023
 - Chip delivery in August 2023
- **Towards full-scale design:**
 - 40 Gb/s output throughput needed to meet the 1% occupancy spec @ 1 MHz
 - Design of on-ASIC transceivers is being finalized
 - Prototype camera development has started
- Tape-out of first full-scale ASIC planned for mid 2024



SparkPix-T

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DREAM reaction microscope at TMO



- Measure 3D momentum of ions & low-energy e^- : access nuclear structure
- Time resolution requirement: **250 ps**
- Currently done with MCP delay-line detectors, but:
 - 10s - 100s electrons/shot: ok for 120 Hz, problematic at high **rep-rate**
 - **MCP degradation** in hours above $\sim 10^6$ counts/s
 - Challenging to identify individual electron peaks without additional dimension: **degradation in resolution**
 - Delay line detector records time-of-arrival and position on detector of ionic fragments in coincidence
 - Delay line detector unable to **disambiguate** ~ 8 ionic fragments, as required for studies of complex systems

SparkPix-T: timeline and requirements

- **Tixel** - origin: LDRD - prototype ASIC fabricated and tested, demonstrated timing 2014-2016
- **SparkPix-T v0.1** prototype (48x48 pixels), additional features added 2019-2021
- **SparkPix-T v0.2** prototype (48x48 pixels), fixed bugs 2021-2022
- **SparkPix-T v1.0**: full-size ASIC fabricated, testing in progress 2022-2023

	SparkPix-T Specifications
Mode of Operation	Time of Arrival (+ ToT)
Timing resolution	100ps
Time depth	6.5 μ s (16bit)
TOT	8bit
Technology	0.13 μ m
Pixel size	100x100 μ m ²
Array	176x192 (48x48 prototype)
Frame rate (Occupancy)	5kHz (100%), 100kHz (5%), 1MHz (0.5%)
Range	10keV-100keV (0.44fC- 4.4fC)
Max Hit rate / area	49Mhit/s/cm ²
Gating	min 20ns

Additional features requested:

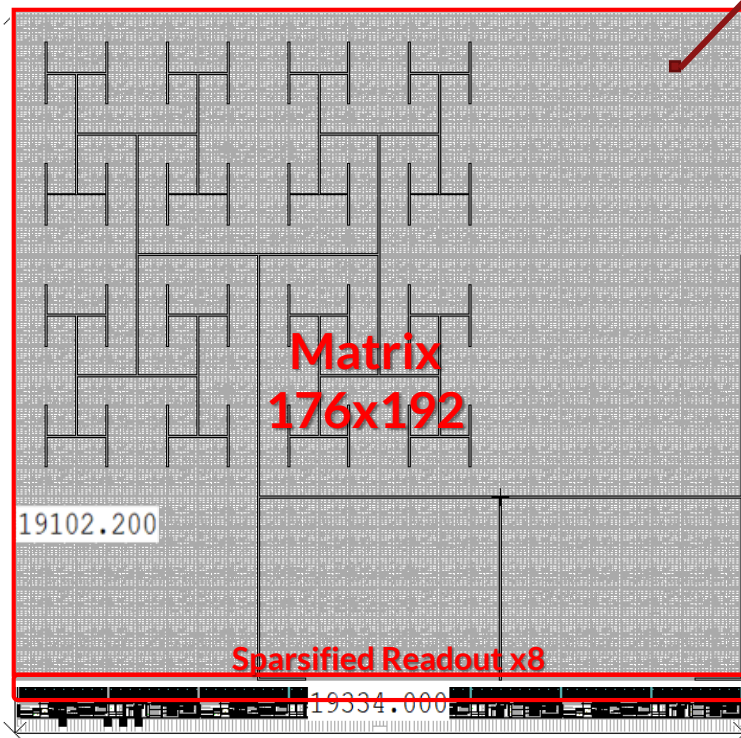
- **Gating of the preamp** in pixel to reject “background” photons
 - LCLS pulse creates “background” photons at t=0 (florescence due to LCLS pulse, scattered X-ray photons, stray light in the range of 0.3-2 keV)
 - Deadtime caused by “background” photons can lead to signal loss in the time interval of interest
- **Sparsified readout**: two ways to handle over-occupancy:
 - Flush data → typical, data over-occupancy are lost
 - Paralyze system → prevent new acquisitions until all the data are readout
 - If specs are exceeded, users notified **in real-time**

SparkPix-T: architecture

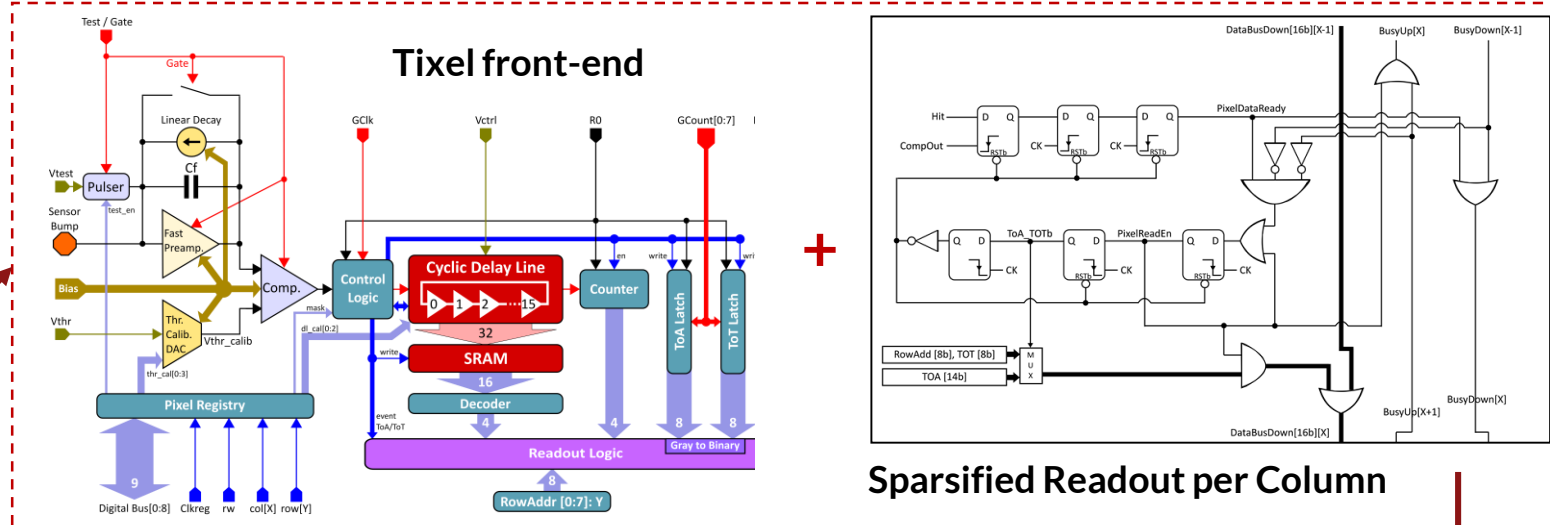
Prototype SparkPix-T:



Full-size SparkPix-T:

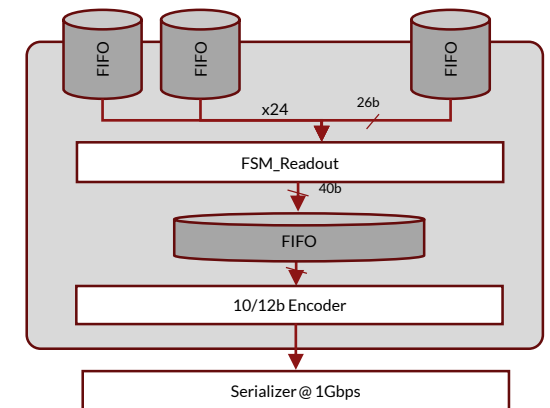
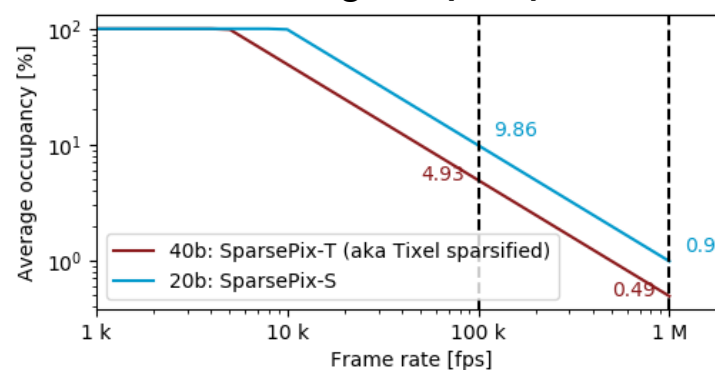


Pixel (100x100um²)



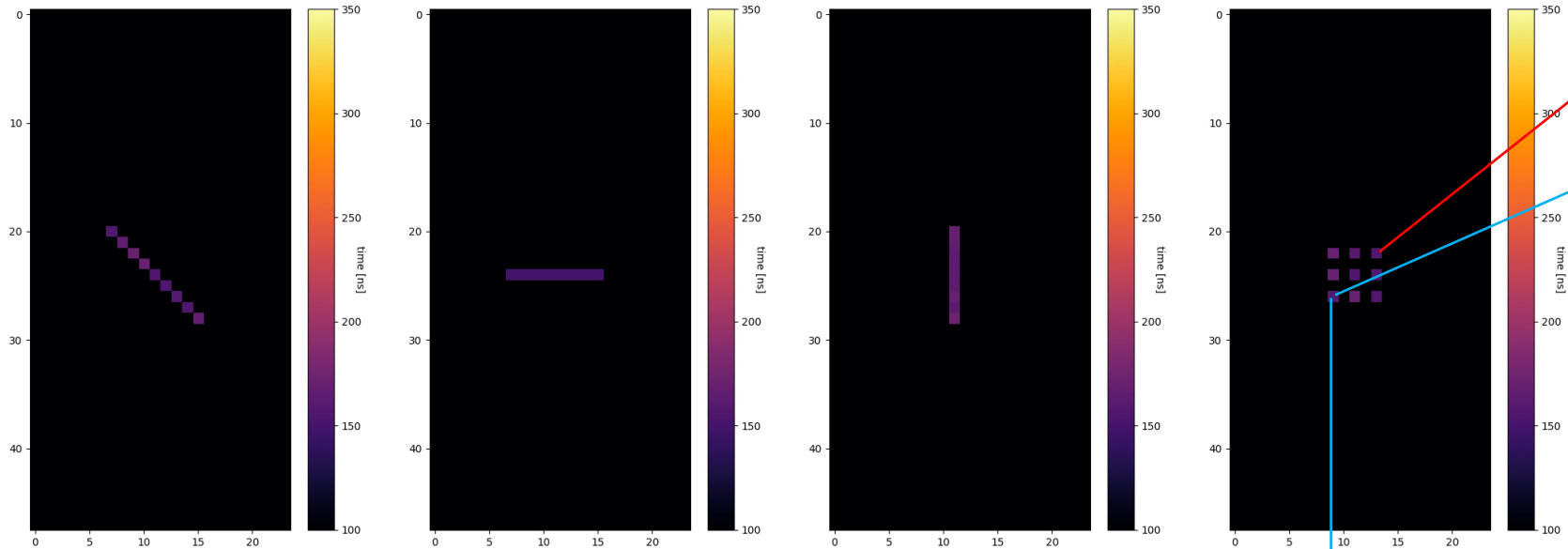
Sparse digital readout (every 24 columns): can be tailored to different ASICs

Simulated avg occupancy/frame



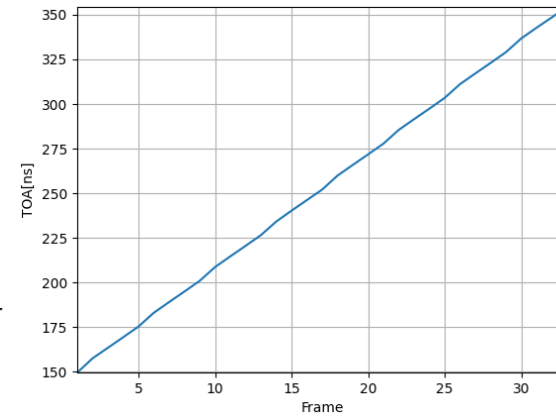
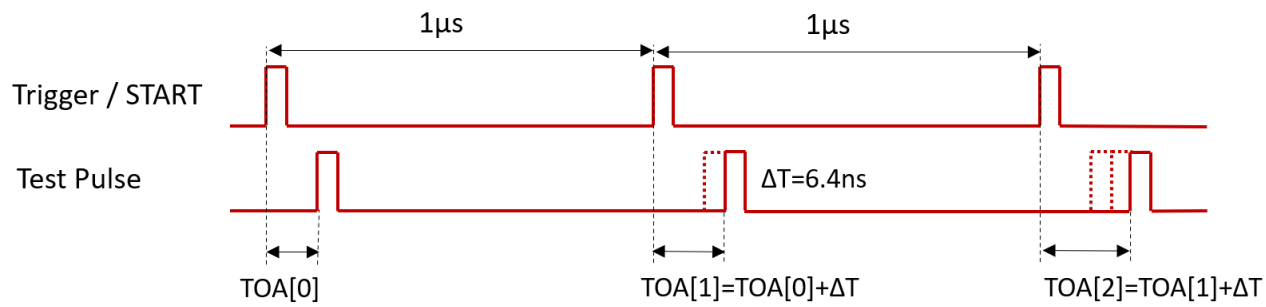
SparkPix-T: sparsified readout

- Readout at **1MHz** frame rate:

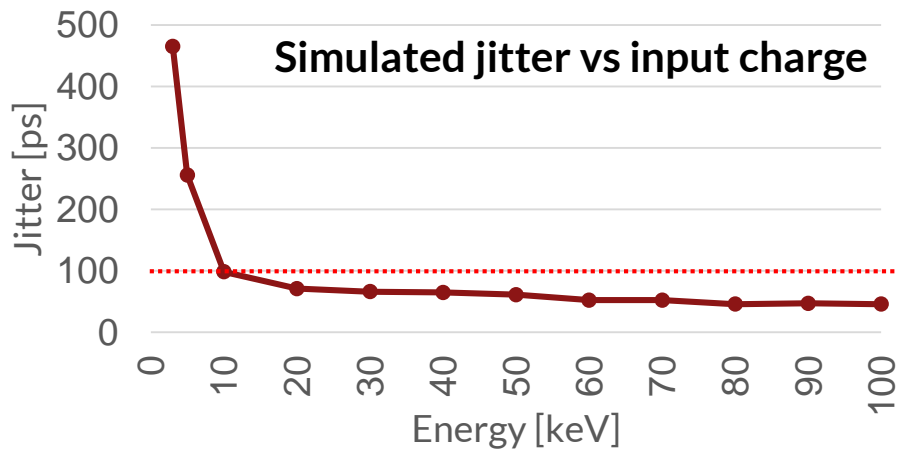
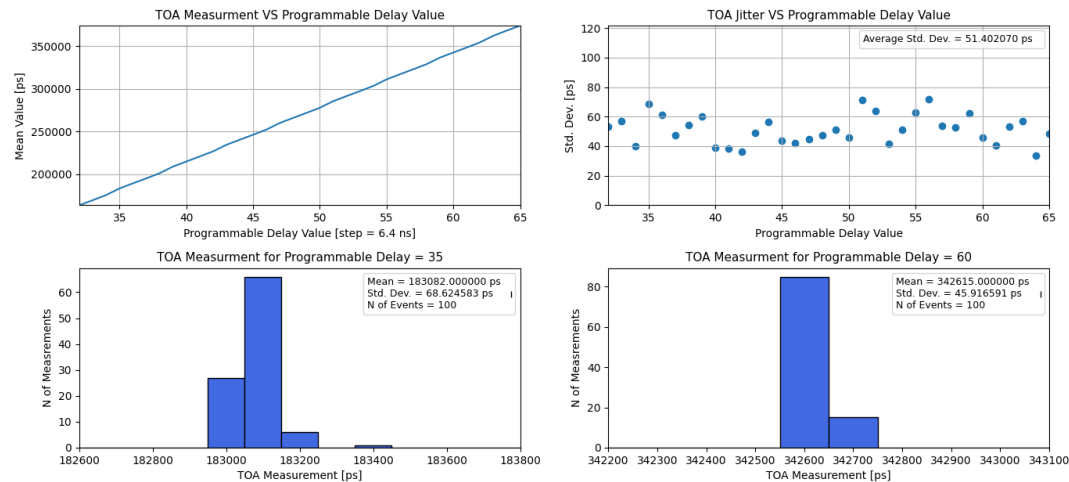


- Sparsified data stream:

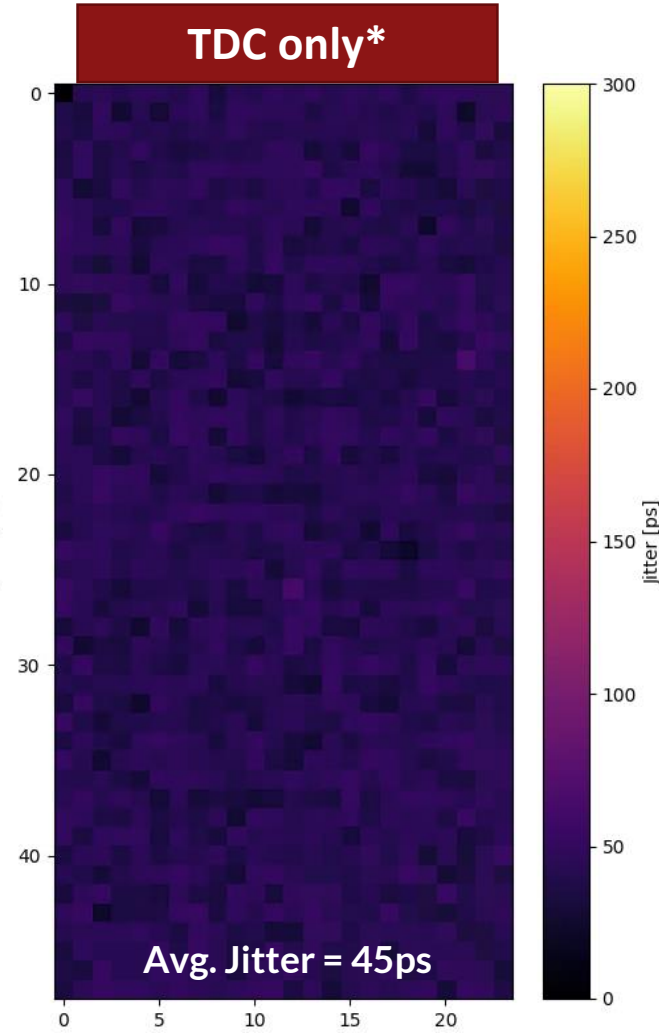
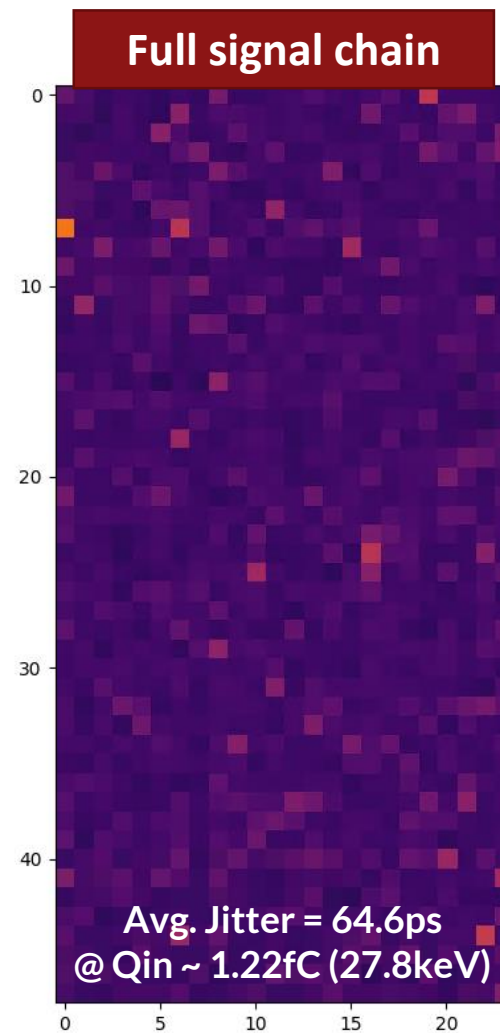
trig=0	col=11	row=22	TOT=15	ToA_C=7	ToA_F=97
trig=0	col=13	row=22	TOT=15	ToA_C=7	ToA_F=97
trig=0	col=9	row=24	TOT=15	ToA_C=7	ToA_F=97
trig=0	col=11	row=24	TOT=15	ToA_C=7	ToA_F=98
trig=0	col=13	row=24	TOT=15	ToA_C=7	ToA_F=96
trig=0	col=13	row=26	TOT=15	ToA_C=7	ToA_F=99
trig=0	col=9	row=26	TOT=15	ToA_C=7	ToA_F=99
trig=0	col=11	row=26	TOT=15	ToA_C=7	ToA_F=99
trig=1	col=13	row=22	TOT=15	ToA_C=7	ToA_F=157
trig=1	col=9	row=22	TOT=15	ToA_C=7	ToA_F=158
trig=1	col=11	row=22	TOT=15	ToA_C=7	ToA_F=156
trig=1	col=11	row=24	TOT=15	ToA_C=7	ToA_F=157
trig=1	col=13	row=24	TOT=15	ToA_C=7	ToA_F=156
trig=1	col=9	row=24	TOT=15	ToA_C=7	ToA_F=156
trig=1	col=9	row=26	TOT=15	ToA_C=7	ToA_F=157
trig=1	col=11	row=26	TOT=15	ToA_C=7	ToA_F=158
trig=1	col=13	row=26	TOT=15	ToA_C=7	ToA_F=158
trig=2	col=9	row=22	TOT=15	ToA_C=7	ToA_F=220
trig=2	col=11	row=22	TOT=15	ToA_C=7	ToA_F=218
trig=2	col=13	row=22	TOT=15	ToA_C=7	ToA_F=218
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trig=3	col=13	row=22	TOT=16	ToA_C=8	ToA_F=37
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trig=3	col=9	row=26	TOT=16	ToA_C=8	ToA_F=39
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trig=4	col=13	row=26	TOT=16	ToA_C=8	ToA_F=40
trig=4	col=9	row=22	TOT=16	ToA_C=8	ToA_F=100
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trig=4	col=13	row=22	TOT=16	ToA_C=8	ToA_F=98
trig=4	col=13	row=24	TOT=16	ToA_C=8	ToA_F=97
trig=4	col=9	row=24	TOT=16	ToA_C=8	ToA_F=97
trig=4	col=11	row=24	TOT=16	ToA_C=8	ToA_F=98
trig=4	col=13	row=24	TOT=16	ToA_C=8	ToA_F=99
trig=4	col=9	row=26	TOT=16	ToA_C=8	ToA_F=99
trig=4	col=11	row=26	TOT=16	ToA_C=8	ToA_F=100



SparkPix-T: timing performance



- **Measured:** jitter < 100ps for $Q_{in} > 10\text{keV}$



*includes jitter contributions from TDCs, reference clock jitter, test-pulse jitter, clock and test-pulse distribution trees.

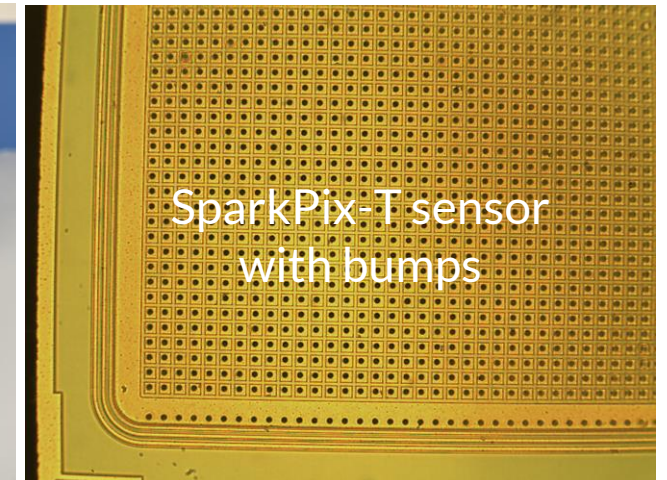
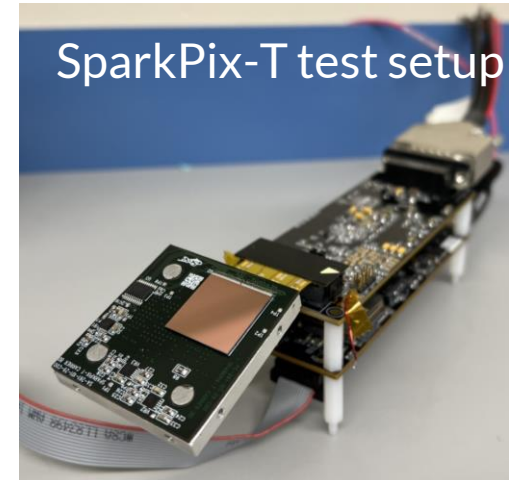
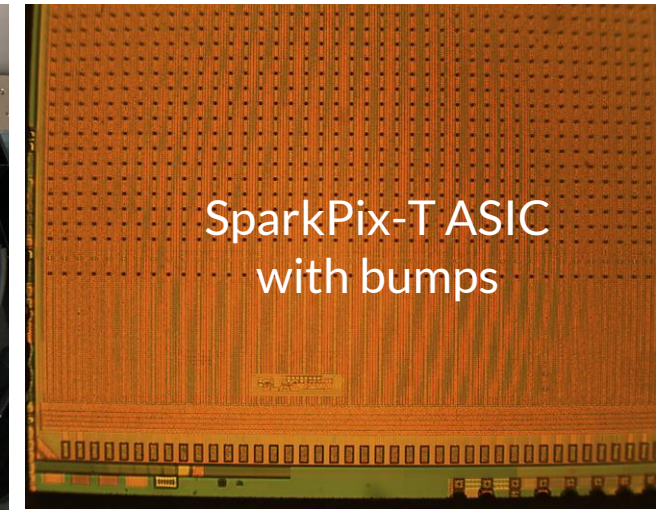
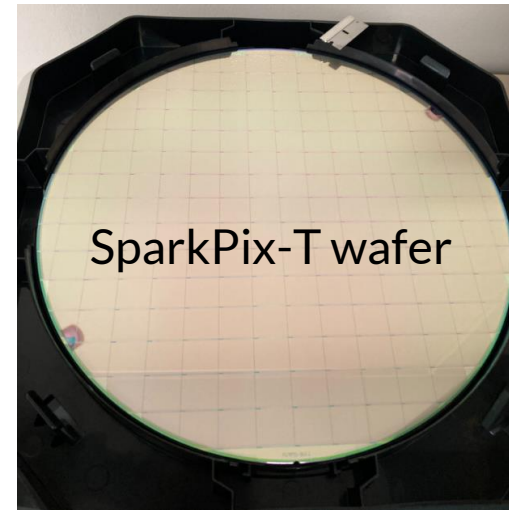
SparkPix-T: summary & next steps

Status:

- First full-reticle ASIC on CMOS 130 nm:
176x192 pixel array with sparsification engine and
8 Gb/s output bandwidth
- Wafers received
- Readout card and FPGA firmware/software ready
(C. Bakalis, D. Doering)
- Testing in progress

Next steps:

- Test-bench characterization of the full-size ASIC
- Camera prototype demonstration at TMO
- Upgrade I/Os to ~5Gbps/channel
- Follow-up project with LGADs for 0.5 Mpix camera



Summary

Summary

SLAC is developing a new family of ultra high-rate X-ray detectors to meet the science goals of LCLS-II / LCLS-II-HE

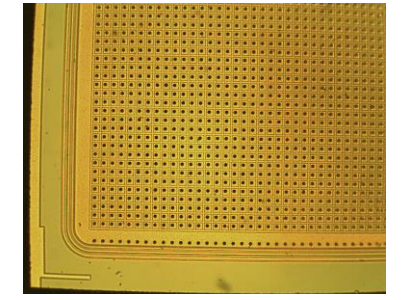
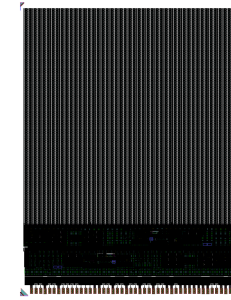
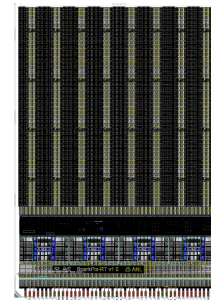
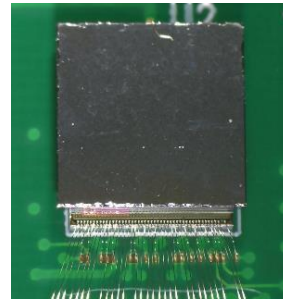
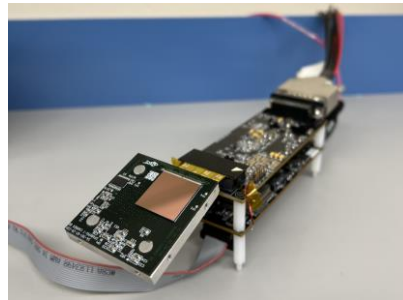
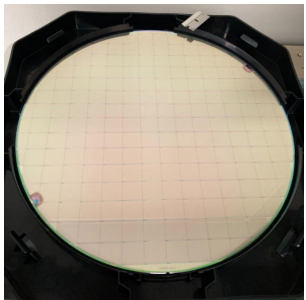
Full-frame detectors:

- **ePixUHR-35kHz:** first large-scale ASIC functional, characterization on-going
- **ePixUHR-100kHz:** upgrade clocking & increase output throughput, 1st prototype in 2024

Tomorrow

Detectors with on-ASIC information extraction:

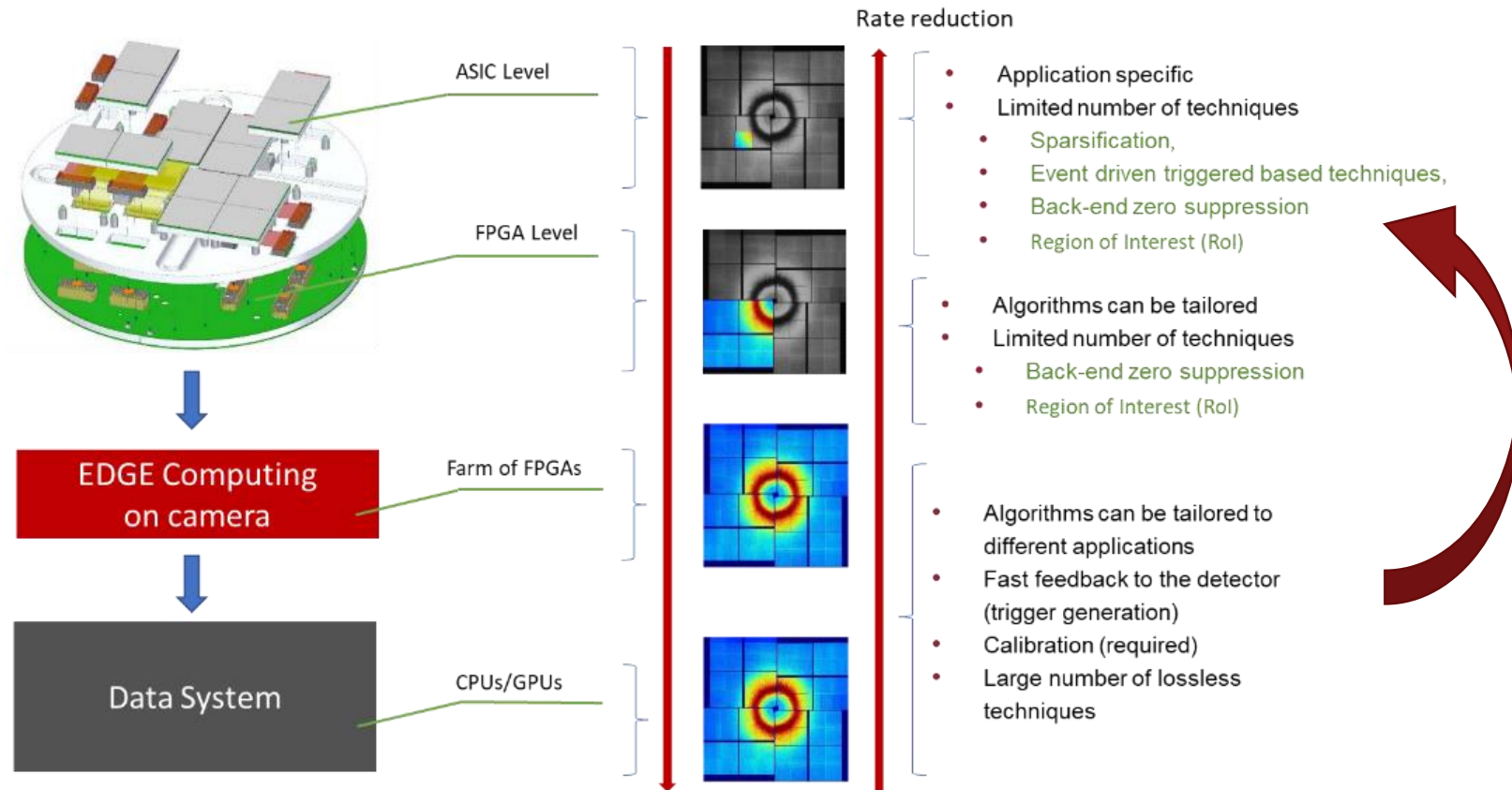
- **SparkPix-T:** 1st full-scale prototype is alive, characterization on-going, next: beam-time at TMO beamline
- **SparkPix-ED:** 1st prototype demonstrated low-latency feedback, re-assessing science specifications
- **SparkPix-RT:** 1st MPW in fab, currently scaling the design to full-scale for late 2023 submission
- **SparkPix-S:** 1st MPW in fab, characterization will start in fall, full-scale ASIC in mid-late 2024



Future research directions

What is the path forward?

- Distributed processing for efficiency (energy, information)
- Leverage AI/ML for real time data extraction with low latency (e.g., SNL library)
- Develop adaptive data driven readout architectures
- Develop supporting technology for high-bandwidth, on-detector communication
- Adopt beyond CMOS technologies with heterogenous integration



Push computing as close as possible to the source