Title : Survey of Techniques for Efficient Solving of Boolean Formulas from Formal Verification of Pipelined, Superscalar, and VLIW Microprocessors at a High Level of Abstraction

Authors : Miroslav N. Velev (Aries Design Automation, U.S.A.)
Speaker : Miroslav N. Velev

Abstract: In 2000 – 2003, the author made publicly available a collection of more than 1,100 Boolean formulas generated in formal verification of complex pipelined, superscalar, and VLIW microprocessors. These formulas galvanized the Boolean Satisfiability (SAT) community, and were used for the development of all recent academic and industrial SAT solvers. The paper evaluates the efficiency of various techniques for efficient solving of such formulas on the latest generation of workstations.