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A novel ANFIS-controlled customized UPQC device for power quality enhancement

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Abstract

Power quality is crucial for the reliable and efficient operation of domestic and industrial loads. Nonlinear power electronic converter loads have increased in usage, which has led to a decline in both voltage and current quality. To overcome these power quality issues, a universal power quality compensator (UPQC) has been developed and integrated into the power distribution network. The UPQC comprises dual active power filters which are equipped with a DC-link capacitor. The voltage of the DC-link capacitor is controlled by a DC-link voltage controller. However, the conventional PI controller is not suitable for regulating voltage at a defined level due to inappropriate gain values. In this work, we propose an intelligent adaptive neuro-fuzzy inference system-based DC voltage controller for customized UPQC devices. The proposed control scheme aims to mitigate the existing power quality challenges by reducing the issues in classical controllers and incorporating intelligence knowledge with subjective decisions. Using the MATLAB/Simulink software tool, we have tested a customized UPQC device controlled by ANFIS for critical operation and performance. The simulation results are presented along with valid comparisons.

Highlights

1. Developed Customized Power quality conditioner
2. Developed novel ANFIS Controller
3. Hybrid Ant Colony Optimization is used to mitigate power quality issues
4. UPQC is used to mitigate power quality issues
5. Different controllers have been used to mitigate the power quality issues

Keywords: Adaptive neuro-fuzzy inference system (ANFIS) controller, Customized UPQC device, Power quality improvement, Total harmonic distortions

Introduction

An electric power system (EPS) is arranged as an interconnected network consisting of various electrical sections deployed for generation, power transfer and distribution to end-level consumers. The distribution system is a most significant network for delivering reliable, stable, continuous, and quality power to meet required load demand. In the

current scenario, maintaining the power quality (PQ) in the distribution system is the key attention because of automated industrial and domestic loads, increased usage of nonlinear power electronic converter loads, arc furnaces, variable speed drives, etc. All these are the primary causes of PQ distortions and PQ deviations due to crucial implications affecting the end-level consumers and utility grid system [1].

The emergence of PQ impacts may cause critical issues affecting the supply voltage, current, and supply frequency from their significant specifications and damaging the other loads and the entire distribution network [2]. In fact, the main causes and sources of current distortions are unbalanced loads, harmonic distortions in supply current, drops in reactive power, non-unity supply power factor, and so on. In a similar way, the main causes and sources of voltage deviations are voltage harmonics, voltage swells, voltage flickers, and so on. The distortions and deviations in both current and voltage imply power pollution and may decrease the transfer of quality power to common coupling points or loads (PCC) connected at the distribution network [3].

The statistical reports on the quality nature of electrical power to end-level consumers in India are included with regard to the growth of PQ issues. In this regard, many power system engineers and researchers are being initiated to implement advanced customized power technology (CPT) for enhancing the power quality [4, 5]. In recent days, various CPT devices have been adopted to compensate for respective PQ problems resulting in the distribution network being maintained as fundamental, linear, sinusoidal, and balanced in nature. Some of the prominent CP devices are active power filter (APF) [6], distributed static compensator (DSTATCOM) [7], dynamic voltage restorer (DVR) [8], etc. Along with this, the customized unified power quality compensator (UPQC) [9] is the most significant PQ compensation device for resolving both voltage–current-allied PQ issues.

From several literature studies, the UPQC utilizes the dual active power filters for compensation of both voltage and current PQ issues which are explored in [10]. Brenna et al. [11], proposed the performance analysis of a novel OPEN-UPQC defined as a custom-UPQC model consisting of steady-state series and shunt devices without a DC-link interface which is installed in low–medium-voltage substation. Xu et al. [12] presented the single-phase UPQC device for enhancing the power quality in a high–medium-voltage distributed power system network using the modular matrix converter. Regardless of several custom compensation devices, the UPQC plays a significant role in the secondary distribution system for enhancing power quality features.

The customized UPQC utilizes multiple voltage source inverters (VSIs) which are constituted as series–parallel forms integrated by a common DC-link capacitor for PQ improvement in the distribution network. The proposed C-UPQC mitigates both supply-side and load-side PQ issues in the distribution power system network and also exchanges the reactive power to maintain voltage stability under standard operating conditions. The proposed C-UPQC requisites efficiently performed control algorithms for extracting the voltage and current reference signals by using voltage and current sensors. In general, the synchronous reference frame (SRF) control algorithm [13] has been employed for the extraction of a reference voltage signal to series VSI of the C-UPQC device, and the instantaneous real-reactive power (IRP) control algorithm [14] has been employed for the extraction of reference current signal to shunt VSI of C-UPQC device [15].

The absolute performance of the C-UPQC device relies on the DC-link voltage of the DC capacitor which is controlled by the DC-link voltage controller and maintains PCC voltage as constant. This control scheme utilizes the proportional-integral (PI) controller which is not suitable for voltage regulation at defined voltage levels due to inappropriate gain values. At present, the modern artificial intelligence control algorithm evidences the intelligence knowledge base through various possible interpretations like, "machines over the human-knowledge" [16–23]. In [24], authors describe performance and security enhancement using an OUPF controller under different conditions. In [25], the improvement of power factor using DSTATCOM with a switchable capacitor bank is discussed. [26] discussed power management schemes. Multi-objective economic operations were implemented using the cuckoo search algorithm [27]. Microgrid energy management systems were discussed in [28]. Different optimization techniques are described in [29–31] for performing performance analysis and optimizing power flow to improve power quality.

In this manner, the FL and ANFIS control algorithms establish the intelligence knowledge with subjective decisions to regulate the issues in classical PI controllers with efficient rule base and membership functions. In this work, an intelligent ANFIS algorithm-based DC voltage controller has been proposed for the C-UPQC device for better compensation characteristics of enhanced power quality. The proposed control scheme aims to reduce the issues in classical controllers and evidences the intelligence knowledge for mitigating the existing PQ challenges. Using the MATLAB/Simulink software tool, the critical operation and performance of the ANFIS-controlled C-UPQC device are demonstrated with valid comparisons.

Proposed customized UPQC device for power quality improvement

C-UPQC device block diagram for PQ enhancement is shown in Fig. 1, and the three-phase utility grid supplies energy to a nonlinear diode-bridge rectifier (DBR) load through a three-phase distribution network. It involves a supply voltage of Vsabc, a supply current of Isabc, and a rated impedance of Zsabc. The balanced nonlinear DBR load is energized with a load voltage of VLabc and a load current of INLabc, respectively. This nonlinear DBR load injects enormous harmonic distortions into the supply current and affects the PCC voltage. This increases the reactive power demand and also increase rapidly the entire power quality of the distribution network. On the other hand, some of the voltage issues affecting the distribution network are voltage harmonics, voltage sags, voltage swells, voltage flickers, and so on. These voltage issues affect the continuous power flow to loads connected at the PCC of the distribution power system network. The voltage and current quality are the major problems raised in the distribution network, which are compensated for by employing active customized compensation methods. C-UPQC is the best choice among various custom compensation techniques for mitigating source current and/or load current-related PQ issues. The C-UPQC comprises dual voltage source inverters (VSIs) developed as shunt series connections. The dual VSIs of C-UPQC are powered by DC-link capacitor (C_{dc}) which is controlled by using sensor-based reference extraction control schemes with a gate-drive circuitry. DC-link capacitor, C_{dc}, is used to regulate the point of common coupling voltages of the dual parallel VSIs of DSTATCOM. The proposed combined DC-link-fed parallel

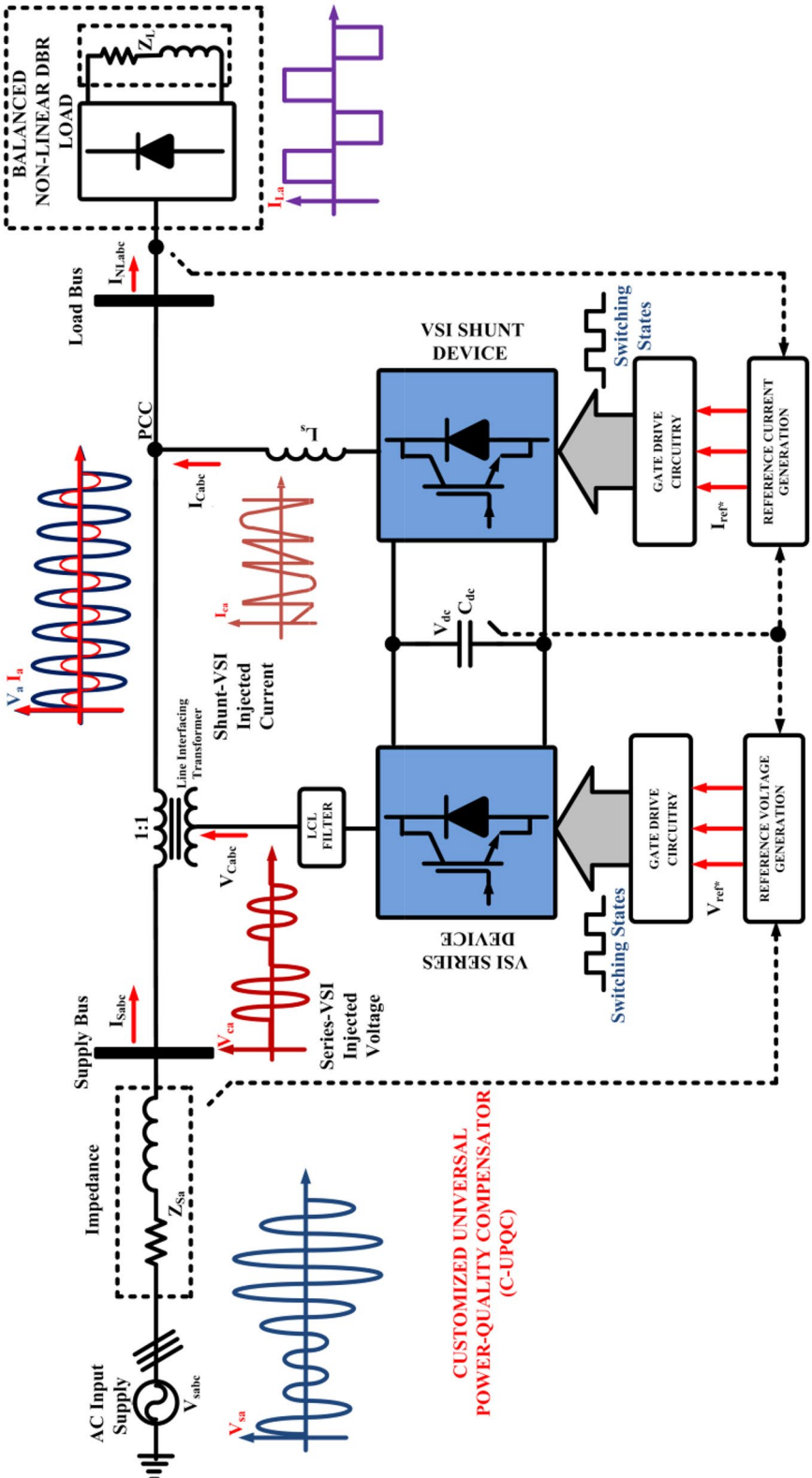


Fig. 1 Schematic of the proposed C-UPQC device for improving PQ

VSI topology requires only a single DC-link capacitor, which offers advantages such as reduced sensing elements, reliable operation, and low-cost compensation compared to the isolated DC-link-fed parallel VSIs topology. To minimize the circulation currents flowing between the DC-link capacitor and the VSIs and to maintain a constant voltage, V_{dc}, across common points, an active DC-link regulator is used. In addition, line-interfacing filters are introduced after the VSI modules to filter the notching and uneven effects during the injection of compensation currents from the VSI modules.

The shunt VSI of C-UPQC functions as an active power compensator for counteracting the harmonics distortion in the supply current by injecting the shunt compensation current as the in-phase current compensation principle. The shunt VSI of C-UPQC manages the supply current to attain harmonic-free response, reactive power exchanging, load balancing and power factor regulation, and so on. It mitigates the current-related issues while maintaining the supply voltage as constant at PCC by injecting the variable currents which are in-phase quadrature of supply voltage through line-interfaced RL filters. It establishes the regulation of reactive power and also maintains the supply-side power factor as a unity nature.

The series VSI of C-UPQC functioned as a series active compensator for counteracting the voltage harmonics and mitigation of voltage sag, swells, and voltage interruptions in load voltage by injecting the series compensation voltage as direct-phase voltage injection principle. The series VSI of C-UPQC is used to manage the load voltage to attain harmonic-free response, maintaining stable and continuous voltage at load terminals or PCC side. It mitigates the voltage-related issues while maintaining the load voltage as constant by injecting the compensation voltages which is in-phase quadrature of PCC voltage through line-interfacing filters and sets the load voltage to an oscillating, fundamental, and balanced nature. Through C-UPQC, the distribution network PCC is enhanced while adhering to IEEE-519/2014 standards through a feasible control technique.

C-UPQC device control schemes

C-UPQC device series VSI control scheme using synchronous reference frame (SRF)

The C-UPQC series VSI is utilized to address voltage-related PQ issues at the distribution system's PCC. To create an appropriate reference voltage signal, the series VSI of C-UPQC employs an SRF control scheme with a sufficient supply voltage value. The accurate supply voltage in an abc-frame (VL.abc) is transformed into a spinning dq-frame (Vdq0.act) using Park's conversion method in a direct and quadrature axis.

$$\begin{bmatrix} V_{d.\mathrm{act}} \\ V_{q.\mathrm{act}} \\ V_{0.\mathrm{act}} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left[\theta - \frac{2\pi}{3}\right] & \cos\left[\theta + \frac{2\pi}{3}\right] \\ \sin\theta & \sin\left[\theta - \frac{2\pi}{3}\right] & \sin\left[\theta + \frac{2\pi}{3}\right] \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_{L.a} \\ V_{L.b} \\ V_{L.c} \end{bmatrix} \tag{1}$$

$$\theta = \int \omega . \mathrm{d}t \tag{2}$$

A PI controller's transfer function is expressed as follows:

$$U_{\mathrm{err}}(s) = k_{\mathrm{pa}} + \frac{k_{ia}}{s} E_{\mathrm{err}}(s) \tag{3}$$

Figure 2 shows a block diagram of the SRF control scheme for series VSI in C-UPQC. The outcome error sequences are minimized by using PI controller which is considered as final reference voltage signal $V_{\mathrm{dq.ref^*}}$. Subsequently, the attained reference voltage in dq-frame is re-transformed into exact abc-frame by employing inverse Park's transformation technique, as expressed in Eq. (4),

$$V^*_{dq.\mathrm{ref}} = (V_{dq.\mathrm{ref}} - V_{dq.\mathrm{act}}) \tag{4}$$

$$\begin{bmatrix} V_{a.\mathrm{ref}} \\ V_{b.\mathrm{ref}} \\ V_{c.\mathrm{ref}} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos\left[\theta - \frac{2\pi}{3}\right] & \sin\left[\theta - \frac{2\pi}{3}\right] & 1 \\ \cos\left[\theta + \frac{2\pi}{3}\right] & \sin\left[\theta + \frac{2\pi}{3}\right] & 1 \end{bmatrix} \begin{bmatrix} V^*_{d.\mathrm{ref}} \\ V^*_{q.\mathrm{ref}} \end{bmatrix} \tag{5}$$

Finally, the extracted reference voltage from SRF control scheme is compared with measured voltage value for generation of switching pulses to series VSI of C-UPQC by using sinusoidal pulse-width modulation (SPWM) technique.

Series VSI power control scheme for C-UPQC devices with instantaneous real-reactive power

In most instances, the IRP controller is implemented as Clarke's conversion technique, which converts standard *abc* into symmetric $\alpha\beta$ coordinates in a stationary frame. The supply voltage $V_{\mathrm{st}.abc}$ and the nonlinear distorted load currents $I_{\mathrm{NL}.abc}$ are transformed into symmetric frames for managing both real and reactive powers as $(V_{\mathrm{st}.\alpha\beta}, I_{\mathrm{NL}.\alpha\beta})$. The conversion procedure of Clarke's transformation expresses the supply voltage and nonlinear distorted currents in Eqs. (6) and (7),

$$\begin{bmatrix} v_{\mathrm{st}.\alpha} \\ v_{\mathrm{st}.\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} v_{\mathrm{st}.a} \\ v_{\mathrm{st}.b} \\ v_{\mathrm{st}.c} \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} i_{\mathrm{NL}.\alpha} \\ i_{\mathrm{NL}.\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{NL}.a} \\ i_{\mathrm{NL}.b} \\ i_{\mathrm{NL}.c} \end{bmatrix} \tag{7}$$

$$p = v_{\mathrm{st}.\alpha} i_{\mathrm{NL}.\alpha} + v_{\mathrm{st}.\beta} i_{\mathrm{NL}.\beta} \tag{8}$$

$$q = -v_{\mathrm{st}.\beta} i_{\mathrm{NL}.\alpha} + v_{\mathrm{st}.\alpha} i_{\mathrm{NL}.\beta} \tag{9}$$

Matrix-form representation of the attained power components is as follows:

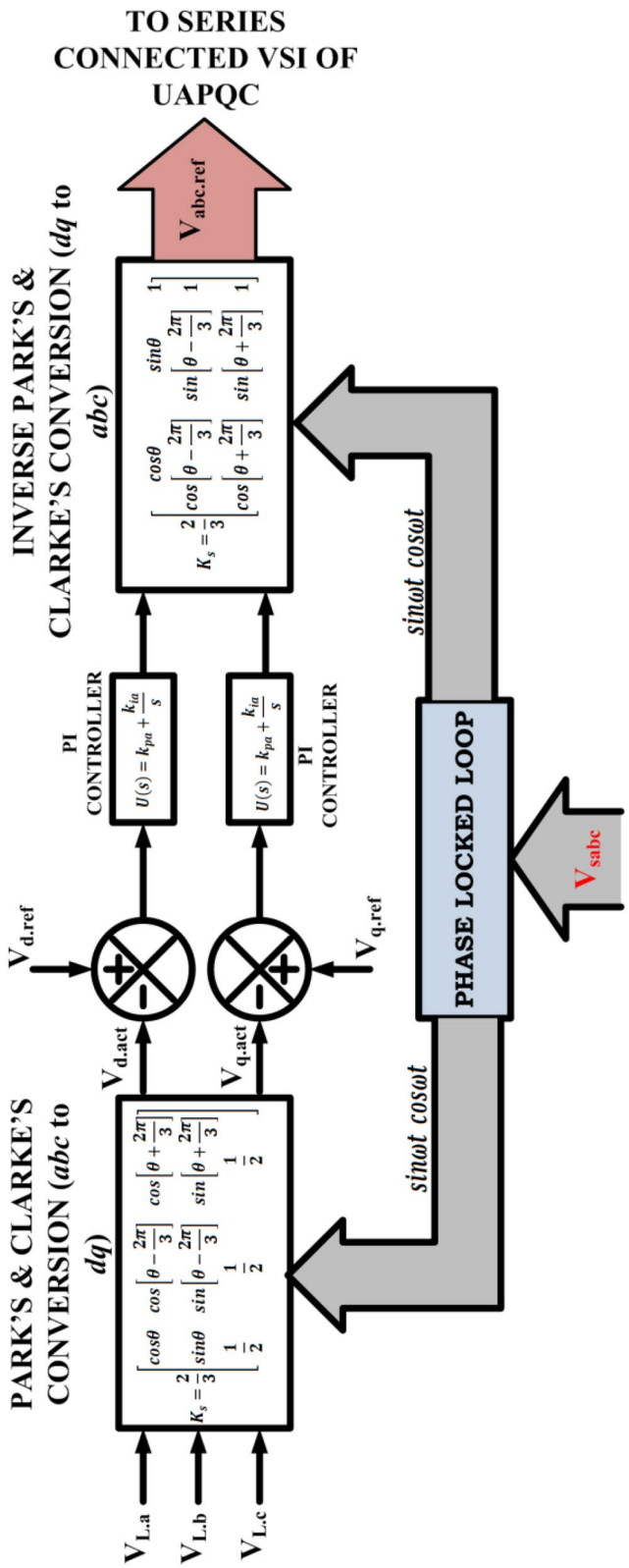


Fig. 2 Schematic of the SRF control scheme for the series VSI of C-UPQC

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_{\mathrm{st}.\alpha} & v_{\mathrm{st}.\beta} \\ -v_{\mathrm{st}.\beta} & v_{\mathrm{st}.\alpha} \end{bmatrix} \begin{bmatrix} i_{\mathrm{NL}.\alpha} \\ i_{\mathrm{NL}.\beta} \end{bmatrix} \tag{10}$$

Distorted load currents in symmetric frames are expressed as follows:

$$\begin{bmatrix} i_{\mathrm{NL}.\alpha} \\ i_{\mathrm{NL}.\beta} \end{bmatrix} = \frac{1}{\Delta_k} \begin{bmatrix} v_{\mathrm{st}.\alpha} & v_{\mathrm{st}.\beta} \\ -v_{\mathrm{st}.\beta} & v_{\mathrm{st}.\alpha} \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \tag{11}$$

where

$$\Delta_k = v_{\mathrm{st}.\alpha}^2 + v_{\mathrm{st}.\beta}^2 \tag{12}$$

The resulting controlling components at the nth point is given below:

$$V_{\mathrm{dc.er}} = V_{\mathrm{dc}.r}^* - V_{\mathrm{dc}.a} \tag{13}$$

$$\Delta_{ia.\mathrm{dc}} = K_{p.d} * \left(V_{\mathrm{dc.er}(n)} - V_{\mathrm{dc.er}(n-1)}\right) + K_{i.d} * \left(V_{\mathrm{dc.er}(n)}\right) \tag{14}$$

The performance of a PI controller is always dependent on the selection of feasible gains with necessary steps using the Ziegler–Nichols method. Because of this method, the traditional PI controller does not auto-tune the gain values during parametric variations, sudden variations, and affecting the overall system stability. Several artificial advanced intelligence approaches are used in a variety of domestic and industrial applications, with the adaptive neuro-fuzzy inference system (ANFIS) playing an important part in control schemes due to increased performance attributes over traditional PI and fuzzy logic control schemes. ANFIS control schemes are distinguished by their use of symbolic notation in conjunction with an expertise inference knowledge base. The block diagram of ANFIS control model is shown in Fig. 3.

Although the ANFIS procedure is more precise and efficient. Layer creation is evaluated by the ANFIS controller for improved error value reduction and specifies the control mechanism that minimizes error values. The structure of ANFIS control scheme is

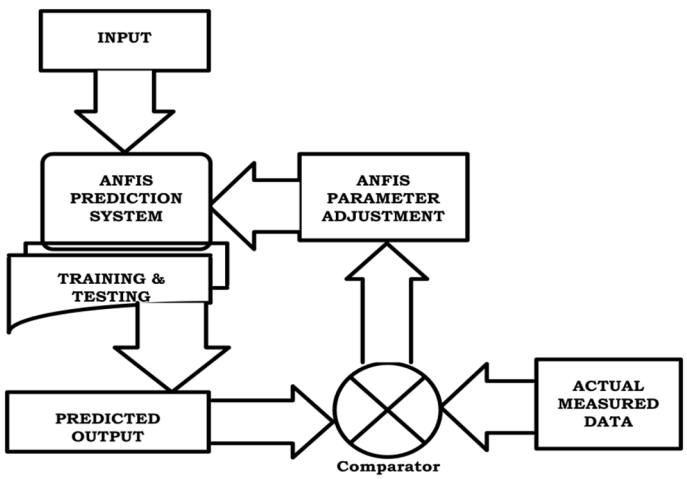


Fig. 3 Block diagram of ANFIS control model

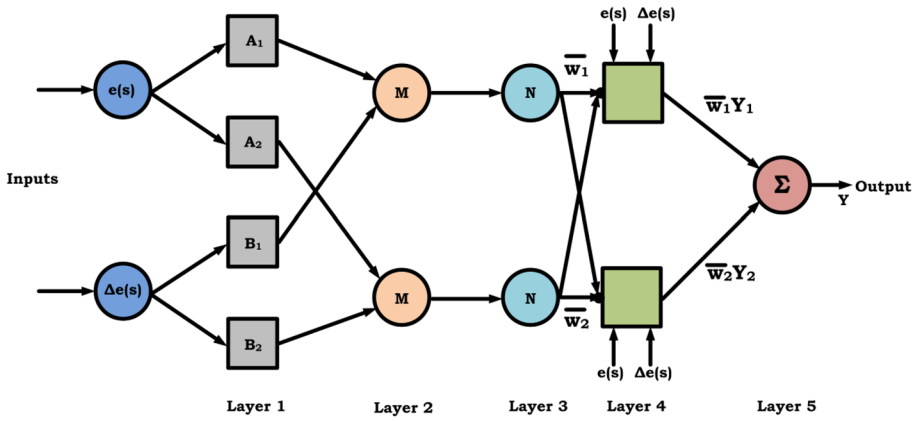


Fig. 4 Structure of ANFIS control scheme

shown in Fig. 4. In the present ANFIS control system, a supervised learning approach is used to train the membership functions in order to deduct the required output during nominal time periods. The ANFIS controller approach involves two phases. In the first phase, the available fuzzy data are verified and converted into required data by detecting errors, changes in error, and output requirements. In the second phase, the given fuzzy data are retransformed into workable membership functions and rule base using a superior training approach connected to the required output DC-link voltage. By providing clear correspondence rules between input and output, the combination of artificial neural networks with fuzzy logic rules enables a better understanding of the control scheme. Although the ANFIS procedure is more precise and efficient, layer creation is evaluated by the ANFIS controller for improved error value reduction and specifies the control mechanism that minimizes error values. The structure of the ANFIS control scheme is shown in Fig. 4.

The feasible membership functions and rule base are trained with the required output by using a hybrid-weighting function algorithm, which is a combination of least squares and backpropagation algorithms for analyzing the various parameters of membership functions used in this work. Based on testing and training, the ANFIS control scheme generates new membership functions and rule base for the regulation of error sequences in the DC-link voltage of the IRP control scheme. The membership functions of available ANFIS data, such as error "$e(s)$" and change in error "$\Delta e(s)$" in the first step of the ANFIS controller are shown in Fig. 5.

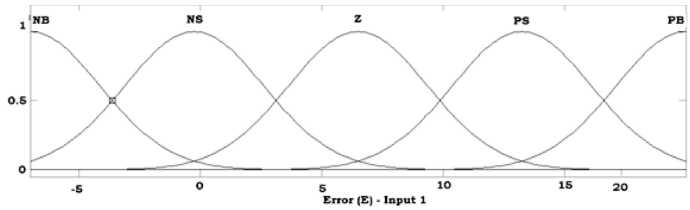
$$\mathrm{e(s)} = V^{*}_{\mathrm{dc}.r} - V_{\mathrm{dc}.a} \tag{15}$$

$$\Delta e(s) = e(s) - e(s-1) \tag{16}$$

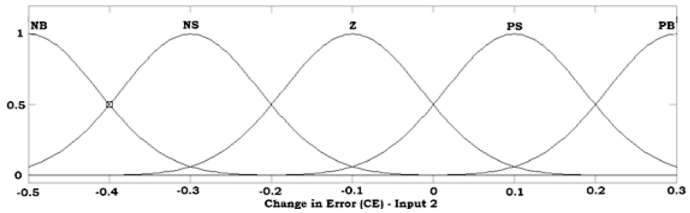
where e(s) and $\Delta e(s)$ are the error and change in error.

The ANFIS control scheme rules are tabulated in Table 1.

There are two types of instantaneous components: oscillatory DC values and averaging AC values,



(a) Error $e(s)$



(b) Change in Error $\Delta e(s)$

Fig. 5 ANFIS control scheme membership functions

Table 1 ANFIS control scheme rules

$e(s)/\Delta e(s)$	NB	NS	Z	PS	PB
NB	R1	R2	R3	R4	R5
NS	R6	R7	R8	R9	R10
Z	R11	R12	R13	R14	R15
PS	R16	R17	R18	R19	R20
PB	R21	R22	R23	R24	R25

$$p = \overline{p} + \widetilde{p}$$

$$q = \overline{q} + \widetilde{q} \tag{17}$$

The extracted final reference current signal ($i^*_{cr.\alpha\beta}$) in αβ symmetric frame is expressed as:

$$\begin{bmatrix} i^*_{\mathrm{cr}.\alpha} \\ i^*_{\mathrm{cr}.\beta} \end{bmatrix} = \frac{1}{\Delta_k} \begin{bmatrix} v_{\mathrm{st}.\alpha} & -v_{\mathrm{st}.\beta} \\ v_{\mathrm{st}.\beta} & v_{\mathrm{st}.\alpha} \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \tag{18}$$

The block diagram of proposed ANFIS-IRP control scheme is shown in Fig. 6.

$$\begin{bmatrix} i^*_{\mathrm{cr}.a} \\ i^*_{\mathrm{cr}.b} \\ i^*_{\mathrm{cr}.c} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i^*_0 \\ i^*_{c.\alpha} \\ i^*_{c.\beta} \end{bmatrix} \tag{19}$$

Figure 7 shows the overall block diagram of the proposed ANFIS-IRP/SRF-controlled customized UPQC device for PQ enhancement.

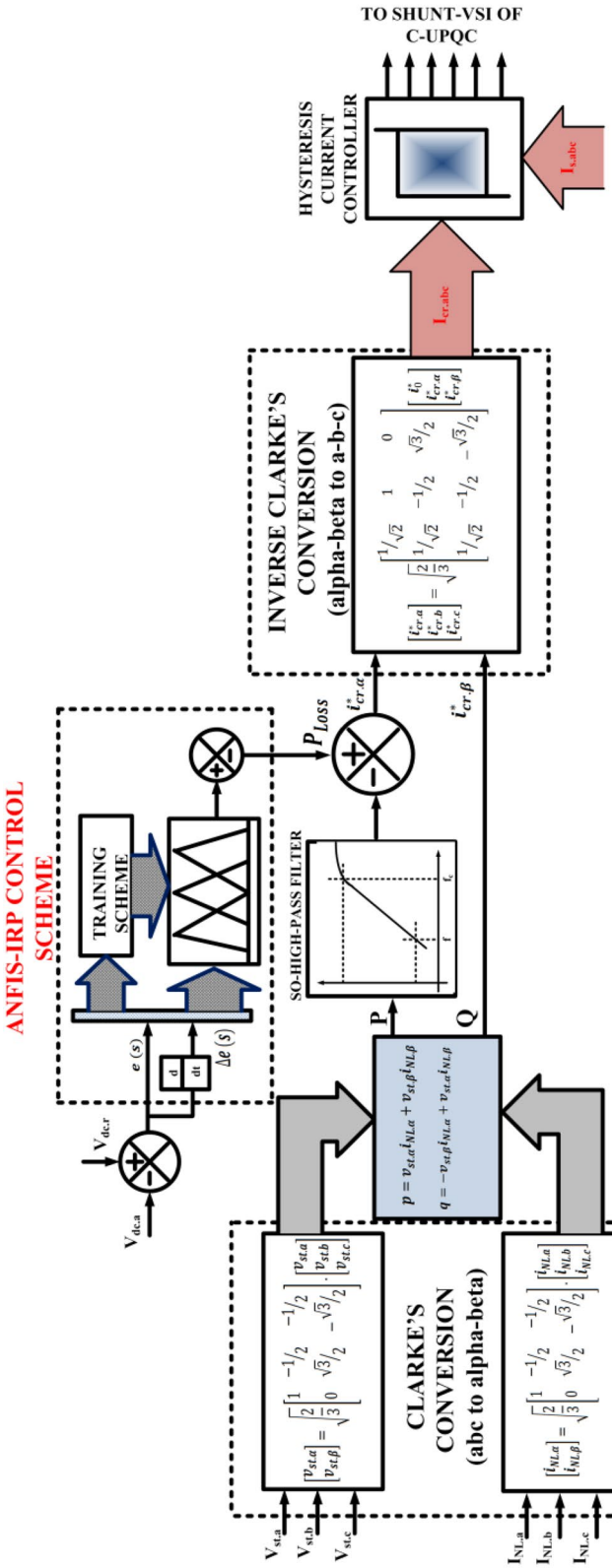


Fig. 6 Block diagram of ANFIS-IRP control scheme for shunt VSI of C-UPQC device

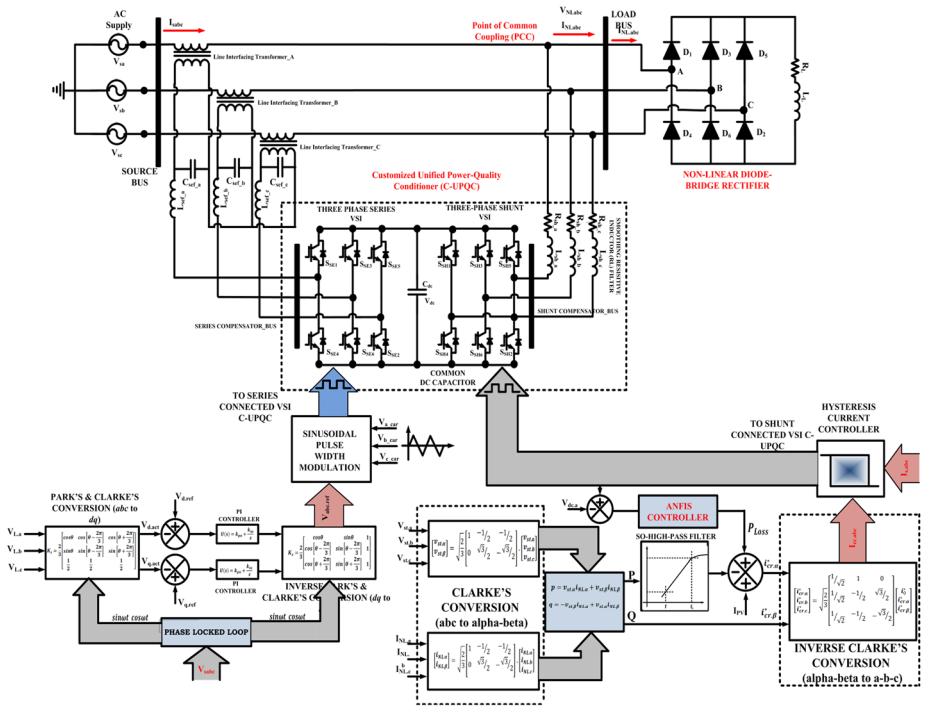


Fig. 7 Overall block diagram of proposed ANFIS-IRP/SRF-controlled customized UPQC device for PQ enhancement

Table 2 System parameters

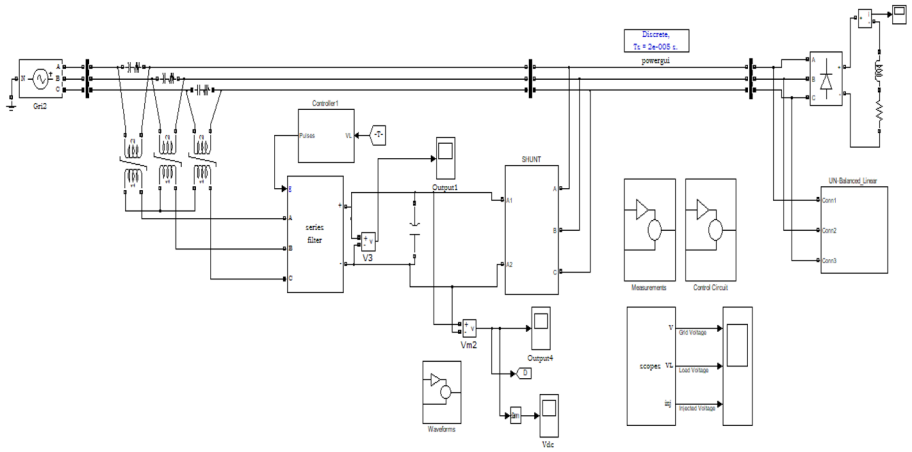
Sl. no.	Parameters	Values
1	Supply voltage	V_{sabc}-415 V, F_S-50 Hz
2	Supply impedance	Rs-0.1 Ω, Ls-0.9 mH
3	Nonlinear load impedance	R_{NL}-20 Ω, L_{NL}-30 mH
4	DC capacitor value	V_{dc}-880 V, C_{dc}-1500 µF
5	VSI's filter impedance	R_f-0.1 Ω, L_f-5 mH
6	PI controller	K_p-2.5, K_i-0.5

MATLAB/Simulink results

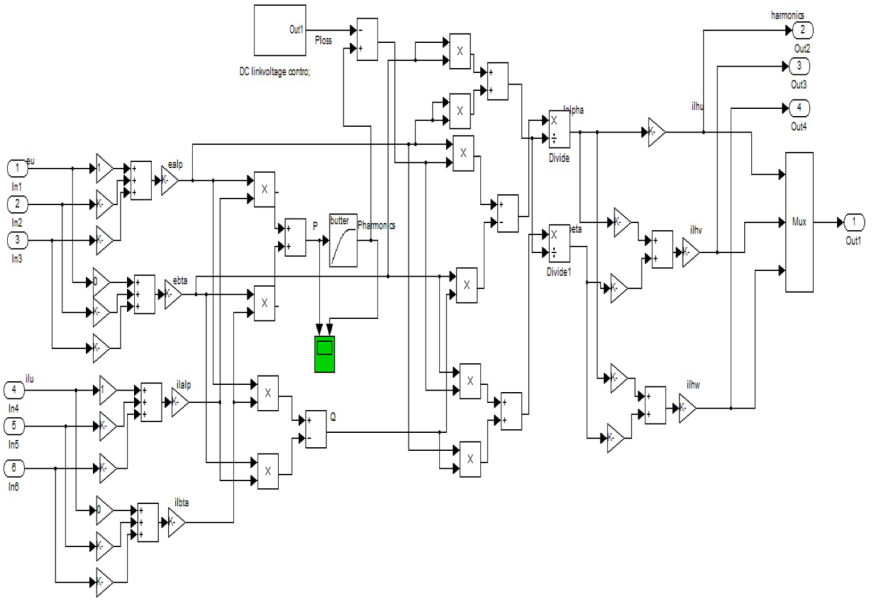
The critical operation and performance of ANFIS-controlled customized UPQC device for PQ improvement are verified. The system parameters of C-UPQC device are presented in Table 2.

Performance of customized UPQC using traditional PI-IRP/SRF control schemes for PQ enhancement

Figures 8 and 9 show the MATLAB/Simulink model and simulation results of traditional PI-IRP/SRF control schemes for customized UPQC for PQ enhancement. It includes (a) voltage and current waveforms under harmonic current compensation, (b) voltage waveforms under voltage sag–swells compensation, (c) supply terminal voltage and current (in-phase), (d) THD spectrum of nonlinear distorted load current, and (e) THD spectrum of supply current, accordingly. In that, the supply voltage of distribution network is maintained as sinusoidal



(a) Diagram showing main Simulink components



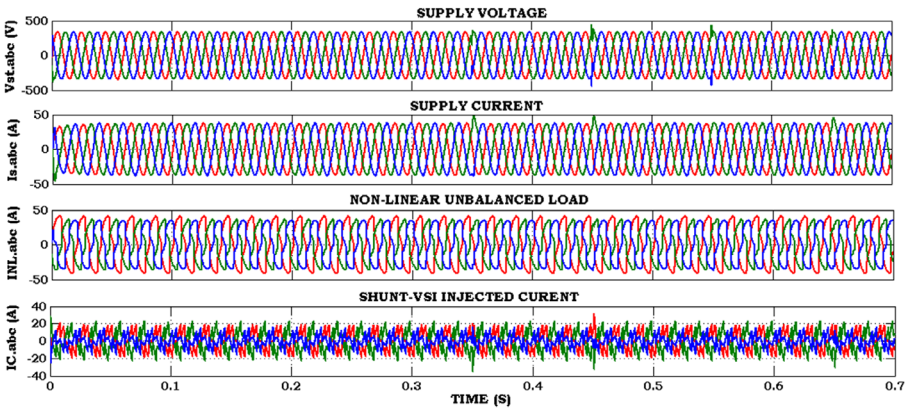
(b) Control circuit subsystem block 1

Fig. 8 MATLAB/Simulink model of traditional PI-IRP/SRF control schemes for customized UPQC device for PQ enhancement

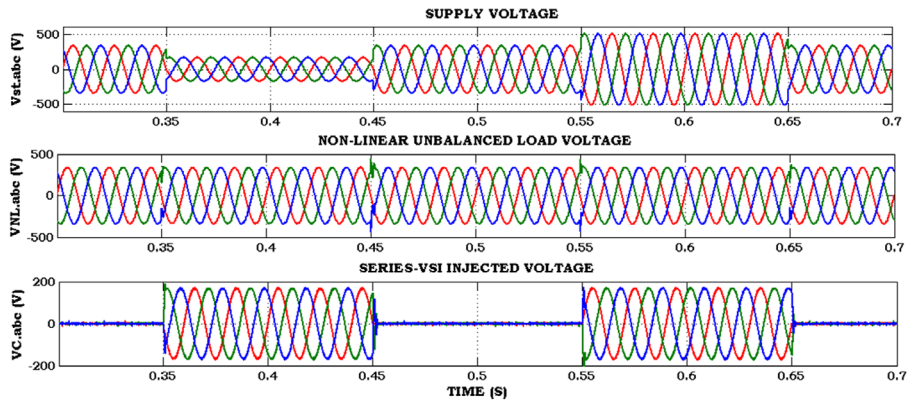
voltage with a value of 415 V, 50 Hz supply to drive the nonlinear unbalanced load. Due to this load, the supply current has been distorted due to injection of harmonic currents coming from the nonlinear unbalanced load. These distorted currents affecting the other loads integrated near to PCC level damage the loads due to increased thermal losses. Implementing the PI-IRP-controlled C-UPQC system can effectively counteract harmonic distortions in the supply current, enabling us to achieve a load current of 36A with a supply current of 38A. The shunt VSI of C-UPQC injects the compensation current of 20A to regulate supply currents as balanced, sinusoidal in shape as shown in Fig. 9a.

The C-UPQC is a series VSI system that uses traditional PI-SRF control to mitigate voltage sags and swells in load voltage. Its purpose is to maintain a balanced, sinusoidal,

and linear load voltage that matches the supply voltage. Before $t-0.35$ s, the supply voltage stays constant at 340 V. However, if a voltage sag occurs between $t-$ 0.35 s and 0.45 s, the supply voltage drops to 170 V, disrupting the performance of loads. To fix this, a traditional PI-SRF-controlled C-UPQC device injects a compensation voltage of 170 V to maintain a constant load voltage of 340 V. Similarly, if a voltage swell occurs between $t-0.55$ s and 0.65 s, the supply voltage increases to 510 V, which can also disrupt load performance. In this case, a traditional PI-SRF-controlled C-UPQC device extracts an additional voltage of 170 V to maintain a constant load voltage of 340 V. You can see the results in Fig. 9b. Accordingly, the supply current is always in-phase with the supply voltage, demonstrating a unity power factor at the supply side, as shown in Fig. 9c. The THD spectrum of the nonlinear distorted load current has been measured at 21.77%, while the THD spectrum of the supply current has been measured at 3.30%, which conforms to the IEEE-519/2014 standards, as shown in Fig. 9d and e.

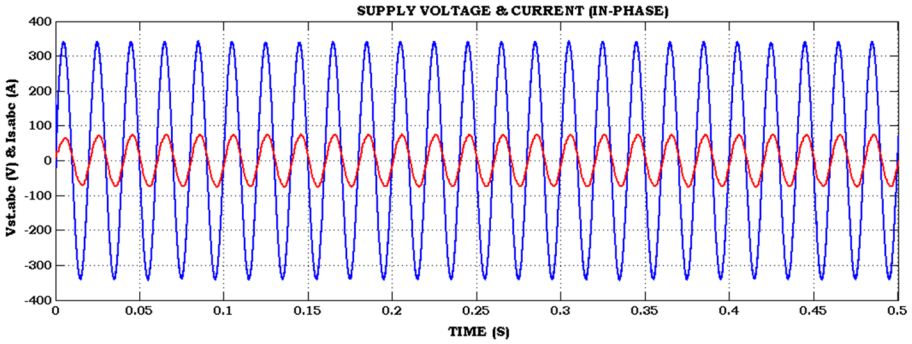


(a) Voltage & Current Waveforms under Harmonic Currents Compensation

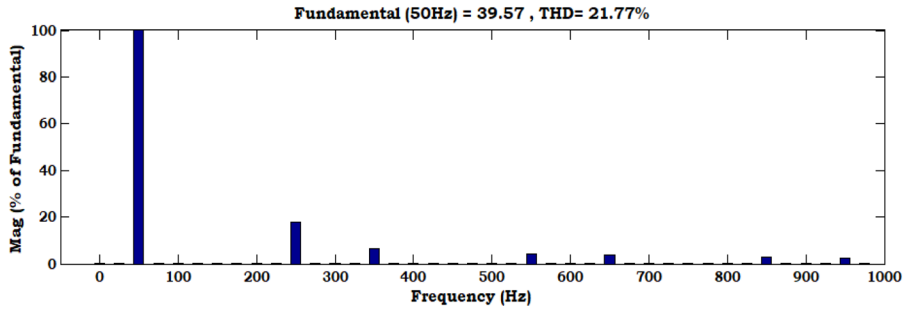


(b) Compensation for voltage sag-swells in voltage waveforms

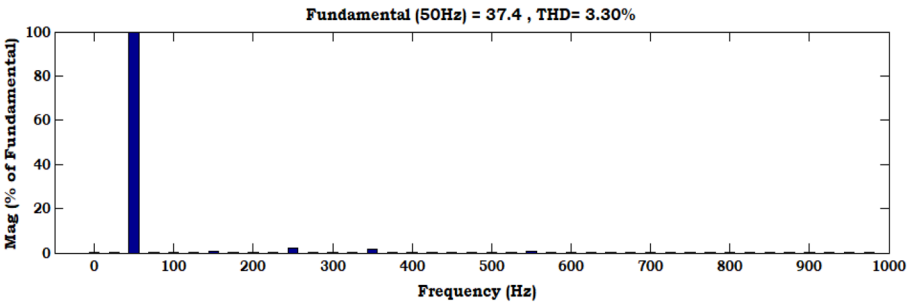
Fig. 9 Simulation results of traditional PI-IRP/SRF control schemes for customized UPQC for PQ enhancement



(c) Voltage and current at the supply terminal (in-phase)



(d) Nonlinear Distorted Current THD Spectrum



(e) Supply current spectrum with THD

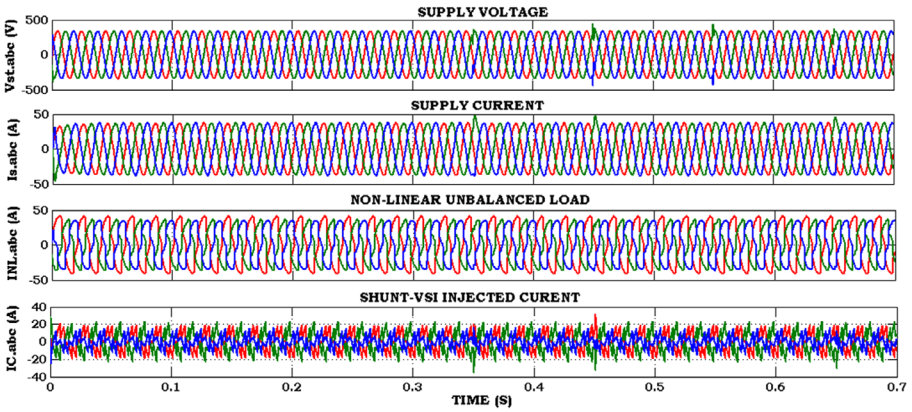
Fig. 9 continued

Performance of customized UPQC using traditional FL-IRP/SRF control schemes for PQ enhancement

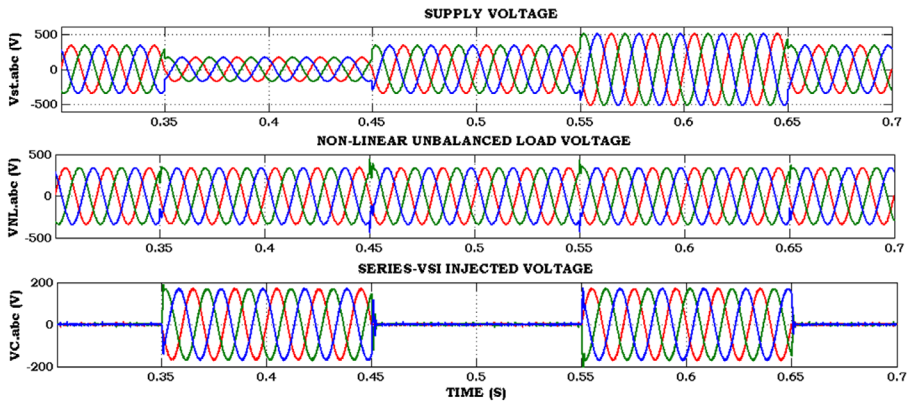
Figure 11 shows the simulation results of traditional FL-IRP/SRF control schemes for customized UPQC for PQ enhancement. It includes (a) voltage and current waveforms under harmonic current compensation, (b) voltage waveforms under voltage sag–swells compensation, (c) supply terminal voltage and current (in-phase), (d) THD spectrum of nonlinear distorted load current, and (e) THD spectrum of supply current, accordingly. In that, the supply voltage of distribution network is maintained as sinusoidal voltage with a value of 415 V, 50 Hz supply to drive the nonlinear unbalanced load. Due to this load, the supply current has been distorted due to injection of harmonic currents coming from the nonlinear unbalanced load. These distorted currents affecting the other loads integrated near to PCC level damage the loads due to increased thermal losses.

Using a traditional FL-IRP-controlled C-UPQC device, the harmonic distortions in the supply current are counteracted to achieve a load current of 36A with a supply current of 38A. The FL controller produces the linguistic variables with intelligence knowledge for regulating the compensation currents by using fuzzy membership functions and rule base. The shunt VSI of C-UPQC injects the compensation current of 20A to regulate supply currents as balanced, sinusoidal in shape as shown in Fig. 10a.

In the C-UPQC system, the traditional FL-SRF-controlled series VSI helps maintain balanced, sinusoidal, and linear load voltage despite voltage sags or swells coming from the supply voltage. Before $t-0.35$ s, the supply voltage is constant and sinusoidal at 340 V. When a voltage sag occurs between $t-0.35$ s and 0.45 s, the supply voltage drops to 170 V, disrupting the load performance. The traditional FL-SRF-controlled C-UPQC device injects 170 V of compensation voltage to maintain a constant load voltage of 340 V. Conversely, when a voltage swell occurs between $t-0.55$ s and 0.65 s, the supply voltage increases to 510 V, also disrupting the load performance. In this case, the traditional FL-SRF-controlled C-UPQC device extracts an additional 170 V to maintain a constant load voltage of 340 V, as shown in Fig. 10b. As a result, the supply current is always in-phase with the supply voltage, representing a unity power factor at the supply

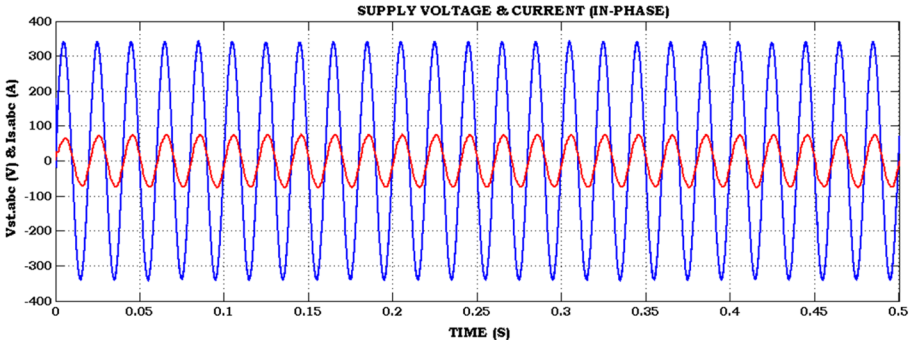


(a) Voltage & Current Waveforms under Harmonic Currents Compensation

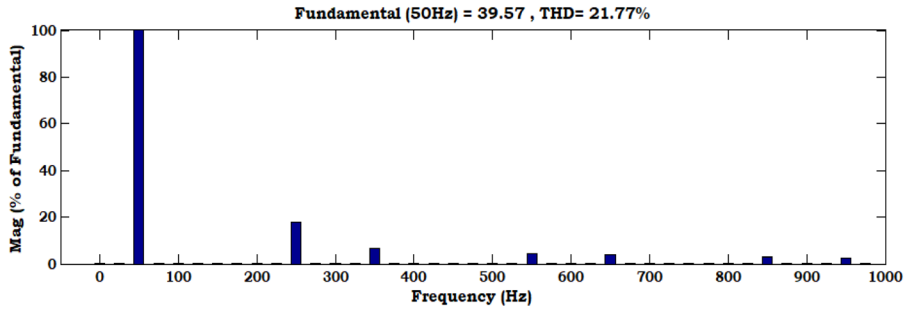


(b) Voltage Waveforms under Voltage Sag-Swells Compensation

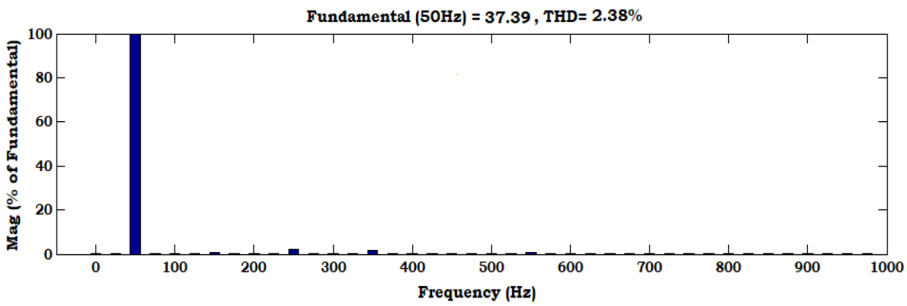
Fig. 10 Simulation results of traditional FL-IRP/SRF control schemes for customized UPQC for PQ enhancement



(c) Voltage and current at the supply terminal (in-phase)



(d) Nonlinear Distorted Current THD Spectrum



(e) Supply current spectrum with THD

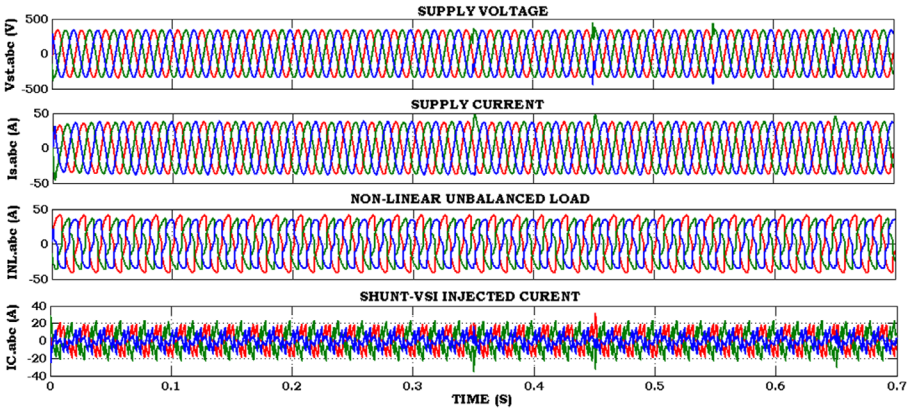
Fig. 10 continued

side (Fig. 10c). The nonlinear distorted load current has a THD spectrum of 21.77%, while the supply current has a THD spectrum of 2.38%, which complies with the IEEE-519/2014 standards (Fig. 10d, e).

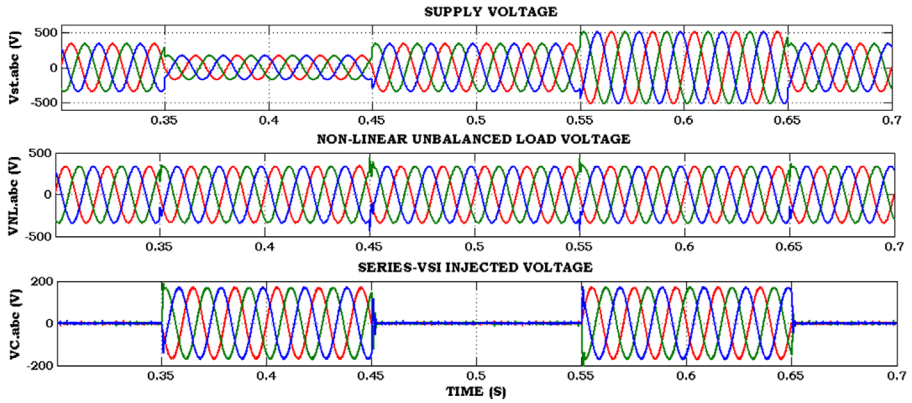
Performance of customized UPQC using proposed ANFIS-IRP/SRF control schemes for PQ enhancement

Figure 11 shows the simulation results of proposed ANFIS-IRP/SRF control schemes for customized UPQC for PQ enhancement. It includes (a) voltage and current waveforms under harmonic currents compensation, (b) voltage waveforms under voltage sag–swells compensation, (c) supply terminal voltage and current (in-phase), (d) THD spectrum of nonlinear distorted load current, and (e) THD spectrum of supply current, accordingly. In that, the supply voltage of distribution network is maintained as sinusoidal voltage

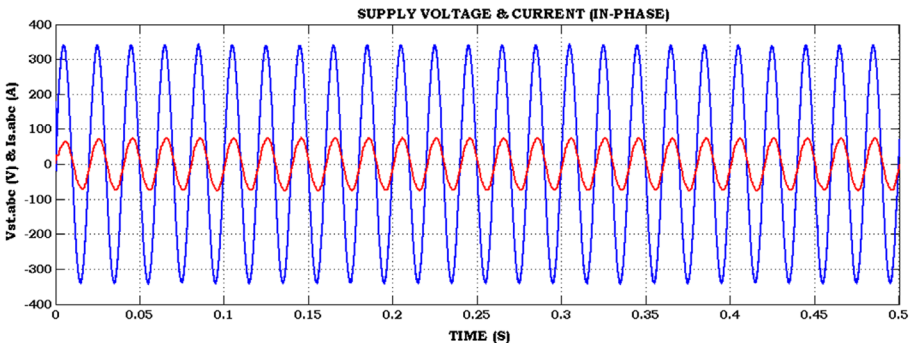
with a value of 415 V, 50 Hz supply to drive the nonlinear unbalanced load. Due to this load, the supply current has been distorted due to injection of harmonic currents coming from the nonlinear unbalanced load. These distorted currents affecting the other loads integrated near to PCC level damage the loads due to increased thermal losses. Using a traditional ANFIS-IRP-controlled C-UPQC device, the harmonic distortions



(a) Voltage & Current Waveforms under Harmonic Currents Compensation

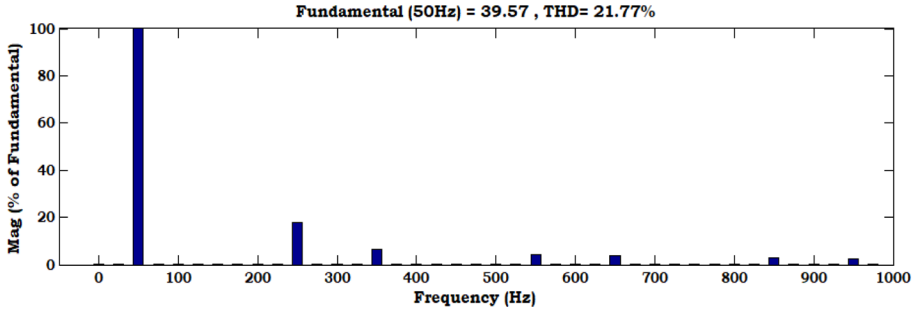


(b) Voltage Waveforms under Voltage Sag-Swells Compensation

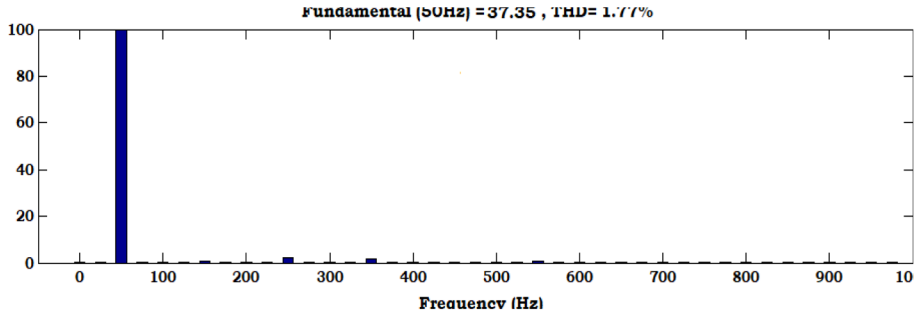


(c) Voltage and current at the supply terminal (in-phase)

Fig. 11 Simulation results of proposed ANFIS-IRP/SRF control schemes for customized UPQC for PQ enhancement



(d) Nonlinear Distorted Current THD Spectrum



(e) Supply current spectrum with THD

Fig. 11 continued

Table 3 Comparison of nonlinear distorted load currents and supply currents

THD (%)	Nonlinear distorted load current (%)	Supply current (%)
Without C-UPQC device	21.83	21.77
With traditional PI-IRP-controlled C-UPQC	21.79	3.30
With traditional FL-IRP-controlled C-UPQC	21.77	2.38
With proposed ANFIS-IRP-controlled C-UPQC	21.77	1.77

in the supply current are counteracted to achieve a load current of 36A with a supply current of 38A. The ANFIS controller produces the supervised learning approach with intelligence knowledge for regulation of the compensation currents by training the membership functions and rule base with minimum epochs. The shunt VSI of C-UPQC injects the compensation current of 20 A to regulate supply currents as balanced, sinusoidal in shape as shown in Fig. 11a.

The ANFIS-SRF-controlled series VSI of C-UPQC is designed to address voltage sags and swells in load voltage caused by fluctuations in supply voltage. Its aim is to maintain load voltage as balanced, sinusoidal, and linear. Prior to a voltage sag, which occurs before $t-0.35$ s, the supply voltage remains constant at 340 V. In the event of a voltage sag occurring between $t-0.35$ s and 0.45 s, the supply voltage drops to 170 V, causing a disruption in the performance of loads. However, the proposed ANFIS-SRF-controlled C-UPQC device can inject the required compensation voltage of 170 V to maintain load voltage at a constant value of 340 V. In the case of a voltage swell occurring between

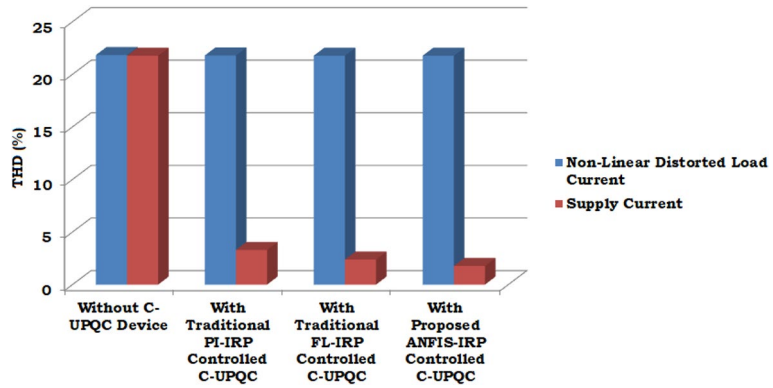


Fig. 12 Graphical representation of nonlinear distortions in load and supply currents

$t-0.55$ s and 0.65 s, the supply voltage increases to 510 V, causing a disruption in the performance of loads. Using the proposed ANFIS-SRF-controlled C-UPQC device, an additional voltage of 170 V is extracted to keep the load voltage constant at 340 V, as shown in Fig. 11b. This ensures that the supply current is always in-phase with the supply voltage, resulting in a unity power factor on the supply side, as shown in Fig. 11c. The THD spectrum of the nonlinear distorted load current is measured at 21.77%, while the THD spectrum of the supply current is measured at 1.77%, which complies with IEEE-519/2014 standards, as shown in Fig. 11d and e. Table 3 and Fig. 12 illustrate the THD comparisons and graphical view of nonlinear distorted load current and supply currents of traditional PI-IRP/SRF, FL-IRP/SRF, and proposed ANFIS-IRP/SRF control schemes for customized UPQC device. Among the traditional PI/FL-IRP/SRF control schemes for C-UPQC, the proposed ANFIS-IRP/SRF-controlled device has superior PQ compensation features.

Conclusions

In this work, attractive performance of proposed customized UPQC device has been verified under both voltage and current allied PQ issues by employing intelligent control schemes. The proposed ANFIS control scheme establishes the intelligence knowledge base with subjective decisions in accordance with significant rule base and membership functions by using supervised learning methodology. The proposed ANFIS-IRP/SRF-controlled C-UPQC device mitigates the harmonic distortions in supply current and voltage sag–swells in load voltage over the traditional PI-IRP/SRF and FL-IRP/SRF control schemes. The measured THD values of supply current in ANFIS-IRP/SRF-controlled C-UPQC device are complying with IEEE-519/2014 standards.

Abbreviations

AC	Alternating current
DC	Direct current
EPS	Electric power system
PCC	Point of common coupling
PQ	Power quality
UPQC	Unified power quality compensator
C-UPQC	Customized universal power quality compensator
CPT	Customized power technology
CPD	Custom power device

DSTATCOM	Distribution static compensator
DVR	Dynamic voltage restorer
VSI	Voltage source inverter
C_{dc}	DC-link capacitor
DBR	Diode-bridge rectifier
PLL	Phase locked loop
HCC	Hysteresis current controller
APF	Active power filter
SAPF	Series active power filter
SHAPF	Shunt active power filter
SRF	Synchronous reference frame
IRP	Instantaneous real-reactive power
PI	Proportional integral
FLC	Fuzzy logic control
ANFIS	Adaptive neuro-fuzzy inference system

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Author contributions
SS wrote the main text of the manuscript; BM and JU revised the manuscript. All authors read and approved the final manuscript.

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Declarations

Competing interests
The authors declare that they have no competing interests. All authors approved the final manuscript.

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