BULLETIN OF THE POLISH ACADEMY OF SCIENCES
TECHNICAL SCIENCES, Vol. 63, No. 4, 2015
DOI: 10.1515/bpasts-2015-0104

Current mode sigma-delta modulator designed with the help of transistor's size optimization tool

P. ŚNIATAŁA[1]*, M. NAUMOWICZ[1], A. HANDKIEWICZ[1], S. SZCZĘSNY[1], J.L.A. de MELO[2], N. PAULINO[2], and J. GOES[2]

[1] Poznań University of Technology, 3A Piotorowo St., 60-965 Poznań, Poland
[2] UNINOVA/CTS, Universidade Nova de Lisboa, 2829-516 Caparica, Portugal

Abstract. The paper presents a second order current mode sigma-delta modulator designed with the help of a new elaborated tool to optimize the transistor sizes. The circuit is composed of two continuous time loop filters, a current comparator and a one bit DAC with a current output. The resulting circuit, designed in a 65 nm 1.2 V CMOS technology, has a bandwidth of 2 MHz for a clock frequency of 250 MHz. The electrical simulation results show that it achieves a maximum signal-to-noise-plus-distortion ratio (SNDR) of 53.6 dB while dissipating 93 μW, which corresponds to an efficiency of 59.7 fJ/conv. The fully current mode structure makes the circuit suitable to be applied in a current mode signal processing like biosensors or image pixels arrays.

Key words: sigma-delta, current comparator, CAE.

1. Introduction

The development of new electronic technologies allows increasing the complexity of modern System on Chip devices (SoC). They contain the complete analog and digital processing chain. Analog solutions are also often applied in portable devices, where the power consumption and the circuit area are critical issues. Several interesting results regarding the A/D and D/A were discussed in [1–3]. Current mode circuits are good candidates to fulfill these requirements. In many applications of signal processing, the information is represented as a current. As examples can be mentioned some types of analog to digital converters or circuits, pulsed neural networks or analog parallel systems that perform the processing of the image data i.e. image sensors. The current output pixels have two main advantages over their voltage counterparts. Current outputs allow simplifying many on-chip computation tasks, which can be implemented on the focal plane using current mode computation-on-readout. Another advantage of using current mode pixels is eliminating the requirement to charge and discharge the column capacitances during readout. It allows achieving significantly higher scan-out rates [4]. The natural choice for a current mode processing chain is to connect it to a current mode analog-to-digital converter. Keeping in mind the requirements regarding the power consumption and size minimization, sigma-delta structure can be taken into consideration. This paper proposes a second order modulator structure. The following section presents blocks used in the design. The circuit is composed of two continuous time low pass filters (loop filters shaping the noise), followed by current comparator and one bit DAC with a current output. The comparator circuit's structure is optimized in terms of required output amplification. The new elaborated EDA tool was used to find the optimal transistor dimensions for a given technology. Section 3 presents the program and the simulation results for the circuit designed for TSMC 65 nm CMOS Process Technology.

2. Modulator structure

The sigma-delta modulator (SDM) proposed in this paper is a second order structure as presented in Fig. 1. It consists of two current mode low pass filters (LPF), current comparator, flip-flop block and DACs with current output. The following subsections briefly describe each block.

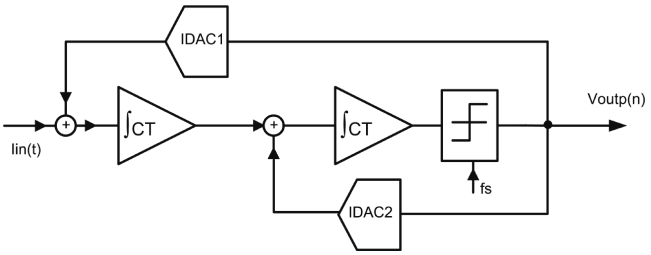

Fig. 1. Second order structure of the modulator

2.1. CT current mode loop filter. A continuous time, current mode integrator was introduced by Smith, Sanchez-Sinencio and Zele, Allstot in [5] and [6]. The proposed circuit is a simplified version of such integrator and is built only with the use of the current mirror with additional capacitance attached to the transistor gates. In order to derive the transfer function of the proposed circuit, one can analyze the current mirror's small signal model presented in Fig. 2.

*e-mail: Pawel.Sniatala@put.poznan.pl

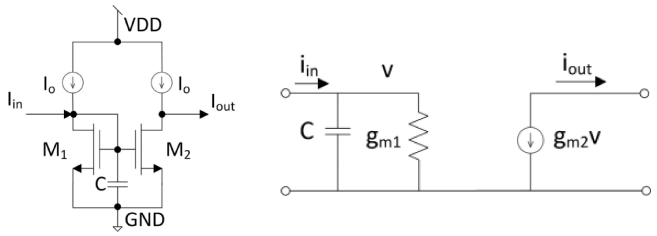

Fig. 2. Current mirror structure and its small-signal model

The transfer function of the current mirror, derived from the presented small-signal model, can be expressed by Eq. (1)

$$H_M(s) = \frac{i_{\text{out}}(s)}{i_{\text{in}}(s)} = \frac{-\frac{g_{m2}}{C}}{s + \frac{g_{m1}}{C}}. \tag{1}$$

This expression neglects output conductance and parasitic capacitance. Assuming identical transistors, i.e. current mirror scaling factor equal to 1, Eq. (1) can be further simplified to (2).

$$H_M(s) = \frac{i_{\text{out}}(s)}{i_{\text{in}}(s)} = \frac{-\frac{g_m}{C}}{s + \frac{g_m}{C}} = \frac{-g_m}{sC + g_m}. \tag{2}$$

According to Eq. (2) the presented circuit can work as a low pass filter, which acts as a loop-filter in the modulator structure. The theoretical model, calculated with the help of MATLAB, quite well fits to the simulation results, obtained based on transistor level simulation using Mentor Graphics ELDO tool as presented in Fig. 3.

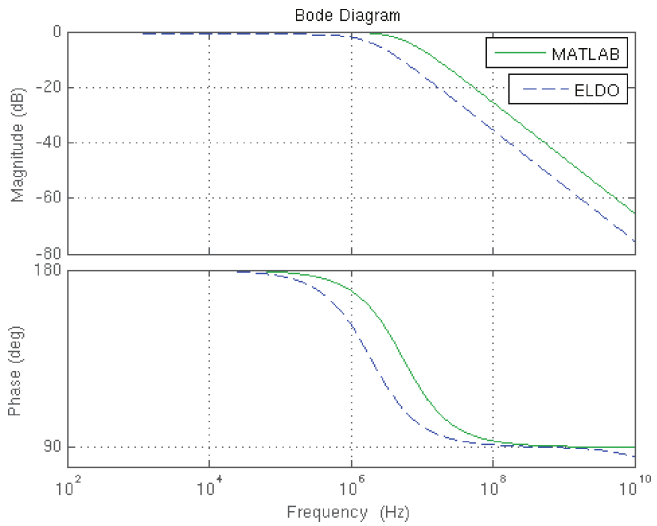

Fig. 3. Transfer function of the loop filter calculated based on the eq.(2) – MATLAB, and transistor level simulation – ELDO

2.2. Current comparator. The comparator is another important part of the design. This block is responsible for analog to digital conversion but at the same time, it introduces the quantization noise. In our design, a current mode comparator is required. Current comparator is widely used in many current mode applications such as A/D converters, oscillators, VLSI neural networks and other signal processing blocks. The simplest current comparator is just an inverter, composed of CMOS pair of transistors. The very sharp slope of its static characteristic, when the inverter is realized in CMOS technology, is a beneficial feature of such a cell working as comparator. Another, possible implementation of the current comparator, proposed by Freitas [7], was build based on two cascade current mirrors. A high output resistance of such AB class stage allows amplifying small differences in input currents to large variations in output voltage. Unfortunately, at the same time, the high impedance at the output node of this structure, reduces the frequency performance of the next CMOS block connected to the comparator. This drawback was improved by Träff in [8]. He proposed a source follower at the input stage of the comparator to reduce the impedance. The current comparator applied in this design is a structure composed of diode connected CMOS pair followed by inverters, which act as voltage amplifiers. This structure is presented in Fig. 4. To achieve a steeper transient characteristic, more output amplifiers (inverters) can be added.

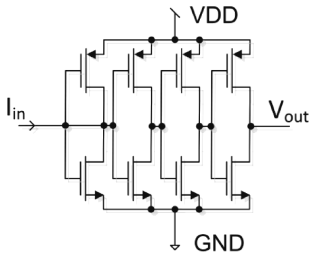

Fig. 4. Schematic diagram of the proposed comparator

To optimize the transistors sizes of the comparator for a given structure, an optimization program was implemented. This tool and achieved results are described in Sec. 3.

2.3. D/A current mode converter. To provide the required feedback in the SDM structure the D/A converter with current output was adopted. The structure of the circuit is presented in Fig. 5.

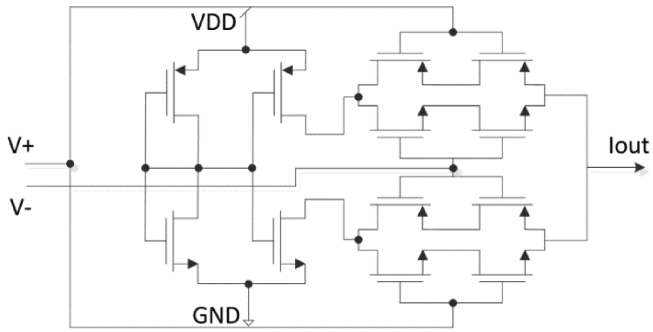

Fig. 5. Schematic diagram of the D/A current mode converter

The proper dimensions of the transistors give the required feedback current of the modulator.

3. Transistor sizing tool

Transistor sizing is an obligatory step in VLSI circuit design. Optimization of a circuit by transistor sizing is often a slow,

tedious and iterative manual process, which relies on the designer intuition. To automate this procedure EDA tool was developed, which was included also as part of bigger EDA tool [9]. The screenshot of the program is shown in Fig. 6.

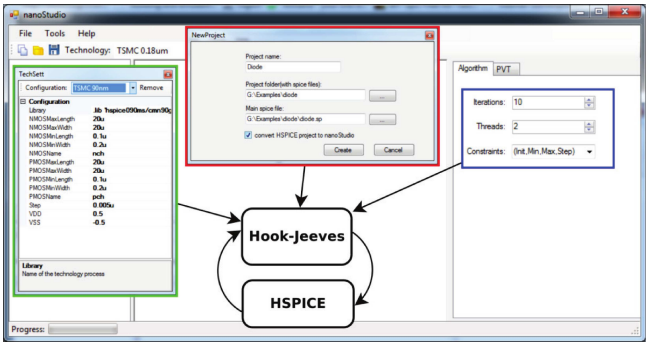

Fig. 6. Screenshot of the interface of the optimization program

The core of the program was prepared based on the Hooke-Jeeves pattern search method, which was originally published in 1961 in [10]. The optimal value of the objective function is obtained using two types of moves: exploratory search and pattern search. Exploratory search is a very local search that looks for an improving direction which to move. Pattern move is a larger search in the improving direction. Larger and larger moves are made as long as the improvement continues. As perturbation vector for the exploratory search, we take the width and length of transistors. The possible perturbation step size is chosen as a multiple of the smallest technology step. Once the exploratory search has found the optimal direction, the pattern move is applied in this direction.

The elaborated tool alters the transistor sizes for the processed cell. HSPICE circuit simulation is carried out in the inner loop of the optimization algorithm. After each step of the optimization, the HSPICE simulator is launched in order to provide the simulations results to calculate the objective function. In our example, the minimization of the delay time of the comparator is our goal. This value is obtained based on the transient analysis of the circuits. The circuit response, in a tabular form is transferred to the core of the optimization program.

The required input parameters of the program can be seen in the Fig. 6. Technology parameters (left window) can be introduced from the external file or directly from the keyboard. The SPICE netlist (central window) is included from external file. Additional data required by the algorithm such as constraints for optimized parameters, number of iterations and number of threads can be also set by designer. It is worth to mention that the program is prepared to be run in the multithreading mode. The optimization tool was implemented in C language.

The designed optimizer can use different optimization criteria. The comparator optimization was defined to minimize the delay time. The goal function was defined as mean squared error. The error was determined by the difference between the response times defined as the time interval between the time when input current crosses zero and time when output voltage reaches 50% of its value. This definition for rise and fall time is presented in Fig. 7. The waveform presents the transient response of the comparator after optimization.

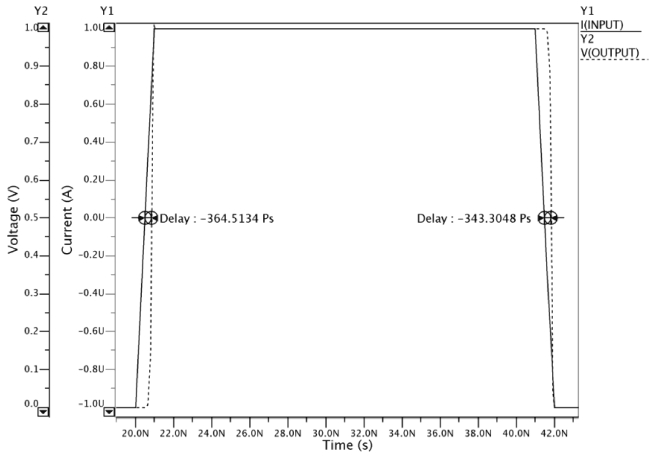

Fig. 7. Transient response of the proposed comparator (3 inverters)

4. Modulator simulation results

A Simulation test bench was prepared to check the performance of the designed circuit. A MATLAB script was used to calculate the input signal frequency according to coherent sampling requirements. Next, the proper, long enough, time of transient simulation was set to collect samples of the response signal. Based on 2^{14} points FFT was applied using Blackman window. The calculated output spectrum is presented in Fig. 8. Simulation results were aggregate into the Walden's Figure of Merit (FoM). It relates the SDM power dissipation to its performance, represented by sampling rate and conversion error amplitude in the form shown in equation

$$FoM = \frac{POWER}{2 \cdot BW \cdot 2^{ENOB}}. \tag{3}$$

For 250 MHz sampling clock frequency, we achieved 53.6 dB SNDR with power consumption equal to 93 μW. The Figure of Merit coefficient is equal to 59.7 fJ/step.

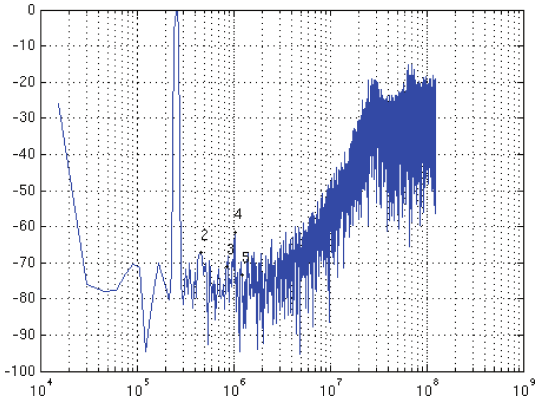

Fig. 8. Output spectrum calculated based on the post-layout simulation of presented $\sum\Delta$ modulator (2^{14} point FFT using Blackman window)

5. Conclusions

This work presents a new structure of a current mode sigma-delta modulator. The prototype circuit was design for TSMC 65 nm CMOS Process Technology. To optimize the transistor sizes for a given technology a computer tool was prepared. The program adopted a Hooke-Jeeves algorithm, which collaborates with HSPICE simulator. This tool was used to optimize the comparator performance. The achieved results are competitive with existing as presented in Table 1. Figure of Merit is equal to 59.665 fJ/step. The layout of the prototype chip is preparing to be ready for the next available manufacturing run and is presented in Fig. 9.

Table 1
Designed modulator performance comparison with other works

	This work	[11]	[12]	[13]
Technology [nm]	65	180	250	130
Supply Voltage [V]	1.2	1.8	1.5	1.2
Clock Frequency [MHz]	250	128	150	200
Signal Bandwidth [MHz]	2	2	2	1
Power [mW]	0.093	11	2.7	0.095
Peak SNDR [dB]	53.6	68	63.4	52.8
FoM [fJ/step]	59.7	1340	560	133

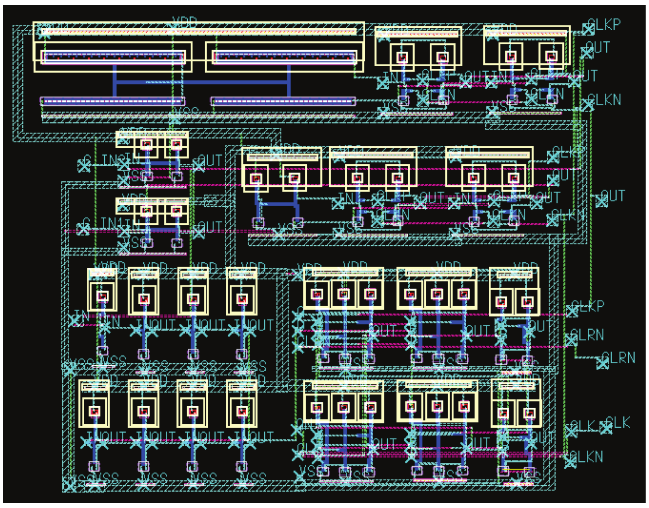

Fig. 9. Layout of the designed $\sum \Delta$ modulator

REFERENCES

[1] R. Suszyński and K. Wawryn, "Rapid prototyping of algorithmic A/D converters based on FPAA devices", *Bull. Pol. Ac.: Tech.* 61 (3), 691–696 (2013).

[2] K. Wawryn and R. Suszyński, "Low power 9-bit pipelined A/D and 8-bit self-calibrated D/A converters for a DSP system", *Bull. Pol. Ac.: Tech.* 61 (4), 979–988 (2013).

[3] J.R. Custodio, J. Goes, N. Paulino, J.P. Oliveira, and E. Bruun, "A 1.2-V 165-/spl mu/W 0.29-mm2 multibit sigma-delta ADC for hearing aids using nonlinear DACs and with over 91 dB dynamic-range", *Biomedical Circuits and Systems, IEEE Trans.* 7 (3), 376–385 (2013).

[4] J. Nakamura, B. Pain, T. Nomoto, T. Nakamura, and E.R. Fossum, "On-focal-plane signal processing for current-mode active pixel sensors", *IEEE Trans. Electron Devices* 44, 1747–1758 (1997).

[5] S.L. Smith and E. Sanchez-Sinencio, "Low voltage integrators for high-frequency CMOS filters using current mode techniques", *IEEE Trans. Circuits and Systems-II: Analog and Digital Signal Processing* 43, 39–48 (1996).

[6] R. Zele and D. Allstot, "Low-power cmos continuous-time filters", *IEEE J. Solid-State Circuits* 31, 157–158 (1996).

[7] D. Freitas and K. Current, "CMOS current comparator circuit", *Electronics Letters* 17, 695–697 (1983).

[8] H. Träff, "Novel approach to high speed CMOS current comparators", *Electronics Letters* 28, 310–312 (1992).

[9] M. Naumowicz, M. Melosik, P. Katarzynski, and A. Handkiewicz, "Automation of CMOS technology migration illustrated by RGB to YCrCb", *Opto-Electro. Rev.* 21, 326–331 (2013).

[10] R. Hooke and T. Jeeves, "Direct search solutions of numerical and statistical problems", *J. Association for Computing Machinery* 8, 212–229 (1961).

[11] Y. Aiba, K. Tomioka, Y. Nakashima, K. Hamashita, and B.-S. Song, "A fifth-order G m-C continuous-time $\Delta\Sigma$ modulator with process-insensitive input linear range", *Solid-State Circuits, IEEE J.* 44, 2381–2391 (2009).

[12] T. Song, Z. Cao, and S. Yan, "A 2.7-mW 2-MHz continuous-time $\Delta\Sigma$ modulator with a hybrid active-passive loop filter", *IEEE J. Solid-State Circuits* 43, 330–341 (2008).

[13] J.L.A. de Melo, "A low power 1-MHz continuous-time $\Delta\Sigma$M using a passive loop filter designed with a genetic algorithm tool", *Proc. IEEE Int. Symp. Circuits Systems* ISCAS'13, 586–589 (2013).