REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

REV																						
SHEET	45	46	47	48	49	50	51															
REV																						
SHEET	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
REV																						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
22-04-18

REVISION LEVEL

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, PROCESSOR, DIGITAL, CMOS, RADIATION HARDENED, QUAD CORE LEON4 SPARC V8 PROCESSOR, MONOLITHIC SILICON

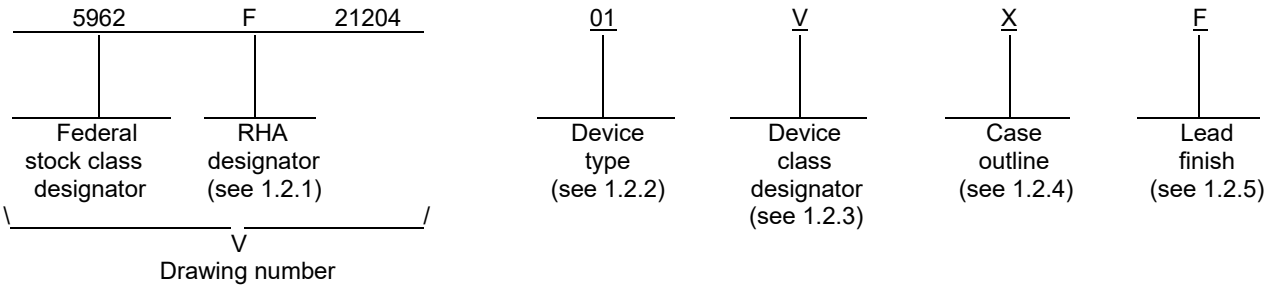
SIZE	CAGE CODE	
A	**67268**	**5962-21204**

SHEET 1 OF 51

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	GR740	Quad Core LEON4 SPARC V8 Processor

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style	
X	See figure 1a	625	Ceramic Column Grid Array (CCGA)	1/
Z	See figure 1b	625	Ceramic Land Grid Array (CLGA)	2/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Terminal lead finish F is tin lead alloy. Package case outline X solder columns material is Sn = 10% and Pb = 90%. Column Attach is Sn/Pb with Palladium doped alloy paste (Sn/Pb/Pd).
2/ The lead finish designator for case outline Z is C (gold plate).

1.3 Absolute maximum ratings. 3/ 4/

DC core supply voltage (VDD1V2) relative to GND	-0.3 V to 1.8 V
DC Analog PLL supply voltage (AVDDPLL1V2_MEMPLL) relative to AGNDPLL1V2_MEMPLL	-0.3 V to 1.8 V
DC Analog PLL supply voltage (AVDDPLL1V2_SPWPLL) relative to AGNDPLL1V2_SPWPLL	-0.3 V to 1.8 V
DC Analog PLL supply voltage (AVDDPLL1V2_SYSPLL) relative to AGNDPLL1V2_SYSPLL	-0.3 V to 1.8 V
DC Digital PLL supply voltage (DVDDPLL1V2_MEMPLL) relative to GND	-0.3 V to 1.8 V
DC Digital PLL supply voltage (DVDDPLL1V2_SPWPLL) relative to GND	-0.3 V to 1.8 V
DC Digital PLL supply voltage (DVDDPLL1V2_SYSPLL) relative to GND	-0.3 V to 1.8 V
DC 3V3 I/O supply voltage (VDIG3V3) relative to VSS3V3	-0.3 V to 4.5 V
DC 2V5 I/O supply voltage (VDIG2V5) relative to VSS2V5	-0.3 V to 4.5 V
LVDS signals relative to VSS2V5	-0.5 V to +4.5 V 5/
LVDS input signals relative to its complementary input	-0.8 V to +0.8 V 6/
LVCMOS signal relative to VSS3V3	-0.5 V to +4.5 V 7/
LVCMOS signal relative to VDIG3V3	-4.5 V to +0.3 V 7/
Storage temperature range (T_{STG})	-55°C to +150°C
Maximum junction temperature (T_J)	+150°C 8/
Thermal resistance, junction-to-case (θ_{JC}): 9/	
Case outline X	4.5°C/W 10/
Case outlines Z	1.4°C/W 11/
ESD rating:	
Human Body Model (HBM) ESD level	2000 V
Charge Device Model (CDM) ESD level	500 V

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Functional operation under these conditions is not implied.
4/ The absolute maximum current on any I/O shall be less than 100 mA for a duration of less than 10 ms, in the operating temperature.
5/ AMR signal voltage is valid for LVDS receivers. For LVDS drivers, AMR is covered by the I-Test conditions of the JESD78 specifications (see note 4/). AMR signal voltage is valid for both LVDS receivers and drivers in the cold sparing state (all supplies equal to 0 V).
6/ Exceeding differential voltage levels may cause over current stress to the on-chip termination resistors.
7/ Signal voltage levels must comply relative to both VSS3V3 and VDIG3V3, except for cold sparing state (all supplies equal to 0 V, see section 1.4.1 where signal voltage levels must comply relative to VSS3V3 only). AMR signal voltage is valid for ios configured in input mode. For ios configured in output mode, AMR is covered by the I-Test conditions of the JESD78 specifications (see note 4/). AMR signal voltage is valid for both ios configured in input and output modes in cold sparing state.
8/ AMR T_J corresponds to the maximum junction temperature applied for a duration of one hour, with biasing conditions as per the recommended operating range, without leading to instantaneous or very short term unrecoverable hard failure.
9/ All thermal resistance data are obtained through simulation.
10/ θ_{JC} for case outline X refers to the thermal resistance between the junction and the bottom of the columns.
11/ θ_{JC} for case outlines Z refers to the thermal resistance between the junction and the bottom of the package.

1.4 Recommended operating conditions.

Digital core supply voltage (VDD1V2)	1.1 V to 1.3 V 12/
I/O bank supply (VDIG2V5)	2.3 V to 2.7 V 12/
I/O bank supply (VDIG3V3)	3.0 V to 3.6 V 12/
Analog PLL supplies ($V_{AVDDPLL1V2\_MEMPLL}$, $V_{AVDDPLL1V2\_SPWPLL}$ & $V_{AVDDPLL1V2\_SYSPLL}$)	1.1 V to 1.3 V 12/
Digital PLL supplies ($V_{DVDDPLL1V2\_MEMPLL}$, $V_{DVDDPLL1V2\_SPWPLL}$ & $V_{DVDDPLL1V2\_SYSPLL}$)	1.1 V to 1.3 V 13/
High (logic 1) level input switching voltage [LVCMOS] (V_{IH})	2.0 V to 3.6 V 14/
Low (logic 0) level input switching voltage [LVCMOS] (V_{IL})	0.0 V to 0.7 V 14/ 15/
LVDS input common mode voltage ($V_{ICM,LVDS}$)	0.05 V to 2.35 V 16/
Absolute LVDS input differential ($\|V_{IDIFF,LVDS}\|$)	0.100 V to 0.600 V
LVDS output termination	80 Ω to 120 Ω
Operating junction temperature (T_J)	-40°C to +125 °C 17/

1.4.1 Cold Sparing State. 18/

Digital core supply voltage (VDD1V2)	0 V
I/O bank supply (VDIG2V5)	0 V 12/
I/O bank supply (VDIG3V3)	0 V 12/
Analog PLL supplies ($V_{AVDDPLL1V2\_MEMPLL}$, $V_{AVDDPLL1V2\_SPWPLL}$ & $V_{AVDDPLL1V2\_SYSPLL}$)	0 V 12/
Digital PLL supplies ($V_{DVDDPLL1V2\_MEMPLL}$, $V_{DVDDPLL1V2\_SPWPLL}$ & $V_{DVDDPLL1V2\_SYSPLL}$)	0 V 13/
I/O level, LVCMOS (V_{I_CE})	-0.3 V to 3.6 V
I/O level, LVDS pins ($V_{i\_LVDS\ ce}$)	0.0 V to 2.7 V
LVDS input differential ($V_{IDIFF,LVDS\ ce}$)	-0.600 V to +0.600 V

1.5 Radiation features.

Maximum total dose available: (dose rate up to = 0.21 rad (Si)/s)	300 krad (Si) 19/
Single event phenomenon (SEP):	
No SEL occurs at effective LET (see 4.4.4.2)	125 MeV.cm^2/mg 20/

12/ Relative to its corresponding grounds (GND, VSS2V5, VSS3V3, AGNDPLL1V2_MEMPLL, AGNDPLL1V2_SPWPLL and AGNDPLL1V2_SYSPLL). All grounds must be connected at the same DC potential.

13/ Relative to GND. On-chip grounds to Digital PLL supplies are connected to GND in the package.

14/ $V_{IH\ OVERSHOOT}$ = 300 mV and $V_{IL\ UNDERSHOOT}$ = -300 mV with a maximum duration of 3 ns beyond the recommended limits can be tolerated per transition. Alternatively, if DC levels (signals and supplies) are limited to 3.4V then $V_{IH\ OVERSHOOT}$ = 500 mV and $V_{IL\ UNDERSHOOT}$ = -500 mV with a maximum duration of 3 ns can be tolerated. The overshoot and undershoot allowances in this footnote have been determined from reliability simulations with the signal at the pin modeled as a 50 MHz square wave input, active 20% of the time, and with the device otherwise within the recommended operating conditions.

15/ With VDIG3V3 IO supply below 3.4V (VDIG3V3 relative to VSS3V3), minimum DC voltage down to -0.2V is permitted and with VDIG3V3 IO supply below 3.3V, minimum DC voltage down to -0.3V is permitted.

16/ Given range for LVDS input differential ($V_{IDIFF,LVDS}$) levels at +/- 100mV. LVDS input voltage of both LVDS inputs must be between 0.0V and 2.4V.

17/ Electrical testing is performed at T_{CASE} = -55ºC.

18/ While all supply rails to the device are powered down, normal I/O level voltages may be present on the device I/O pins without causing any inrush current into the device. The device will draw some minor leakage current (limited by I_{leak}). All outputs should be returned to undriven state in a device that has been acting as cold spare before starting the power-up sequence.

19/ The manufacturer's supplying this CMOS device is irradiated at a dose rate= 0.21 rad(Si)/s in accordance with MIL-STD-883, method 1019, condition B, and is guaranteed to a maximum total dose as specified. The dose rate condition B is the intended application, the parties to the test may agree to perform the test at a dose rate ≥ the maximum dose rate of the intended application.

20/ Heavy ion single event effects (SEE) test was performed at the Université Catholique de Louvain (UCL), in Louvain-la-Neuve, Belgium. No single event latch-up (SEL) was observed under Xenon heavy ion at an angle 60° with TCASE=85ºC, VVDD1V2=1.3V, VVDIG2V5=2.7V, VVDIG3V3=3.6V corresponding to an effective LET of 125 MeV·cm2/mg. For more information on SEP test results, customers are requested to contact the manufacturer

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD57 – Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy-Ion Irradiation.
JEP163 - Selection of Burn-In/Life Test Conditions and Critical Parameters for QML Microcircuits.

(Copies of these documents are available online at https:/www.jedec.org).

(Non-Government standards and other publications are normally available from the organizations that prepare of distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.1.1 Solderability test for case outline X. Solderability test for case outline X for CGA packages have been verified during the solder column attachment process in accordance with table 1 of test method 2003 of MIL-STD-883

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2

3.2.3 Block diagram. The block diagram shall be as specified on figure 3

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control.

3.2.5 Equivalent test conditions for LVCMOS outputs (1), LVCMOS inputs (2), LVDS outputs (3) and LVDS inputs (4). The Equivalent test conditions for LVCMOS outputs (1), LVCMOS inputs (2), LVDS outputs (3) and LVDS inputs (4) shall be as specified on figure 4.

3.2.6 Timing waveforms and test circuits: AC characteristics. The Timing waveforms and test circuits: AC characteristics shall be as specified on figure 5.

3.2.7 Timing waveforms: Phase-locked loop timings. The Timing waveforms: Phase-locked loop timings shall be as specified on figure 6.

3.2.8 Timing waveforms: Processor error mode signal timing. The Timing waveforms: Processor error mode signal timing shall be as specified on figure 7.

3.2.9 Timing waveforms and test circuits: 64-bit PC100 SDRAM Controller with Reed-Solomon EDAC timing. The Timing waveforms and test circuits: 64-bit PC100 SDRAM Controller with Reed-Solomon EDAC timing shall be as specified on figure 8.

3.2.10 Timing waveforms: DSU signals timing. The Timing waveforms: DSU signals timing shall be as specified on figure 9.

3.2.11 Timing waveforms: JTAG interface timing. The Timing waveforms: JTAG interface timing shall be as specified on figure10

3.2.12 Timing waveforms: Gigabit Ethernet Media Access Controller (MAC) w. EDCL timing. The Timing waveforms: Gigabit Ethernet Media Access Controller (MAC) w. EDCL timing shall be as specified on figure 11.

3.2.13 Timing waveforms: MDIO timing. The Timing waveforms: MDIO timing shall be as specified on figure 12

3.2.14 Timing waveforms: SpaceWire router interface timing. The Timing waveforms: SpaceWire router interface timing shall be as specified on figure 13.

3.2.15 Timing waveforms: SpaceWire debug interface timing. The Timing waveforms: SpaceWire debug interface timing shall be as specified on figure 14.

3.2.16 Timing waveforms: PCI interface timing. The Timing waveforms: PCI interface timing shall be as specified on figure 15.

3.2.17 Timing waveforms: MIL-STD-1553B / AS15531 interface timing. The Timing waveforms: MIL-STD-1553B / AS15531 interface timing shall be as specified on figure 16.

3.2.18 Timing waveforms: Fault-tolerant 8/16-bit PROM/IO memory interface timing (PROM accesses). The Timing waveforms: Fault-tolerant 8/16-bit PROM/IO memory interface timing (PROM accesses) shall be as specified on figure 17.

3.2.19 Timing waveforms: Fault-tolerant 8/16-bit PROM/IO memory interface timing (I/O accesses). The Timing waveforms: Fault-tolerant 8/16-bit PROM/IO memory interface timing (I/O accesses) shall be as specified on figure 18.

3.2.20 Timing waveforms: Watchdog signal timing. The Timing waveforms: Watchdog signal timing shall be as specified on figure 19.

3.2.21 Timing waveforms: General purpose I/O interface timing. The Timing waveforms: General purpose I/O interface timing shall be as specified on figure 20

3.2.22 Timing waveforms: UART interface timing. The Timing waveforms: UART interface timing shall be as specified on figure 21.

3.2.23 Timing waveforms: SPI controller timing. The Timing waveforms: SPI controller timing shall be as specified on figure 22.

3.2.24 Timing waveforms: CAN controller interface timing. The Timing waveforms: CAN controller interface timing shall be as specified on figure 23.

3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA and shall apply over the full junction operating temperature (T_J) range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.4.1 Solderability test for CLGA/CCGA packages: Solderability test for case outline X and Z for CCGA/CLGA package has been verified during solder column or ball attachment process in accordance with method 2003 of MIL-STD-883.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ as per section 1.4 unless otherwise specified	Group A Subgroups	Limits		Unit
				Min	Max	
Power Supply Operating Characteristics						
Static core supply current	I_{DD1V2S}	$T_C \leq +25°C$ V_{DD1V2S} = 1.3V, No clocking	1,3		20	mA
		$T_J \leq +125°C$ V_{DD1V2S} = 1.3V, No clocking	2		300	mA
Static I/O supply current V_{DIG2V5}	$I_{DIG2V5S}$	No clocking	1,2,3		300	mA
Static I/O supply current V_{DIG3V3}	$I_{DIG3V3S}$	No clocking	1,2,3		120	mA
Analog PLL supply current $V_{AVDDPLL1V2\_MEMPLL}$ and $V_{AVDDPLL1V2\_SPWPLL}$	$I_{AVDDPLL1V2\_MEMPLL}$ $I_{AVDDPLL1V2\_SPWPLL}$		4,5,6		8	mA
Analog PLL supply current, $V_{AVDDPLL1V2\_SYSPLL}$	$I_{AVDDPLL1V2\_SYSPLL}$		4,5,6		6	mA
Digital PLL supply current $V_{DVDDPLL1V2\_MEMPLL}$, $V_{DVDDPLL1V2\_SPWPLL}$, and $V_{DVDDPLL1V2\_SYSPLL}$	$I_{DVDDPLL1V2\_MEMPLL}$ $I_{DVDDPLL1V2\_SPWPLL}$ $I_{DVDDPLL1V2\_SYSPLL}$		4,5,6		10	mA
Input and output DC characteristics						
Input leakage current (LVCMOS)	I_{leak}		1,2,3	-10	10 5/	µA
Input capacitance (LVCMOS)	C_{in}	At package pin	1,2,3		10 4/	pF
Schmitt-trigger hysteresis for LVCMOS inputs	V_{hyst}		1,2,3	50 4/		mV
Pull-down current on DSU_EN and JTAG_TRST	I_{pd}	Input at 3.6V	1,2,3	50	400	µA
LVCMOS Output high voltage	V_{oh}	10mA load, default setting 2/	1,2,3	VDIG3V3-0.4	VDIG3V3	V
LVCMOS Output low voltage	V_{ol}	-10mA load, default setting 2/	1,2,3	0.0	0.5	V
LVDS input differential resistance 3/	$R_{I,LVDS}$		1,2,3	80	120	Ohm
LVDS input differential hysteresis	$V_{hyst,LVDS}$		1,2,3	25 4/		mV
LVDS output common mode voltage	$V_{OCM,LVDS}$		1,2,3	1.100	1.300	V
LVDS output difference	$V_{ODIFF,LVDS}$	100 Ω termination	1,2,3	0.250	0.450	V

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ as per section 1.4 unless otherwise specified	Group A Subgroups	Limits Min	Limits Max	Unit
DC characteristics under recommended operating conditions for cold-sparing state						
I/O leakage current (LVCMOS) in cold-spare	$I_{leak,LVCMOS,cs}$	7/	1,2,3	-10	10	µA
I/O leakage current (LVDS) in cold-spare	$I_{leak,LVDS,cs}$	Not counting current on inputs due to $R_{I,LVDS}$ 7/	1,2,3	-15	15	µA
LVDS input differential resistance 6/	$R_{I,LVDS,cs}$	7/	1,2,3	80	120	Ω
AC and functional Characteristics for Clock signals						
SYS_CLK frequency 12/	f_{sys_clk}	8/	7,8a,8b	20	70	MHz
SYS_CLK duty cycle 17/		8/	9,10,11	40	60	%
SPW_CLK frequency 12/	f_{spw_clk}	8/	7,8a,8b	20	55	MHz
SPW_CLK duty cycle 17/		8/	9,10,11	40	60	%
MEM_EXTCLK frequency 12/ 13/	f_{mem_extclk}	8/	7,8a,8b	20	55	MHz
MEM_EXTCLK duty cycle 17/		8/	9,10,11	40	60	%
SYS_CLK frequency 12/ 17/	$f_{sys\_clk\_bypass}$	9/	9,10,11	0	100	MHz
SYS_CLK duty cycle 17/		9/	9,10,11	20	80	%
SPW_CLK frequency 12/ 17/	$f_{spw\_clk\_bypass}$	9/	9,10,11	0	100	MHz
SPW_CLK duty cycle 17/		9/	9,10,11	40	60	%
MEM_EXTCLK frequency 12/ 13/ 17/	$f_{mem\_extclk\_bypass}$	9/	9,10,11	0	100	MHz
MEM_EXTCLK duty cycle 17/		9/	9,10,11	20	80	%
MEM_ CLK _IN frequency 18/	f_{mem_clk}	10/	7,8a,8b	0	100	MHz
MEM_CLK_IN duty cycle 17/		10/	9,10,11	20	80	%
PCI_CLK frequency 14/ 18/	$f_{pci\_clk\_ext}$	10/	7,8a,8b	33	33	MHz
PCI_CLK duty cycle 17/		10/	9,10,11	20	80	%
ETH*_GTXCLK frequency 18/	$f_{eth\_gtxclk\_ext}$	10/	7,8a,8b	125	125	MHz
ETH*_GTXCLK duty cycle 17/		10/	9,10,11	40	60	%
ETH*_TXCLK frequency 18/	$f_{eth\_txclk\_ext}$	10/	7,8a,8b	25	25	MHz
ETH*_TXCLK duty cycle 17/		10/	9,10,11	20	80	%
ETH*_RXCLK frequency 18/	$f_{eth\_rxclk\_ext}$	10/	7,8a,8b	25	125	MHz

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ as per section 1.4 unless otherwise specified	Group A Subgroups	Limits Min	Limits Max	Unit
AC and functional Characteristics for Clock signals – Continued.						
ETH*_RXCLK duty cycle 17/		10/	9,10,11	40	60	%
GR1553_CLK frequency 18/	$f_{gr1553\_clk\_ext}$	10/	7,8a,8b	19.999	20.001	MHz
GR1553_CLK duty cycle 17/		10/	9,10,11	20	80	%
GR1553_CLK jitter 17/ 19/		10/	9,10,11		5	ns
AMBA system clock frequency 15/ 16/	f_{soc_system}	11/	7,8a,8b	40 17/	250	MHz
Internal SPW clock frequency	$f_{internal\_spw\_clk}$	11/	9,10,11	10 17/	400	MHz
Phase-locked loop timings (Figure 6)						
PLL power-down duration 20/	t_{PLL0}		9,10,11	10000 21/		ns
PLL locking time	t_{PLL1}	rising *sys_resetn*	9,10,11		150000	ns
Processor error mode timing (Figure 7)						
Processor error mode Clock to output tri-state delay	t_{LEON4_0}	rising *clk* edge	9,10,11	0 22/	30 23/	ns
64-bit PC100 SDRAM Controller with Reed-Solomon EDAC timing (Figure 4,5 & 8)						
SDRAM Clock to output delay	t_{SDRAM0}		9,10,11	2.5	12.0	ns
SDRAM Clock to data output delay	t_{SDRAM1}		9,10,11	2.5	12.0	ns
SDRAM Data clock to data tri-state delay	t_{SDRAM2}		9,10,11	0 22/	30.0 24/	ns
SDRAM Data input to clock setup	t_{SDRAM3}		9,10,11	2.3		ns
SDRAM Data input from clock hold	t_{SDRAM4}		9,10,11	1.8		ns
DSU signals timing (Figure 9)						
DSU Clock to output delay	t_{DSU0}	rising *clk* edge	9,10,11	0 22/	30 24/	ns
DSU Input to clock hold	t_{DSU1}	rising *clk* edge	9,10,11	25/	25/	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ as per section 1.4 unless otherwise specified	Group A Subgroups	Limits		Unit
				Min	Max	
JTAG interface timing (Figure 10)						
JTAG Clock period	$t_{AHBJTAG0}$		9,10,11	50 22/		ns
JTAG Clock low/high period	$t_{AHBJTAG1}$		9,10,11	25 22/		ns
JTAG Data input to clock setup	$t_{AHBJTAG2}$	rising *jtag_tck* edge	9,10,11	10 22/		ns
JTAG Data input from clock hold	$t_{AHBJTAG3}$	rising *jtag_tck* edge	9,10,11	10 22/		ns
JTAG Clock to data output delay	$t_{AHBJTAG4}$	falling *jtag_tck* edge	9,10,11	0 22/	15 23/	ns
Gigabit Ethernet Media Access Controller (MAC) w. EDCL timing (Figure 4, 5 & 11)						
Ethernet MII transmit clock (ETH*_TXCLK) period	$t_{ETHTXCLK0}$		9,10,11	40 22/		ns
Ethernet MII receive clock (ETH*_RXCLK) period 26/	$t_{ETHRXCLK0}$		9,10,11	40 22/		ns
Ethernet GMII transmit clock (ETH*_GTXCLK) period	$t_{ETHGTXCLK0}$		9,10,11	8 22/		ns
Ethernet GMII receive clock period (ETH*_RXCLK) 26/	$t_{ETHRXCLK1}$		9,10,11	8 22/		ns
Ethernet transmitter clock to output delay	$t_{ETH0MII}$	rising (MII) clock edge	9,10,11	0 22/	15 23/	ns
Ethernet transmitter clock to output delay	$t_{ETH0GMII}$	rising (GMII) clock edge	9,10,11	1.5	10.5	ns
Ethernet input to receiver clock hold, ETH0 27/	$t_{ETH1MII/GMII\_ETH0}$	rising RX clock edge	9,10,11	0.5		ns
Ethernet input to receiver clock setup, ETH0 27/	$t_{ETH2MII/GMII\_ETH0}$	rising RX clock edge	9,10,11	1.5		ns
Ethernet input to receiver clock hold, ETH1 27/	$t_{ETH1MII/GMII\_ETH1}$	rising RX clock edge	9,10,11	0.3		ns
Ethernet input to receiver clock setup, ETH1 27/	$t_{ETH2MII/GMII\_ETH1}$	rising RX clock edge	9,10,11	2.6		ns
MDIO timing (Figure 12)						
MDIO clock-to-output delay	t_{MDIO0}	rising clock edge where ETH0_MDC rises	9,10,11	4 22/	4 22/	T_{clk}
MDIO input sampling point	t_{MDIO1}	rising clock edge where ETH0_MDC falls	9,10,11	1 22/	1 22/	T_{clk}

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ as per section 1.4 unless otherwise specified	Group A Subgroups	Limits Min	Limits Max	Unit
SpaceWire router interface timing (Figure 4, 5 & 13) 28/						
SpaceWire Transmit clock period	t_{SPW0}		9,10,11	1 / $f_{internal\_spw\_clk}$(max)	1 / $f_{internal\_spw\_clk}$(min)	ns
SpaceWire Clock to output delay	t_{SPW1}		9,10,11	29/	29/	
SpaceWire Input to clock hold	t_{SPW2}		9,10,11	29/	29/	
SpaceWire Input to clock setup	t_{SPW3}		9,10,11	29/	29/	
SpaceWire Output data bit period	t_{SPW4}		9,10,11	2.5 30/		ns
SpaceWire Input data bit period	t_{SPW5}		9,10,11	2.5 30/		ns
SpaceWire Data & strobe input edge separation	t_{SPW6}		9,10,11	2.5 30/ 31/		ns
SpaceWire Data & strobe output skew	t_{SPW7}		9,10,11	-0.3 31/	0.3 31/	ns
SpaceWire debug interface timing (Figure 14)						
SpaceWire debug Transmit clock period	t_{SPW0}		9,10,11	1 / $f_{internal\_spw\_clk}$(max)	1 / $f_{internal\_spw\_clk}$(min)	ns
SpaceWire debug Clock to output delay	t_{SPWD1}		9,10,11	29/	29/	
SpaceWire debug Input to clock hold	t_{SPWD2}		9,10,11	29/	29/	
SpaceWire debug Input to clock setup	t_{SPWD3}		9,10,11	29/	29/	
SpaceWire debug Output data bit period	t_{SPWD4}		9,10,11	20 23/ 30/		ns
SpaceWire debug Input data bit period	t_{SPWD5}		9,10,11	20 23/ 30/		ns
SpaceWire debug Data & strobe edge separation	t_{SPWD6}		9,10,11	10 23/ 30/		ns
SpaceWire debug Data & strobe output skew	t_{SPWD7}		9,10,11	-5 23/	5 23/	ns
PCI interface timing (Figure 4,5 & 15)						
PCI clock period 32/	$t_{PCICLK0}$		9,10,11	15 22/	30	ns
PCI clock to output delay	t_{PCI0}	rising PCI_CLK edge	9,10,11	2.5	14.5	ns
PCI input to clock hold	t_{PCI1}	rising PCI_CLK edge	9,10,11	2.3		ns
PCI input to clock setup	t_{PCI2}	rising PCI_CLK edge	9,10,11	4.8		ns
PCI clock to output delay	t_{PCI3}	rising PCI_CLK edge	9,10,11	2.5	14.5	ns
PCI input to clock hold	t_{PCI4}	rising PCI_CLK edge	9,10,11	2.3		ns
PCI input to clock setup	t_{PCI5}	rising PCI_CLK edge	9,10,11	4.8		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ as per section 1.4 unless otherwise specified	Group A Subgroups	Limits		Unit
				Min	Max	
MIL-STD-1553B / AS15531 interface timing (Figure 16)						
MIL-STD-1553B/AS15531 clock to data output delay	$t_{1553BRM0}$	rising GR1553_CLK edge	9,10,11	0 22/	40 23/	ns
MIL-STD-1553B/AS15531 data input to clock setup	$t_{1553BRM1}$	rising GR1553_CLK edge	9,10,11	33/	33/	ns
MIL-STD-1553B/AS15531 data input from clock hold	$t_{1553BRM2}$	rising GR1553_CLK edge	9,10,11	33/	33/	ns
Fault-tolerant 8/16-bit PROM/IO memory interface timing (Figure 17 (PROM accesses) & Figure 18 (I/O accesses))						
PROM and I/O accesses address clock to output delay	$t_{FTMCTRL0}$	rising clock edge 34/	9,10,11	0 22/	25 23/	ns
PROM and I/O accesses clock to output delay	$t_{FTMCTRL1}$	rising clock edge 34/	9,10,11	0 22/	25 23/	ns
PROM and I/O accesses clock to output delay	$t_{FTMCTRL2}$	rising clock edge 34/	9,10,11	0 22/	25 23/	ns
PROM and I/O accesses clock to data output delay	$t_{FTMCTRL3}$	rising clock edge 34/	9,10,11	0 22/	25 23/	ns
PROM and I/O accesses clock to data non-tri-state delay	$t_{FTMCTRL4}$	rising clock edge 34/	9,10,11	0 22/	25 23/	ns
PROM and I/O accesses clock to data tri-state delay	$t_{FTMCTRL5}$	rising clock edge 34/	9,10,11	0 22/	25 23/	ns
PROM and I/O accesses clock to output delay	$t_{FTMCTRL6}$	rising clock edge 34/	9,10,11	0 22/	25 23/	ns
PROM and I/O accesses data input to clock setup	$t_{FTMCTRL7}$	rising clock edge 34/ 35/	9,10,11	5 23/		ns
PROM and I/O accesses data input from clock hold	$t_{FTMCTRL8}$	rising clock edge 34/ 35/	9,10,11	5 23/		ns
PROM and I/O accesses input to clock setup	$t_{FTMCTRL9}$	rising clock edge 34/ 35/	9,10,11	5 23/		ns
PROM and I/O accesses input from clock hold	$t_{FTMCTRL10}$	rising clock edge 34/ 35/	9,10,11	5 23/		ns
Watchdog signal timing (Figure 19)						
Watchdog signal clock to output tri-state	$t_{GPTIMER0}$	rising clock edge	9,10,11	0 22/	40 23/	ns
Watchdog signal clock to output delay	$t_{GPTIMER1}$	rising clock edge	9,10,11	0 22/	40 23/	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ as per section 1.4 unless otherwise specified	Group A Subgroups	Limits		Unit
				Min	Max	
General purpose I/O interface timing (Figure 20)						
General purpose I/O clock to output delay	$t_{GRGPIO0}$	rising clock edge	9,10,11	0 22/	40 23/	ns
General purpose I/O clock to non-tri-state delay	$t_{GRGPIO1}$	rising clock edge	9,10,11	0 22/	40 23/	ns
General purpose I/O clock to tri-state delay	$t_{GRGPIO2}$	rising clock edge	9,10,11	0 22/	40 23/	ns
General purpose I/O input to clock hold	$t_{GRGPIO3}$	rising clock edge 37/	9,10,11	5 23/		ns
General purpose I/O input to clock setup	$t_{GRGPIO4}$	rising clock edge 37/	9,10,11	10 23/		ns
UART interface timing (Figure 21)						
UART clock to output delay	$t_{APBUART0}$	rising clock edge	9,10,11	0 22/	40 23/	ns
UART input to clock hold	$t_{APBUART1}$	rising clock edge 38/	9,10,11	10 23/		ns
UART input to clock setup	$t_{APBUART2}$	rising clock edge 38/	9,10,11	10 23/		ns
SPI controller timing (Figure 22)						
SPI clock to output delay	$t_{SPICTRL0}$	rising clock edge	9,10,11	0 22/	20 23/	ns
SPI clock to non-tri-state delay	$t_{SPICTRL1}$	rising clock edge	9,10,11	0 22/	20 23/	ns
SPI clock to tri-state delay	$t_{SPICTRL2}$	rising clock edge	9,10,11	0 22/	20 23/	ns
SPI input to clock hold	$t_{SPICTRL3}$	rising clock edge 39/	9,10,11	5 23/		ns
SPI input to clock setup	$t_{SPICTRL4}$	rising clock edge 39/	9,10,11	5 23/		ns
CAN controller interface timing (Figure 23)						
CAN clock to output delay	t_{GRCAN0}	rising clock edge	9,10,11	0 22/	20 23/	ns
CAN data input to clock setup	t_{GRCAN1}	rising clock edge 40/	9,10,11	5 23/		ns
CAN data input from clock hold	t_{GRCAN2}	rising clock edge 40/	9,10,11	5 23/		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

1/ RHA parts for device type 01 supplied to this drawing have been characterized through all levels M, D, P, L, R and F of irradiation. However, this device is only tested at the 'F' level. Pre and Post irradiation values are identical unless otherwise specified in Table IIC. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.
2/ The outputs can be digitally reprogrammed to reduce the drive strength. In addition to testing at default full strength with a +/- 10 mA load, the outputs are also tested to the same limits at the minimum strength with a +/- 4 mA load.
3/ Internal termination is provided on all LVDS inputs.
4/ Guaranteed by design, not production tested.
5/ Does not apply for pins with pull-down where I_{PD} applies. Applies to single LVDS input pins when the opposite input of the differential LVDS inputs is non-connected (no current through differential resistor).
6/ Guaranteed by design, not production tested. Internal termination is provided on all LVDS inputs also when powered down.
7/ Conditions as per section 1.4.2.
8/ Externally fed PLL input clocks, PLLs enabled (in default configuration).
9/ Externally fed PLL input clocks, PLLs bypassed.
10/ Externally fed clocks, non-PLL.
11/ Internally generated clocks.
12/ Min/max values are maximum for on-chip PLL input, limits for the generated frequencies must also be satisfied. Nominal frequency required for correct operation with PLL power-up configuration and will change if reconfigured.
13/ Assuming MEM_CLKSEL has been set high so that MEM_EXTCLK is used.
14/ The PCI interface of this device is not compliant to the DC I/V characteristics and AC timings required by the PCI specification. The PCI interface can be functionally clocked at any frequency up to 66 MHz provided that board-level timing can be met.
15/ The minimum clock frequency for the on-chip system is determined by functional interface limitations and has not been fully characterized. A clock frequency over 40 MHz is required for the Ethernet interfaces to function at gigabit speeds.
16/ The maximum given here is from static timing analysis, and it is also used as clock rate during production tests.
17/ Supplied as design parameter, not tested.
18/ The PCI_CLK, ETH_GTXCLK, ETH_TXCLK, ETH_RXCLK, MEM_CLKIN and GR1553_CLK clock domains are production tested at nominal frequency using a clock generated internally with the on-chip PLLs. The external AC timing is production tested using the functional clock input but at reduced frequency.
19/ Limit on rising edge only.
20/ PLL is in power-down as long as SYS_RESETN is held low. Unused PLLs for selected configuration are permanently in power-down and their corresponding lock signals never go high.
21/ This parameter is not tested.
22/ This parameter is guaranteed by design, not production tested.
23/ This parameter is determined by static timing analysis and is not tested.
24/ This parameter is determined by characterization and is not tested.
25/ The BREAK and DSU_EN signals are re-synchronized internally. These signals do not have to meet any setup or hold requirements. As the DSU_EN signal controls clock gating for the Debug AHB bus the signal's value should be kept constant from power-up.
26/ ETH*_RXCLK is used in both MII and GMII mode, with different frequencies.
27/ Signals ETH*_COL, ETH*_CRS, ETH*_MDINT, ETH*_MDIO are resynchronized internally and do not have any setup/hold timing requirements.
28/ Internal SpaceWire clock generated from PLL or from SPW_CLK input.
29/ The inputs are asynchronous to the clock and are internally resynchronized to internal spw_clk. The outputs are synchronous to the internal spw_clk but its output delay is irrelevant for the SpaceWire protocol.
30/ Assuming SpaceWire PLL used in nominal configuration.
31/ Edge separation and skew limits refer to each pair of data/strobe signals separately. Global skew and separation over the entire set of eight pairs is not specified.
32/ The PCI interface can be internally clocked at any clock period in the supported range. Board signal timing must also be satisfied for the PCI interface to be functional.
33/ The inputs are asynchronous to the clock and are internally resynchronized to GR1553_CLK.
34/ Timing values are relative to the internal clock for the PROM/IO memory controller.
35/ Setup and hold relative to the clock edge on which the data is captured, which can be adjusted through wait states settings in the controller.

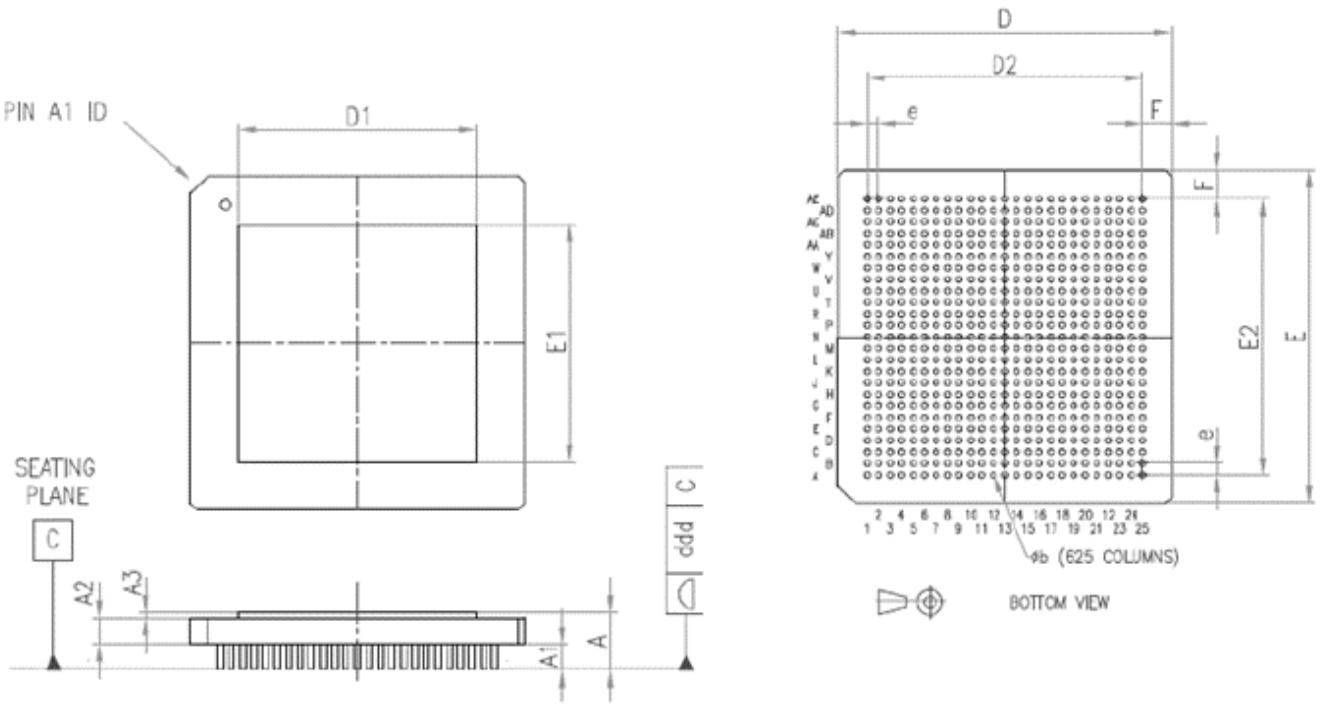
36/ In asynchronous bus ready mode, the BRDYN signal is internally synchronized and setup and hold constraints on BRDYN may be violated. The earliest time a transition is guaranteed to be captured is the internal clock edge where setup and hold are met.
37/ The general purpose I/O interface (GPIO) inputs are re-synchronized internally, therefore these signals may change asynchronously and do not have to meet any setup or hold requirements. The earliest time a transition is guaranteed to be captured is the internal clock edge where setup and hold are met.
38/ The UART*_CSTN and UART*_RXD inputs are re-synchronized internally. Therefore, these signals may change asynchronously and do not have to meet any setup or hold requirements. However, the earliest time a signal transition is guaranteed to be captured is the internal clock edge where setup and hold are met.
39/ The SPI_SCK, SPI_MISO, SPI_MOSI AND SPI_SPISEL inputs are re-synchronized internally, therefore these signals do not have to meet any setup or hold requirements. However, the earliest time a signal transition is guaranteed to be captured is the internal clock edge where setup and hold are met.
40/ The CAN inputs are re-synchronized internally therefore these signals do not have to meet any setup or hold requirements. However, the earliest time a signal transition is guaranteed to be captured is the internal clock edge where setup and hold are met.

Table IB. SEP test limits. 1/ 2/ 3/

Device type	SEP	Bias for Single event latch-up (SEL) test. V_{VDD1V2}=1.3V, $V_{VDIG2V5}$=2.7V, $V_{VDIG3V3}$=3.6V No SEL occurs at effective linear energy transfer (LET)
All	No SEL	Effective LET ≤ 125 MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Heavy ion single event effects (SEE) test was performed at the Université Catholique de Louvain (UCL), in Louvain-la-Neuve, Belgium. No single event latch-up (SEL) was observed under Xenon heavy ion at an angle 60° with T_{CASE}=85ºC, V_{VDD1V2}=1.3V, $V_{VDIG2V5}$=2.7V, $V_{VDIG3V3}$=3.6V corresponding to an effective LET of 125 MeV·cm^2/mg. For more information on SEP test results, customers are requested to contact the manufacturer.

Case X



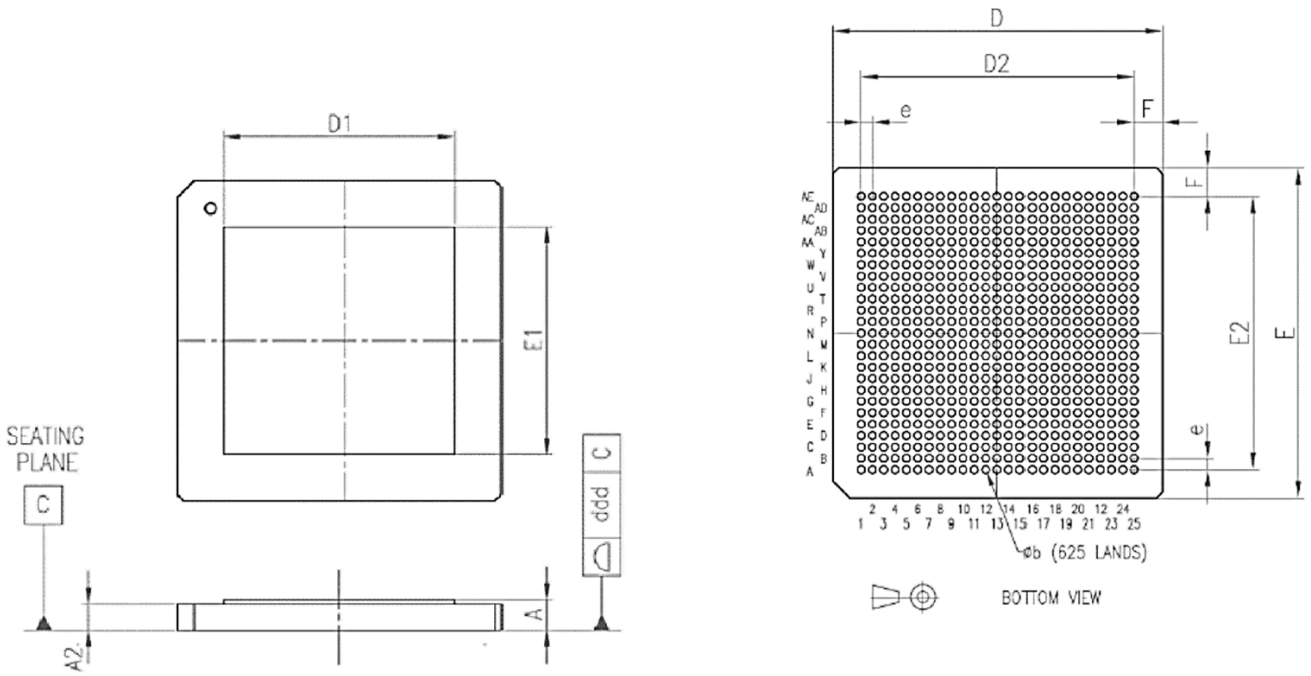
Dimensions									
Symbol	Millimeters				Symbol	Millimeters			
	Min	Typ	Max	Notes		Min	Typ	Max	Notes
A	4.77	5.12	5.47	1/	D2	23.90	24.00	24.10	
A1	2.16	2.24	2.31	2/	E	28.85	29.00	29.15	
A2	2.25	2.50	2.75		E1	20.40	20.47	20.55	
A3	0.36	0.38	0.41	3/	E2	23.90	24.00	24.10	
b	0.48	0.51	0.52		e	0.92	1.00	1.08	
D	28.85	29.00	29.15		F		2.5		
D1	20.40	20.47	20.55		ddd			0.08	

Notes:

1. The total profile height (Dim.A) MAX = A1 MAX + A2 MAX + A3 MAX. Same for A MIN and A TYP.
2. Column height.
3. Lid height (perform not included)

Figure 1a: Case outline X

Case Z



Dimensions									
Symbol	Millimeters				Symbol	Millimeters			
	Min	Typ	Max	Notes		Min	Typ	Max	Notes
A	2.61	2.88	3.16	1/	E	28.85	29.00	29.15	
A2	2.25	2.50	2.75		E1	20.39	20.47	20.55	
B	0.70	0.75	0.80		E2	23.90	24.00	24.10	
D	28.85	29.00	29.15		E	0.92	1.00	1.08	
D1	20.40	20.47	20.55		F	2.37	2.5	2.62	
D2	23.90	24.00	24.10						

Notes:

1. The total profile height (Dim.A) TYP is measured with = A2 TYP + lid height TYP without the preform. Same method for A MAX and A MIN.

Figure 1b: Case outline Z – Continued

Position	Signal Name	I/O	Level	Volt. [V]	Pull	Polarity	Note
A1	GND	Power/ground pin					GND
A2	GND	Power/ground pin					GND
A3	PROMIO_ADDR[6]	O	LVCMOS	3.3	-		PROM
A4	PROMIO_ADDR[2]	O	LVCMOS	3.3	-		PROM
A5	PROMIO_WEN	O	LVCMOS	3.3	-	Low	PROM
A6	PROMIO_DATA[14]	IO	LVCMOS	3.3	-		PROM
A7	PROMIO_DATA[10]	IO	LVCMOS	3.3	-		PROM
A8	PROMIO_DATA[6]	IO	LVCMOS	3.3	-		PROM
A9	PROMIO_DATA[2]	IO	LVCMOS	3.3	-		PROM
A10	GR1553_BUSATXIN	O	LVCMOS	3.3	-		MIL-1553
A11	SPI_MOSI	IO	LVCMOS	3.3	-		SPI
A12	SYS_CLK	I	LVCMOS	3.3	-		Sys/spw CLK
A13	MEM_EXTCLK	I	LVCMOS	3.3	-		Sys/spw CLK
A14	SYS_EXTLOCK	I	LVCMOS	3.3	-		Sys/spw CLK
A15	JTAG_TCK	I	LVCMOS	3.3	-		JTAG
A16	JTAG_TRST	I	LVCMOS	3.3	PullDown	Low	JTAG
A17	GPIO[14]	IO	LVCMOS	3.3	-		GPIO
A18	GPIO[12]	IO	LVCMOS	3.3	-		GPIO
A19	GPIO[8]	IO	LVCMOS	3.3	-		GPIO
A20	GPIO[4]	IO	LVCMOS	3.3	-		GPIO
A21	GPIO[0]	IO	LVCMOS	3.3	-		GPIO
A22	PLL_BYPASS[0]	I	LVCMOS	3.3	-	High	Bootstrap
A23	GND	Reserved for test, must be tied to ground					GND
A24	GND	Power/ground pin					GND
A25	GND	Power/ground pin					GND
B1	GND	Power/ground pin					GND
B2	PROMIO_ADDR[9]	O	LVCMOS	3.3	-		PROM
B3	PROMIO_ADDR[8]	O	LVCMOS	3.3	-		PROM
B4	PROMIO_ADDR[4]	O	LVCMOS	3.3	-		PROM
B5	PROMIO_ADDR[0]	O	LVCMOS	3.3	-		PROM
B6	PROMIO_READ	O	LVCMOS	3.3	-	High	PROM
B7	PROMIO_DATA[12]	IO	LVCMOS	3.3	-		PROM
B8	PROMIO_DATA[8]	IO	LVCMOS	3.3	-		PROM
B9	PROMIO_DATA[4]	IO	LVCMOS	3.3	-		PROM
B10	GR1553_CLK	I	LVCMOS	3.3	-		MIL-1553
B11	SPI_MISO	IO	LVCMOS	3.3	-		SPI
B12	SPW_CLK	I	LVCMOS	3.3	-		Sys/spw CLK
B13	SYS_RESETN	I	LVCMOS	3.3	-	Low	Sys/spw CLK
B14	JTAG_TMS	I	LVCMOS	3.3	-		JTAG

Figure 2: Terminal connections and pin descriptions

Position	Signal Name	I/O	Level	Volt. [V]	Pull	Polarity	Note
B15	JTAG_TDO	O	LVCMOS	3.3	-		JTAG
B16	JTAG_TDI	I	LVCMOS	3.3	-		JTAG
B17	GPIO[7]	IO	LVCMOS	3.3	-		GPIO
B18	GPIO[10]	IO	LVCMOS	3.3	-		GPIO
B19	GPIO[6]	IO	LVCMOS	3.3	-		GPIO
B20	GPIO[2]	IO	LVCMOS	3.3	-		GPIO
B21	PCIMODE_ENABLE	I	LVCMOS	3.3	-	High	Bootstrap
B22	PLL_BYPASS[1]	I	LVCMOS	3.3	-	High	Bootstrap
B23	PLL_IGNLOCK	I	LVCMOS	3.3	-	High	Bootstrap
B24	PLL_LOCKED[4]	O	LVCMOS	3.3	-	High	Bootstrap
B25	GND	Power/ground pin					GND
C1	PROMIO_ADDR[10]	O	LVCMOS	3.3	-		PROM
C2	PROMIO_ADDR[12]	O	LVCMOS	3.3	-		PROM
C3	PROMIO_ADDR[7]	O	LVCMOS	3.3	-		PROM
C4	PROMIO_ADDR[3]	O	LVCMOS	3.3	-		PROM
C5	PROMIO_OEN	O	LVCMOS	3.3	-	Low	PROM
C6	PROMIO_DATA[15]	IO	LVCMOS	3.3	-		PROM
C7	PROMIO_DATA[9]	IO	LVCMOS	3.3	-		PROM
C8	PROMIO_DATA[5]	IO	LVCMOS	3.3	-		PROM
C9	PROMIO_DATA[0]	IO	LVCMOS	3.3	-		PROM
C10	GR1553_BUSBTXIN	O	LVCMOS	3.3	-	High	MIL-1553
C11	SPI_SCK	IO	LVCMOS	3.3	-		SPI
C12	SPI_SEL	I	LVCMOS	3.3	-	Low	SPI
C13	SPI_SLVSEL[0]	O	LVCMOS	3.3	-	Low	SPI
C14	SPI_SLVSEL[1]	O	LVCMOS	3.3	-	Low	SPI
C15	GPIO[13]	IO	LVCMOS	3.3	-		GPIO
C16	GPIO[9]	IO	LVCMOS	3.3	-		GPIO
C17	GPIO[3]	IO	LVCMOS	3.3	-		GPIO
C18	GPIO[1]	IO	LVCMOS	3.3	-		GPIO
C19	DSU_ACTIVE	O	LVCMOS	3.3	-	High	Bootstrap
C20	MEM_IFWIDTH	I	LVCMOS	3.3	-		Bootstrap
C21	VSS2V5	Power/ground pin					VSS2V5
C22	VSS2V5	Power/ground pin					VSS2V5
C23	VSS2V5	Power/ground pin					VSS2V5
C24	VSS2V5	Power/ground pin					VSS2V5
C25	VSS2V5	Power/ground pin					VSS2V5
D1	PROMIO_ADDR[14]	O	LVCMOS	3.3	-		PROM
D2	PROMIO_ADDR[16]	IO	LVCMOS	3.3	-		PROM
D3	PROMIO_ADDR[11]	O	LVCMOS	3.3	-		PROM
D4	PROMIO_ADDR[5]	O	LVCMOS	3.3	-		PROM

Figure 2: Terminal connections and pin descriptions – Continued

Position	Signal Name	I/O	Level	Volt. [V]	Pull	Polarity	Note
D5	PROMIO_BRDYN	I	LVCMOS	3.3	-	Low	PROM
D6	PROMIO_DATA[13]	IO	LVCMOS	3.3	-		PROM
D7	PROMIO_DATA[11]	IO	LVCMOS	3.3	-		PROM
D8	PROMIO_DATA[3]	IO	LVCMOS	3.3	-		PROM
D9	VSS3V3	Power/ground pin					VSS3V3
D10	VDIG3V3	Power/ground pin					VDIG3V3
D11	VSS3V3	Power/ground pin					VSS3V3
D12	VDIG3V3	Power/ground pin					VDIG3V3
D13	VSS3V3	Power/ground pin					VSS3V3
D14	GPIO[15]	IO	LVCMOS	3.3	-		GPIO
D15	GPIO[11]	IO	LVCMOS	3.3	-		GPIO
D16	GPIO[5]	IO	LVCMOS	3.3	-		GPIO
D17	BREAK	I	LVCMOS	3.3	-	High	Bootstrap
D18	DSU_EN	I	LVCMOS	3.3	PullDown	High	Bootstrap
D19	WDOGN	O	LVCMOS	3.3	-	Low	Bootstrap, Open-drain
D20	PLL_LOCKED[2]	O	LVCMOS	3.3	-	High	Bootstrap
D21	VSS2V5	Power/ground pin					VSS2V5
D22	SPW_TXS_P[7]	O	LVDS	2.5	-	Pos	SpaceWire
D23	SPW_TXS_N[7]	O	LVDS	2.5	-	Neg	SpaceWire
D24	SPW_TXD_P[7]	O	LVDS	2.5	-	Pos	SpaceWire
D25	SPW_TXD_N[7]	O	LVDS	2.5	-	Neg	SpaceWire
E1	PROMIO_ADDR[18]	IO	LVCMOS	3.3	-		PROM
E2	PROMIO_ADDR[20]	IO	LVCMOS	3.3	-		PROM
E3	VDIG3V3	Power/ground pin					VDIG3V3
E4	PROMIO_ADDR[15]	O	LVCMOS	3.3	-		PROM
E5	PROMIO_ADDR[13]	O	LVCMOS	3.3	-		PROM
E6	PROMIO_ADDR[1]	O	LVCMOS	3.3	-		PROM
E7	PROMIO_DATA[7]	IO	LVCMOS	3.3	-		PROM
E8	PROMIO_DATA[1]	IO	LVCMOS	3.3	-		PROM
E9	VDIG3V3	Power/ground pin					VDIG3V3
E10	VSS3V3	Power/ground pin					VSS3V3
E11	VDIG3V3	Power/ground pin					VDIG3V3
E12	AGNDPLL1V2_SYSPLL	Power/ground pin					PLL
E13	AGNDPLL1V2_MEMPLL	Power/ground pin					PLL
E14	AGNDPLL1V2_SPWPLL	Power/ground pin					PLL
E15	PROC_ERRORN	O	LVCMOS	3.3	-	Low	Bootstrap, Open-drain
E16	MEM_CLKSEL	I	LVCMOS	3.3	-		Bootstrap
E17	PLL_BYPASS[2]	I	LVCMOS	3.3	-	High	Bootstrap
E18	PLL_LOCKED[5]	O	LVCMOS	3.3	-	High	Bootstrap

Figure 2: Terminal connections and pin descriptions – Continued

Position	Signal Name	I/O	Level	Volt. [V]	Pull	Polarity	Note
E19	PLL_LOCKED[3]	O	LVCMOS	3.3	-	High	Bootstrap
E20	PLL_LOCKED[0]	O	LVCMOS	3.3	-	High	Bootstrap
E21	VSS2V5	Power/ground pin					VSS2V5
E22	SPW_RXS_P[7]	I	LVDS	2.5	DiffTerm	Pos	SpaceWire
E23	SPW_RXS_N[7]	I	LVDS	2.5	DiffTerm	Neg	SpaceWire
E24	SPW_RXD_P[7]	I	LVDS	2.5	DiffTerm	Pos	SpaceWire
E25	SPW_RXD_N[7]	I	LVDS	2.5	DiffTerm	Neg	SpaceWire
F1	PROMIO_ADDR[22]	IO	LVCMOS	3.3	-		PROM
F2	PROMIO_ADDR[24]	IO	LVCMOS	3.3	-		PROM
F3	VSS3V3	Power/ground pin					VSS3V3
F4	PROMIO_ADDR[19]	IO	LVCMOS	3.3	-		PROM
F5	PROMIO_ADDR[17]	IO	LVCMOS	3.3	-		PROM
F6	VDIG3V3	Power/ground pin					VDIG3V3
F7	VSS3V3	Power/ground pin					VSS3V3
F8	VDIG3V3	Power/ground pin					VDIG3V3
F9	VSS3V3	Power/ground pin					VSS3V3
F10	VDIG3V3	Power/ground pin					VDIG3V3
F11	VSS3V3	Power/ground pin					VSS3V3
F12	AVDDPLL1V2_SYSPLL	Power/ground pin					PLL
F13	AVDDPLL1V2_MEMPLL	Power/ground pin					PLL
F14	AVDDPLL1V2_SPWPLL	Power/ground pin					PLL
F15	VSS3V3	Power/ground pin					VSS3V3
F16	VDIG3V3	Power/ground pin					VDIG3V3
F17	VSS3V3	Power/ground pin					VSS3V3
F18	VDIG3V3	Power/ground pin					VDIG3V3
F19	VSS3V3	Power/ground pin					VSS3V3
F20	PLL_LOCKED[1]	O	LVCMOS	3.3	-	High	Bootstrap
F21	VSS2V5	Power/ground pin					VSS2V5
F22	SPW_TXS_P[6]	O	LVDS	2.5	-	Pos	SpaceWire
F23	SPW_TXS_N[6]	O	LVDS	2.5	-	Neg	SpaceWire
F24	SPW_TXD_P[6]	O	LVDS	2.5	-	Pos	SpaceWire
F25	SPW_TXD_N[6]	O	LVDS	2.5	-	Neg	SpaceWire
G1	PROMIO_ADDR[26]	IO	LVCMOS	3.3	-		PROM
G2	IO_SN	IO	LVCMOS	3.3	-	Low	PROM
G3	VDIG3V3	Power/ground pin					VDIG3V3
G4	PROMIO_ADDR[23]	IO	LVCMOS	3.3	-		PROM
G5	PROMIO_ADDR[21]	IO	LVCMOS	3.3	-		PROM
G6	VSS3V3	Power/ground pin					VSS3V3
G7	VDIG3V3	Power/ground pin					VDIG3V3

Figure 2: Terminal connections and pin descriptions – Continued

Position	Signal Name	I/O	Level	Volt. [V]	Pull	Polarity	Note
~~G8~~	VSS3V3	Power/ground pin					VSS3V3
G9	VDIG3V3	Power/ground pin					VDIG3V3
G10	VSS3V3	Power/ground pin					VSS3V3
G11	VDIG3V3	Power/ground pin					VDIG3V3
G12	DVDDPLL1V2_SYSPLL	Power/ground pin					PLL
G13	DVDDPLL1V2_MEMPLL	Power/ground pin					PLL
G14	DVDDPLL1V2_SPWPLL	Power/ground pin					PLL
G15	VDIG3V3	Power/ground pin					VDIG3V3
G16	VSS3V3	Power/ground pin					VSS3V3
G17	VDIG3V3	Power/ground pin					VDIG3V3
G18	VSS3V3	Power/ground pin					VSS3V3
G19	VDIG3V3	Power/ground pin					VDIG3V3
G20	VSS3V3	Power/ground pin					VSS3V3
G21	VSS2V5	Power/ground pin					VSS2V5
G22	SPW_RXS_P[6]	I	LVDS	2.5	DiffTerm	Pos	SpaceWire
G23	SPW_RXS_N[6]	I	LVDS	2.5	DiffTerm	Neg	SpaceWire
G24	SPW_RXD_P[6]	I	LVDS	2.5	DiffTerm	Pos	SpaceWire
G25	SPW_RXD_N[6]	I	LVDS	2.5	DiffTerm	Neg	SpaceWire
H1	PROM_CEN[1]	IO	LVCMOS	3.3	-	Low	PROM
H2	PROM_CEN[0]	O	LVCMOS	3.3	-	Low	PROM
H4	PROMIO_ADDR[27]	IO	LVCMOS	3.3	-		PROM
H5	PROMIO_ADDR[25]	IO	LVCMOS	3.3	-		PROM
H6	VDIG3V3	Power/ground pin					VDIG3V3
H7	VSS3V3	Power/ground pin					VSS3V3
H8	VDD1V2	Power/ground pin					VDD
H9	GND	Power/ground pin					GND
H10	VDD1V2	Power/ground pin					VDD
H11	GND	Power/ground pin					GND
H12	VDD1V2	Power/ground pin					VDD
H13	GND	Power/ground pin					GND
H14	VDD1V2	Power/ground pin					VDD
H15	GND	Power/ground pin					GND
H16	VDD1V2	Power/ground pin					VDD
H17	GND	Power/ground pin					GND
H18	VDD1V2	Power/ground pin					VDD
H19	VSS3V3	Power/ground pin					VSS3V3
H20	VDIG3V3	Power/ground pin					VDIG3V3
H21	VSS2V5	Power/ground pin					VSS2V5

Figure 2: Terminal connections and pin descriptions – Continued

Position	Signal Name	I/O	Level	Volt. [V]	Pull	Polarity	Note
H22	SPW_TXS_P[5]	O	LVDS	2.5	-	Pos	SpaceWire
H23	SPW_TXS_N[5]	O	LVDS	2.5	-	Neg	SpaceWire
H24	SPW_TXD_P[5]	O	LVDS	2.5	-	Pos	SpaceWire
H25	SPW_TXD_N[5]	O	LVDS	2.5	-	Neg	SpaceWire
J1	ETH0_MDC	O	LVCMOS	3.3	-		Ethernet
J2	ETH0_RXCLK	I	LVCMOS	3.3	-		Ethernet
J3	VDIG3V3	Power/ground pin					VDIG3V3
J4	ETH0_MDINT	I	LVCMOS	3.3	-	Low	Ethernet
J5	ETH0_CRS	I	LVCMOS	3.3	-	High	Ethernet
J6	VSS3V3	Power/ground pin					VSS3V3
J7	VDIG3V3	Power/ground pin					VDIG3V3
J8	GND	Power/ground pin					GND
J9	VDD1V2	Power/ground pin					VDD
J10	GND	Power/ground pin					GND
J11	VDD1V2	Power/ground pin					VDD
J12	GND	Power/ground pin					GND
J13	VDD1V2	Power/ground pin					VDD
J14	GND	Power/ground pin					GND
J15	VDD1V2	Power/ground pin					VDD
J16	GND	Power/ground pin					GND
J17	VDD1V2	Power/ground pin					VDD
J18	GND	Power/ground pin					GND
J19	VDIG3V3	Power/ground pin					VDIG3V3
J20	VSS3V3	Power/ground pin					VSS3V3
J21	VDIG2V5	Power/ground pin					VDIG2V5
J22	SPW_RXS_P[5]	I	LVDS	2.5	DiffTerm	Pos	SpaceWire
J23	SPW_RXS_N[5]	I	LVDS	2.5	DiffTerm	Neg	SpaceWire
J24	SPW_RXD_P[5]	I	LVDS	2.5	DiffTerm	Pos	SpaceWire
J25	SPW_RXD_N[5]	I	LVDS	2.5	DiffTerm	Neg	SpaceWire
K1	ETH0_RXD[0]	I	LVCMOS	3.3	-		Ethernet
K2	ETH0_RXD[2]	I	LVCMOS	3.3	-		Ethernet
K3	VSS3V3	Power/ground pin					VSS3V3
K4	ETH0_MDIO	IO	LVCMOS	3.3	-		Ethernet
K5	ETH0_COL	I	LVCMOS	3.3	-	High	Ethernet
K6	VDIG3V3	Power/ground pin					VDIG3V3
K7	VSS3V3	Power/ground pin					VSS3V3
K8	VDD1V2	Power/ground pin					VDD
K9	GND	Power/ground pin					GND
K10	VDD1V2	Power/ground pin					VDD

Figure 2: Terminal connections and pin descriptions – Continued

Position	Signal Name	I/O	Level	Volt. [V]	Pull	Polarity	Note
K11	VDIG3V3	Power/ground pin					VDIG3V3
K12		VDD1V2		Power/ground pin			VDD
K13		GND		Power/ground pin			GND
K14		VDD1V2		Power/ground pin			VDD
K15		GND		Power/ground pin			GND
K16		VDD1V2		Power/ground pin			VDD
K17		GND		Power/ground pin			GND
K18		VDD1V2		Power/ground pin			VDD
K19		VSS3V3		Power/ground pin			VSS3V3
K20		VDIG3V3		Power/ground pin			VDIG3V3
K21		VSS2V5		Power/ground pin			VSS2V5
K22	SPW_TXS_P[4]	O	LVDS	2.5	-	Pos	SpaceWire
K23	SPW_TXS_N[4]	O	LVDS	2.5	-	Neg	SpaceWire
K24	SPW_TXD_P[4]	O	LVDS	2.5	-	Pos	SpaceWire
K25	SPW_TXD_N[4]	O	LVDS	2.5	-	Neg	SpaceWire
L1	ETH0_RXD[4]	I	LVCMOS	3.3	-		Ethernet
L2	ETH0_RXD[6]	I	LVCMOS	3.3	-		Ethernet
L4	ETH0_RXD[1]	I	LVCMOS	3.3	-		Ethernet
L5	ETH0_RXDV	I	LVCMOS	3.3	-	High	Ethernet
L6	VSS3V3	Power/ground pin					VSS3V3
L7	VDIG3V3	Power/ground pin					VDIG3V3
L8	GND	Power/ground pin					GND
L9	VDD1V2	Power/ground pin					VDD
L10	GND	Power/ground pin					GND
L11	VDD1V2	Power/ground pin					VDD
L12	GND	Power/ground pin					GND
L13	VDD1V2	Power/ground pin					VDD
L14	GND	Power/ground pin					GND
L15	VDD1V2	Power/ground pin					VDD
L16	GND	Power/ground pin					GND
L17	VDD1V2	Power/ground pin					VDD
L18	GND	Power/ground pin					GND
L19	VDIG3V3	Power/ground pin					VDIG3V3
L20	VSS3V3	Power/ground pin					VSS3V3
L21	VDIG2V5	Power/ground pin					VDIG2V5
L22	SPW_RXS_P[4]	I	LVDS	2.5	DiffTerm	Pos	SpaceWire
L23	SPW_RXS_N[4]	I	LVDS	2.5	DiffTerm	Neg	SpaceWire
L24	SPW_RXD_P[4]	I	LVDS	2.5	DiffTerm	Pos	SpaceWire

Figure 2: Terminal connections and pin descriptions – Continued

Position	Signal Name	I/O	Level	Volt. [V]	Pull	Polarity	Note
L25	SPW_RXD_N[4]	I	LVDS	2.5	DiffTerm	Neg	SpaceWire
M1	ETH0_RXER	I	LVCMOS	3.3	-	High	Ethernet
M2	ETH0_GTXCLK	I	LVCMOS	3.3	-		Ethernet
M3	ETH0_RXD[5]	I	LVCMOS	3.3	-		Ethernet
M4	ETH0_RXD[3]	I	LVCMOS	3.3	-		Ethernet
M5	ETH0_RXD[7]	I	LVCMOS	3.3	-		Ethernet
M6	VDIG3V3	Power/ground pin					VDIG3V3
M7	VSS3V3	Power/ground pin					VSS3V3
M8	VDD1V2	Power/ground pin					VDD
M9	GND	Power/ground pin					GND
M10	VDD1V2	Power/ground pin					VDD
M11	GND	Power/ground pin					GND
M12	VDD1V2	Power/ground pin					VDD
M13	GND	Power/ground pin					GND
M14	VDD1V2	Power/ground pin					VDD
M15	GND	Power/ground pin					GND
M16	VDD1V2	Power/ground pin					VDD
M17	GND	Power/ground pin					GND
M18	VDD1V2	Power/ground pin					VDD
M19	VSS3V3	Power/ground pin					VSS3V3
M20	VDIG3V3	Power/ground pin					VDIG3V3
M21	VSS2V5	Power/ground pin					VSS2V5
M22	SPW_TXS_P[3]	O	LVDS	2.5	-	Pos	SpaceWire
M23	SPW_TXS_N[3]	O	LVDS	2.5	-	Neg	SpaceWire
M24	SPW_TXD_P[3]	O	LVDS	2.5	-	Pos	SpaceWire
M25	SPW_TXD_N[3]	O	LVDS	2.5	-	Neg	SpaceWire
N1	ETH0_TXD[0]	O	LVCMOS	3.3	-		Ethernet
N2	ETH0_TXD[2]	O	LVCMOS	3.3	-		Ethernet
N3	VSS3V3	Power/ground pin					VSS3V3
N4	ETH0_TXEN	O	LVCMOS	3.3	-	High	Ethernet
N5	ETH0_TXCLK	I	LVCMOS	3.3	-		Ethernet
N6	VSS3V3	Power/ground pin					VSS3V3
N7	VDIG3V3	Power/ground pin					VDIG3V3
N8	GND	Power/ground pin					GND
N9	VDD1V2	Power/ground pin					VDD
N10	GND	Power/ground pin					GND
N11	VDD1V2	Power/ground pin					VDD
N12	GND	Power/ground pin					GND
N13	VDD1V2	Power/ground pin					VDD

Figure 2: Terminal connections and pin descriptions – Continued

Position	Signal Name	I/O	Level	Volt. [V]	Pull	Polarity	Note
N14	GND	Power/ground pin					GND
N15	VDD1V2	Power/ground pin					VDD
N16	GND	Power/ground pin					GND
N17	VDD1V2	Power/ground pin					VDD
N18	GND	Power/ground pin					GND
N19	VDIG3V3	Power/ground pin					VDIG3V3
N20	VSS3V3	Power/ground pin					VSS3V3
N21	VDIG2V5	Power/ground pin					VDIG2V5
N22	SPW_RXS_P[3]	I	LVDS	2.5	DiffTerm	Pos	SpaceWire
N23	SPW_RXS_N[3]	I	LVDS	2.5	DiffTerm	Neg	SpaceWire
N24	SPW_RXD_P[3]	I	LVDS	2.5	DiffTerm	Pos	SpaceWire
N25	SPW_RXD_N[3]	I	LVDS	2.5	DiffTerm	Neg	SpaceWire
P1	ETH0_TXD[4]	O	LVCMOS	3.3	-		Ethernet
P2	ETH0_TXD[6]	O	LVCMOS	3.3	-		Ethernet
P3	VDIG3V3	Power/ground pin					VDIG3V3
P4	ETH0_TXD[3]	O	LVCMOS	3.3	-		Ethernet
P5	ETH0_TXD[1]	O	LVCMOS	3.3	-		Ethernet
P6	VDIG3V3	Power/ground pin					VDIG3V3
P7	VSS3V3	Power/ground pin					VSS3V3
P8	VDD1V2	Power/ground pin					VDD
P9	GND	Power/ground pin					GND
P10	VDD1V2	Power/ground pin					VDD
P11	GND	Power/ground pin					GND
P12	VDD1V2	Power/ground pin					VDD
P13	GND	Power/ground pin					GND
P14	VDD1V2	Power/ground pin					VDD
P15	GND	Power/ground pin					GND
P16	VDD1V2	Power/ground pin					VDD
P17	GND	Power/ground pin					GND
P18	VDD1V2	Power/ground pin					VDD
P19	VSS3V3	Power/ground pin					VSS3V3
P20	VDIG3V3	Power/ground pin					VDIG3V3
P21	VSS2V5	Power/ground pin					VSS2V5
P22	SPW_TXS_P[2]	O	LVDS	2.5	-	Pos	SpaceWire
P23	SPW_TXS_N[2]	O	LVDS	2.5	-	Neg	SpaceWire
P24	SPW_TXD_P[2]	O	LVDS	2.5	-	Pos	SpaceWire
P25	SPW_TXD_N[2]	O	LVDS	2.5	-	Neg	SpaceWire
R1	ETH0_TXER	O	LVCMOS	3.3	-	High	Ethernet
R2	MEM_DQ[1]	IO	LVCMOS	3.3	-		SDRAM
R3	VSS3V3	Power/ground pin					VSS3V3

Figure 2: Terminal connections and pin descriptions – Continued

Position	Signal Name	I/O	Level	Volt. [V]	Pull	Polarity	Note
R4	ETH0_TXD[7]	O	LVCMOS	3.3	-		Ethernet
R5	ETH0_TXD[5]	O	LVCMOS	3.3	-		Ethernet
R6	VSS3V3	Power/ground pin					VSS3V3
R7	VDIG3V3	Power/ground pin					VDIG3V3
R8	GND	Power/ground pin					GND
R9	VDD1V2	Power/ground pin					VDD
R10	GND	Power/ground pin					GND
R11	VDD1V2	Power/ground pin					VDD
R12	GND	Power/ground pin					GND
R13	VDD1V2	Power/ground pin					VDD
R14	GND	Power/ground pin					GND
R15	VDD1V2	Power/ground pin					VDD
R16	GND	Power/ground pin					GND
R17	VDD1V2	Power/ground pin					VDD
R18	GND	Power/ground pin					GND
R19	VDIG3V3	Power/ground pin					VDIG3V3
R20	VSS3V3	Power/ground pin					VSS3V3
R21	VDIG2V5	Power/ground pin					VDIG2V5
R22	SPW_RXS_P[2]	I	LVDS	2.5	DiffTerm	Pos	SpaceWire
R23	SPW_RXS_N[2]	I	LVDS	2.5	DiffTerm	Neg	SpaceWire
R24	SPW_RXD_P[2]	I	LVDS	2.5	DiffTerm	Pos	SpaceWire
R25	SPW_RXD_N[2]	I	LVDS	2.5	DiffTerm	Neg	SpaceWire
T1	MEM_DQ[3]	IO	LVCMOS	3.3	-		SDRAM
T2	MEM_DQ[5]	IO	LVCMOS	3.3	-		SDRAM
T3	MEM_DQ[2]	IO	LVCMOS	3.3	-		SDRAM
T4	MEM_DQ[4]	IO	LVCMOS	3.3	-		SDRAM
T5	MEM_DQ[0]	IO	LVCMOS	3.3	-		SDRAM
T6	VDIG3V3	Power/ground pin					VDIG3V3
T7	VSS3V3	Power/ground pin					VSS3V3
T8	VDD1V2	Power/ground pin					VDD
T9	GND	Power/ground pin					GND
T10	VDD1V2	Power/ground pin					VDD
T11	GND	Power/ground pin					GND
T12	VDD1V2	Power/ground pin					VDD
T13	GND	Power/ground pin					GND
T14	VDD1V2	Power/ground pin					VDD
T15	GND	Power/ground pin					GND
T16	VDD1V2	Power/ground pin					VDD
T17	GND	Power/ground pin					GND
T18	VDD1V2	Power/ground pin					VDD

Figure 2: Terminal connections and pin descriptions – Continued

Position	Signal Name	I/O	Level	Volt. [V]	Pull	Polarity	Note
T19	VSS3V3	Power/ground pin					VSS3V3
T20	VDIG3V3	Power/ground pin					VDIG3V3
T21	VSS2V5	Power/ground pin					VSS2V5
T22	SPW_TXS_P[1]	O	LVDS	2.5	-	Pos	SpaceWire
T23	SPW_TXS_N[1]	O	LVDS	2.5	-	Neg	SpaceWire
T24	SPW_TXD_P[1]	O	LVDS	2.5	-	Pos	SpaceWire
T25	SPW_TXD_N[1]	O	LVDS	2.5	-	Neg	SpaceWire
U1	MEM_DQ[7]	IO	LVCMOS	3.3	-		SDRAM
U2	MEM_DQM[1]	O	LVCMOS	3.3	-	Low	SDRAM
U3	VDIG3V3	Power/ground pin					VDIG3V3
U4	MEM_DQM[0]	O	LVCMOS	3.3	-	Low	SDRAM
U5	MEM_DQ[6]	IO	LVCMOS	3.3	-		SDRAM
U6	VSS3V3	Power/ground pin					VSS3V3
U7	VDIG3V3	Power/ground pin					VDIG3V3
U8	GND	Power/ground pin					GND
U9	VDD1V2	Power/ground pin					VDD
U10	GND	Power/ground pin					GND
U11	VDD1V2	Power/ground pin					VDD
U12	GND	Power/ground pin					GND
U13	VDD1V2	Power/ground pin					VDD
U14	GND	Power/ground pin					GND
U15	VDD1V2	Power/ground pin					VDD
U16	GND	Power/ground pin					GND
U17	VDD1V2	Power/ground pin					VDD
U18	GND	Power/ground pin					GND
U19	VDIG3V3	Power/ground pin					VDIG3V3
U20	VSS3V3	Power/ground pin					VSS3V3
U21	VDIG2V5	Power/ground pin					VDIG2V5
U22	SPW_RXS_P[1]	I	LVDS	2.5	DiffTerm	Pos	SpaceWire
U23	SPW_RXS_N[1]	I	LVDS	2.5	DiffTerm	Neg	SpaceWire
U24	SPW_RXD_P[1]	I	LVDS	2.5	DiffTerm	Pos	SpaceWire
U25	SPW_RXD_N[1]	I	LVDS	2.5	DiffTerm	Neg	SpaceWire
V1	MEM_DQ[9]	IO	LVCMOS	3.3	-		SDRAM
V2	MEM_DQ[11]	IO	LVCMOS	3.3	-		SDRAM
V3	VSS3V3	Power/ground pin					VSS3V3
V4	MEM_DQ[10]	IO	LVCMOS	3.3	-		SDRAM
V5	MEM_DQ[8]	IO	LVCMOS	3.3	-		SDRAM
V6	VDIG3V3	Power/ground pin					VDIG3V3
V7	VSS3V3	Power/ground pin					VSS3V3

Figure 2: Terminal connections and pin descriptions – Continued

Position	Signal Name	I/O	Level	Volt. [V]	Pull	Polarity	Note
V8	VDD1V2	Power/ground pin					VDD
V9	GND	Power/ground pin					GND
V10	VDD1V2	Power/ground pin					VDD
V11	GND	Power/ground pin					GND
V12	VDD1V2	Power/ground pin					VDD
V13	GND	Power/ground pin					GND
V14	VDD1V2	Power/ground pin					VDD
V15	GND	Power/ground pin					GND
V16	VDD1V2	Power/ground pin					VDD
V17	GND	Power/ground pin					GND
V18	VDD1V2	Power/ground pin					VDD
V19	VSS3V3	Power/ground pin					VSS3V3
V20	VDIG3V3	Power/ground pin					VDIG3V3
V21	VSS2V5	Power/ground pin					VSS2V5
V22	SPW_TXS_P[0]	O	LVDS	2.5	-	Pos	SpaceWire
V23	SPW_TXS_N[0]	O	LVDS	2.5	-	Neg	SpaceWire
V24	SPW_TXD_P[0]	O	LVDS	2.5	-	Pos	SpaceWire
V25	SPW_TXD_N[0]	O	LVDS	2.5	-	Neg	SpaceWire
W1	MEM_DQ[15]	IO	LVCMOS	3.3	-		SDRAM
W2	MEM_DQ[13]	IO	LVCMOS	3.3	-		SDRAM
W3	VDIG3V3	Power/ground pin					VDIG3V3
W4	MEM_DQ[14]	IO	LVCMOS	3.3	-		SDRAM
W5	MEM_DQ[12]	IO	LVCMOS	3.3	-		SDRAM
W6	VSS3V3	Power/ground pin					VSS3V3
W7	VDIG3V3	Power/ground pin					VDIG3V3
W8	VSS3V3	Power/ground pin					VSS3V3
W9	VDIG3V3	Power/ground pin					VDIG3V3
W10	VSS3V3	Power/ground pin					VSS3V3
W11	VDIG3V3	Power/ground pin					VDIG3V3
W12	VSS3V3	Power/ground pin					VSS3V3
W13	VDIG3V3	Power/ground pin					VDIG3V3
W14	VSS3V3	Power/ground pin					VSS3V3
W15	VDIG3V3	Power/ground pin					VDIG3V3
W16	VSS3V3	Power/ground pin					VSS3V3
W17	VDIG3V3	Power/ground pin					VDIG3V3
W18	VSS3V3	Power/ground pin					VSS3V3
W19	VDIG3V3	Power/ground pin					VDIG3V3
W20	VSS3V3	Power/ground pin					VSS3V3
W21	VSS2V5	Power/ground pin					VSS2V5
W22	SPW_RXS_P[0]	I	LVDS	2.5	DiffTerm	Pos	SpaceWire

Figure 2: Terminal connections and pin descriptions – Continued

Position	Signal Name	I/O	Level	Volt. [V]	Pull	Polarity	Note
W23	SPW_RXS_N[0]	I	LVDS	2.5	DiffTerm	Neg	SpaceWire
W24	SPW_RXD_P[0]	I	LVDS	2.5	DiffTerm	Pos	SpaceWire
W25	SPW_RXD_N[0]	I	LVDS	2.5	DiffTerm	Neg	SpaceWire
Y1	MEM_DQ[19]	IO	LVCMOS	3.3	-		SDRAM
Y2	MEM_DQ[17]	IO	LVCMOS	3.3	-		SDRAM
Y3	VSS3V3	Power/ground pin					VSS3V3
Y4	MEM_DQ[20]	IO	LVCMOS	3.3	-		SDRAM
Y5	MEM_DQ[16]	IO	LVCMOS	3.3	-		SDRAM
Y6	VDIG3V3	Power/ground pin					VDIG3V3
Y7	VSS3V3	Power/ground pin					VSS3V3
Y8	VDIG3V3	Power/ground pin					VDIG3V3
Y9	VSS3V3	Power/ground pin					VSS3V3
Y10	VDIG3V3	Power/ground pin					VDIG3V3
Y11	VSS3V3	Power/ground pin					VSS3V3
Y12	VDIG3V3	Power/ground pin					VDIG3V3
Y13	VSS3V3	Power/ground pin					VSS3V3
Y14	VDIG3V3	Power/ground pin					VDIG3V3
Y15	VSS3V3	Power/ground pin					VSS3V3
Y16	VDIG3V3	Power/ground pin					VDIG3V3
Y17	VSS3V3	Power/ground pin					VSS3V3
Y18	VDIG3V3	Power/ground pin					VDIG3V3
Y19	VSS3V3	Power/ground pin					VSS3V3
Y20	MEM_CLK_OUT	O	LVCMOS	3.3	-		SDRAM
Y21	VSS2V5	Power/ground pin					VSS2V5
Y22	VSS2V5	Power/ground pin					VSS2V5
Y23	VSS2V5	Power/ground pin					VSS2V5
Y24	VSS2V5	Power/ground pin					VSS2V5
Y25	VSS2V5	Power/ground pin					VSS2V5
AA1	MEM_DQ[23]	IO	LVCMOS	3.3	-		SDRAM
AA2	MEM_DQ[21]	IO	LVCMOS	3.3	-		SDRAM
AA3	MEM_DQM[2]	O	LVCMOS	3.3	-	Low	SDRAM
AA4	MEM_DQ[22]	IO	LVCMOS	3.3	-		SDRAM
AA5	MEM_DQ[18]	IO	LVCMOS	3.3	-		SDRAM
AA6	MEM_DQ[36]	IO	LVCMOS	3.3	-		SDRAM
AA7	MEM_DQ[40]	IO	LVCMOS	3.3	-		SDRAM
AA8	MEM_DQ[46]	IO	LVCMOS	3.3	-		SDRAM
AA9	MEM_SN[1]	O	LVCMOS	3.3	-	Low	SDRAM
AA10	MEM_ADDR[7]	O	LVCMOS	3.3	-		SDRAM
AA11	MEM_ADDR[13]	O	LVCMOS	3.3	-		SDRAM

Figure 2: Terminal connections and pin descriptions – Continued

Position	Signal Name	I/O	Level	Volt. [V]	Pull	Polarity	Note
AA12	MEM_CASN	O	LVCMOS	3.3	-	Low	SDRAM
AA13	MEM_WEN	O	LVCMOS	3.3	-	Low	SDRAM
AA14	MEM_DQ[51]	IO	LVCMOS	3.3	-		SDRAM
AA15	MEM_DQ[53]	IO	LVCMOS	3.3	-		SDRAM
AA16	MEM_DQM[7]	IO	LVCMOS	3.3	-	Low	SDRAM
AA17	MEM_DQ[65]	IO	LVCMOS	3.3	-		SDRAM
AA18	MEM_DQ[69]	IO	LVCMOS	3.3	-		SDRAM
AA19	MEM_DQ[73]	IO	LVCMOS	3.3	-		SDRAM
AA20	MEM_DQ[79]	IO	LVCMOS	3.3	-		SDRAM
AA21	MEM_DQ[88]	IO	LVCMOS	3.3	-		SDRAM
AA22	MEM_DQ[92]	IO	LVCMOS	3.3	-		SDRAM
AA23	MEM_DQ[94]	IO	LVCMOS	3.3	-		SDRAM
AA24	MEM_CLK_OUT_DIFF_P	O	LVDS	2.5	-	Pos	SDRAM
AA25	MEM_CLK_OUT_DIFF_N	O	LVDS	2.5	-	Neg	SDRAM
AB1	MEM_DQM[3]	O	LVCMOS	3.3	-	Low	SDRAM
AB2	MEM_DQ[25]	IO	LVCMOS	3.3	-		SDRAM
AB3	MEM_DQ[26]	IO	LVCMOS	3.3	-		SDRAM
AB4	MEM_DQ[28]	IO	LVCMOS	3.3	-		SDRAM
AB5	MEM_DQ[24]	IO	LVCMOS	3.3	-		SDRAM
AB6	MEM_DQM[4]	IO	LVCMOS	3.3	-	Low	SDRAM
AB7	MEM_DQ[44]	IO	LVCMOS	3.3	-		SDRAM
AB8	MEM_CLK_IN	I	LVCMOS	3.3	-		SDRAM
AB9	MEM_ADDR[1]	O	LVCMOS	3.3	-		SDRAM
AB10	MEM_ADDR[3]	O	LVCMOS	3.3	-		SDRAM
AB11	MEM_ADDR[11]	O	LVCMOS	3.3	-		SDRAM
AB12	MEM_BA[0]	O	LVCMOS	3.3	-		SDRAM
AB13	MEM_CKE[1]	O	LVCMOS	3.3	-	High	SDRAM
AB14	MEM_DQ[49]	IO	LVCMOS	3.3	-		SDRAM
AB15	MEM_DQ[55]	IO	LVCMOS	3.3	-		SDRAM
AB16	MEM_DQ[59]	IO	LVCMOS	3.3	-		SDRAM
AB17	MEM_DQ[61]	IO	LVCMOS	3.3	-		SDRAM
AB18	MEM_DQ[67]	IO	LVCMOS	3.3	-		SDRAM
AB19	MEM_DQ[71]	IO	LVCMOS	3.3	-		SDRAM
AB20	MEM_DQ[77]	IO	LVCMOS	3.3	-		SDRAM
AB21	MEM_DQ[86]	IO	LVCMOS	3.3	-		SDRAM
AB22	MEM_DQM[10]	IO	LVCMOS	3.3	-	Low	SDRAM
AB23	MEM_DQ[90]	IO	LVCMOS	3.3	-		SDRAM
AB24	MEM_DQ[95]	IO	LVCMOS	3.3	-		SDRAM
AB25	MEM_DQ[93]	IO	LVCMOS	3.3	-		SDRAM

Figure 2: Terminal connections and pin descriptions – Continued

Position	Signal Name	I/O	Level	Volt. [V]	Pull	Polarity	Note
AC1	MEM_DQ[29]	IO	LVCMOS	3.3	-		SDRAM
AC2	MEM_DQ[27]	IO	LVCMOS	3.3	-		SDRAM
AC3	MEM_DQ[30]	IO	LVCMOS	3.3	-		SDRAM
AC4	MEM_DQ[32]	IO	LVCMOS	3.3	-		SDRAM
AC5	MEM_DQ[34]	IO	LVCMOS	3.3	-		SDRAM
AC6	MEM_DQ[38]	IO	LVCMOS	3.3	-		SDRAM
AC7	MEM_DQ[42]	IO	LVCMOS	3.3	-		SDRAM
AC8	VDIG3V3	Power/ground pin					VDIG3V3
AC9	VSS3V3	Power/ground pin					VSS3V3
AC10	MEM_ADDR[5]	O	LVCMOS	3.3	-		SDRAM
AC11	MEM_ADDR[9]	O	LVCMOS	3.3	-		SDRAM
AC12	VDIG3V3	Power/ground pin					VDIG3V3
AC13	VSS3V3	Power/ground pin					VSS3V3
AC14	GND	Reserved for test, must be tied to ground.					GND
AC15	MEM_DQ[52]	IO	LVCMOS	3.3	-		SDRAM
AC16	MEM_DQ[57]	IO	LVCMOS	3.3	-		SDRAM
AC17	MEM_DQ[63]	IO	LVCMOS	3.3	-		SDRAM
AC18	MEM_DQ[68]	IO	LVCMOS	3.3	-		SDRAM
AC19	MEM_DQM[9]	O	LVCMOS	3.3	-	Low	SDRAM
AC20	MEM_DQ[75]	IO	LVCMOS	3.3	-		SDRAM
AC21	MEM_DQ[81]	IO	LVCMOS	3.3	-		SDRAM
AC22	MEM_DQ[82]	IO	LVCMOS	3.3	-		SDRAM
AC23	MEM_DQ[91]	IO	LVCMOS	3.3	-		SDRAM
AC24	MEM_DQ[89]	IO	LVCMOS	3.3	-		SDRAM
AC25	MEM_DQM[11]	IO	LVCMOS	3.3	-	Low	SDRAM
AD1	GND	Power/ground pin					GND
AD2	GND	Power/ground pin					GND
AD25	GND	Power/ground pin					GND
AD3	MEM_DQ[31]	IO	LVCMOS	3.3	-		SDRAM
AD4	MEM_DQ[35]	IO	LVCMOS	3.3	-		SDRAM
AD5	MEM_DQ[39]	IO	LVCMOS	3.3	-		SDRAM
AD6	MEM_DQ[41]	IO	LVCMOS	3.3	-		SDRAM
AD7	MEM_DQ[45]	IO	LVCMOS	3.3	-		SDRAM
AD8	MEM_SN[0]	O	LVCMOS	3.3	-	Low	SDRAM
AD9	MEM_ADDR[2]	O	LVCMOS	3.3	-		SDRAM
AD10	MEM_ADDR[6]	O	LVCMOS	3.3	-		SDRAM
AD11	MEM_ADDR[10]	O	LVCMOS	3.3	-		SDRAM
AD12	MEM_ADDR[14]	O	LVCMOS	3.3	-		SDRAM
AD13	MEM_RASN	O	LVCMOS	3.3	-	Low	SDRAM

Figure 2: Terminal connections and pin descriptions – Continued

Position	Signal Name	I/O	Level	Volt. [V]	Pull	Polarity	Note
AD14	MEM_DQ[50]	IO	LVCMOS	3.3	-		SDRAM
AD15	MEM_DQM[6]	IO	LVCMOS	3.3	-	Low	SDRAM
AD16	MEM_DQ[56]	IO	LVCMOS	3.3	-		SDRAM
AD17	MEM_DQ[60]	IO	LVCMOS	3.3	-		SDRAM
AD18	MEM_DQ[64]	IO	LVCMOS	3.3	-		SDRAM
AD19	MEM_DQM[8]	O	LVCMOS	3.3	-	Low	SDRAM
AD20	MEM_DQ[74]	IO	LVCMOS	3.3	-		SDRAM
AD21	MEM_DQ[78]	IO	LVCMOS	3.3	-		SDRAM
AD22	MEM_DQ[87]	IO	LVCMOS	3.3	-		SDRAM
AD23	MEM_DQ[85]	IO	LVCMOS	3.3	-		SDRAM
AD24	MEM_DQ[84]	IO	LVCMOS	3.3	-		SDRAM
AE1	GND	Power/ground pin					GND
AE2	GND	Power/ground pin					GND
AE3	MEM_DQ[33]	IO	LVCMOS	3.3	-		SDRAM
AE4	MEM_DQ[37]	IO	LVCMOS	3.3	-		SDRAM
AE5	MEM_DQM[5]	IO	LVCMOS	3.3	-	Low	SDRAM
AE6	MEM_DQ[43]	IO	LVCMOS	3.3	-		SDRAM
AE7	MEM_DQ[47]	IO	LVCMOS	3.3	-		SDRAM
AE8	MEM_ADDR[0]	O	LVCMOS	3.3	-		SDRAM
AE9	MEM_ADDR[4]	O	LVCMOS	3.3	-		SDRAM
AE10	MEM_ADDR[8]	O	LVCMOS	3.3	-		SDRAM
AE11	MEM_ADDR[12]	O	LVCMOS	3.3	-		SDRAM
AE12	MEM_BA[1]	O	LVCMOS	3.3	-		SDRAM
AE13	MEM_CKE[0]	O	LVCMOS	3.3	-	High	SDRAM
AE14	MEM_DQ[48]	IO	LVCMOS	3.3	-		SDRAM
AE15	MEM_DQ[54]	IO	LVCMOS	3.3	-		SDRAM
AE16	MEM_DQ[58]	IO	LVCMOS	3.3	-		SDRAM
AE17	MEM_DQ[62]	IO	LVCMOS	3.3	-		SDRAM
AE18	MEM_DQ[66]	IO	LVCMOS	3.3	-		SDRAM
AE19	MEM_DQ[70]	IO	LVCMOS	3.3	-		SDRAM
AE20	MEM_DQ[72]	IO	LVCMOS	3.3	-		SDRAM
AE21	MEM_DQ[76]	IO	LVCMOS	3.3	-		SDRAM
AE22	MEM_DQ[80]	IO	LVCMOS	3.3	-		SDRAM
AE23	MEM_DQ[83]	IO	LVCMOS	3.3	-		SDRAM
AE24	GND	Power/ground pin					GND
AE25	GND	Power/ground pin					GND

Figure 2: Terminal connections and pin descriptions – Continued

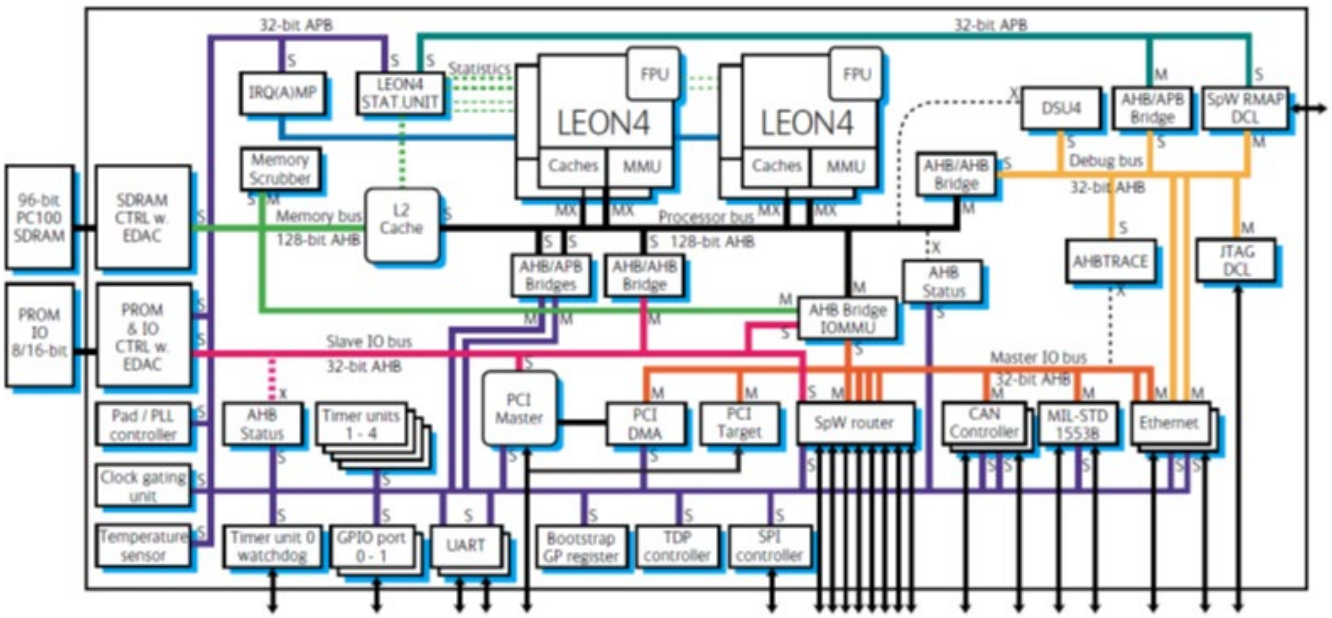


Figure 3: Block diagram

AC characteristics, test conditions

For the SDRAM, Ethernet and PCI interfaces, timing is tested using a transmission line setup as shown in Figure 4. The propagation delays in the test fixture is calibrated out as part of the test procedure.

Interfaces are tested with the pad drive strength set to maximum unless noted otherwise.

Interface timing measurement (setup, hold and clock-to-out) are done with reference to inputs or outputs entering or leaving the limits given for AC parameter test in table IA.

The SDRAM, Ethernet and PCI interfaces are clocked at 25 MHz for the AC parametric tests. For clock-to-output measurements, a test mode is used where one output signal at a time toggles per cycle. For setup/hold timing, a test mode is used where a pseudo-random input sequence is clocked in in parallel on all inputs and compared with an expected sequence.

The SpaceWire interface receive characteristics is tested in functional mode by sending a package at speed into the device and checking that the data was correctly received. For SpaceWire TX skew, the D/S skew is measured directly from the device outputs using time measurement hardware in the test equipment.

It is up to the end user to translate the timing data to data relevant for the system. An IBIS model of the drivers can be provided to aid in this process.

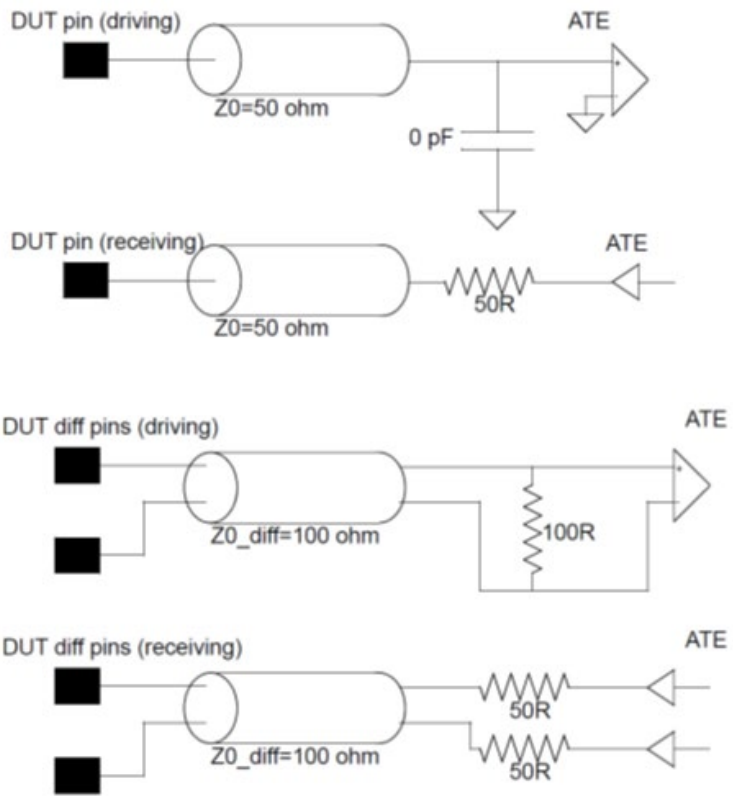


Figure 4: Equivalent test conditions for LVCMOS outputs (1), LVCMOS inputs (2), LVDS outputs (3) and LVDS inputs (4)

Levels and thresholds for AC parameters tests			
Test	Symbol	Value	Unit
High output threshold for AC parameter tests	$V_{OH,ACtest}$	VDIG3V3-0.4	V
Low output threshold for AC parameter tests	$V_{OL,ACtest}$	0.4	V
Clock and input reference point for AC parameter tests	$V_{iref,ACtest}$	VDIG3V3 * 0.5	V
Low DC input level for AC parameter tests	$V_{il,ACtest}$	0.0	V
High DC input level for AC parameter tests	$V_{ih,ACtest}$	VDIG3V3	V
Input signal transition time for AC parameter tests, 10% to 90%	$t_{T,ACtest}$	1.2	ns
LVDS output differential threshold	$V_{Odiff,ACtest}$	0.0	V

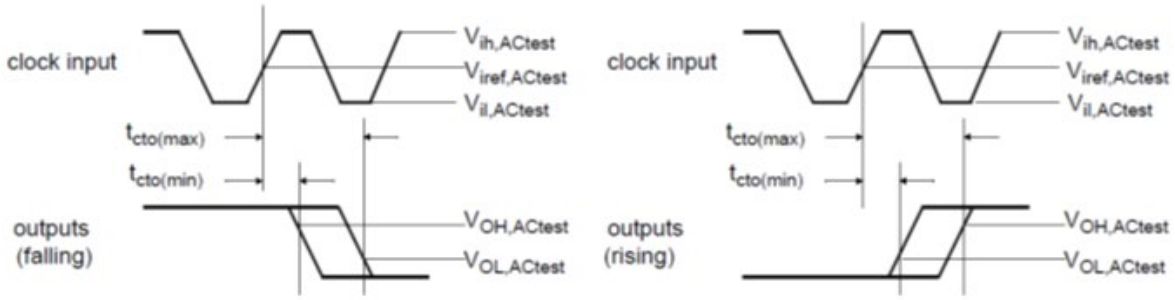


Figure 56. Clock-to-out definition

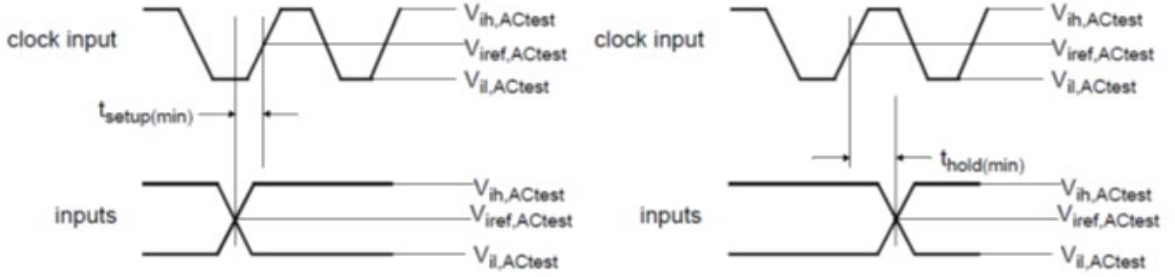


Figure 5: Timing waveforms and test circuits: AC characteristics

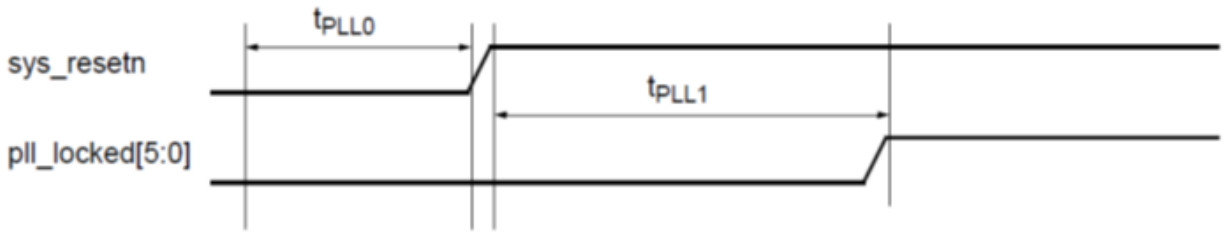


Figure 6: Timing waveforms: Phase-locked loop timings

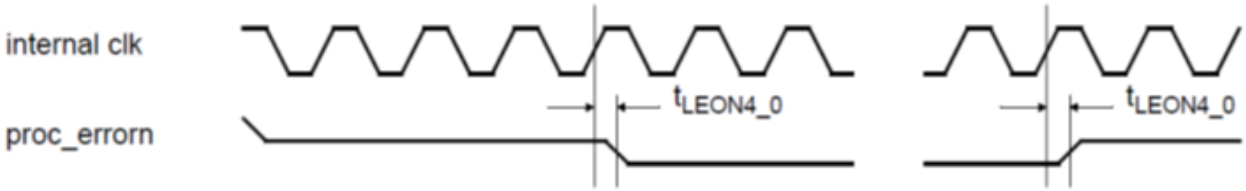


Figure 7: Timing waveforms: Processor error mode signal timing

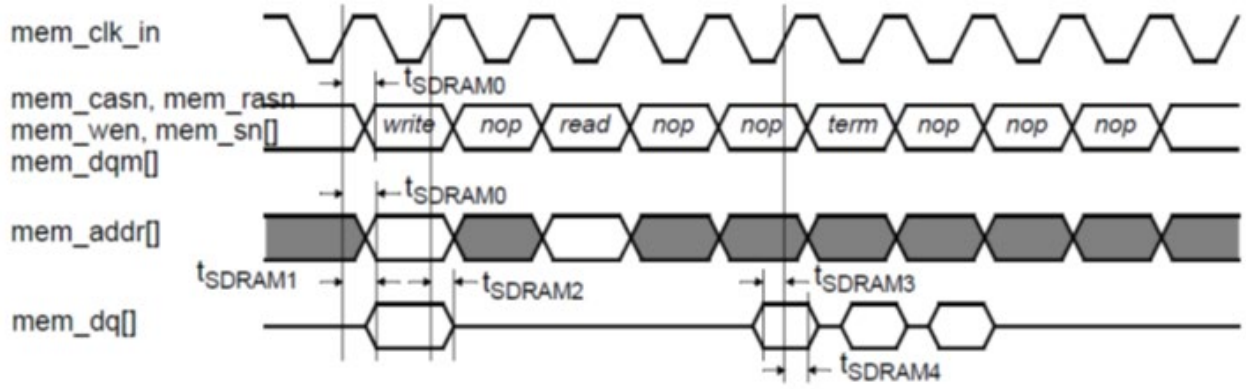


Figure 8: Timing waveforms and test circuits: 64-bit PC100 SDRAM Controller with Reed-Solomon EDAC timing

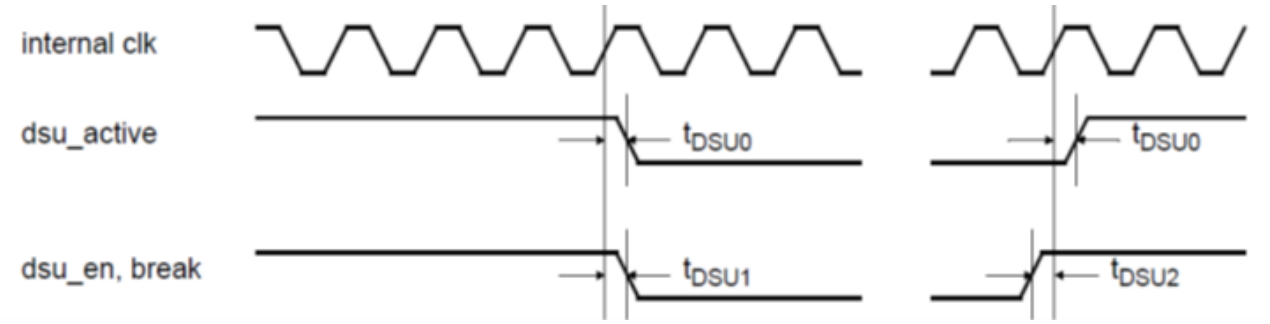


Figure 9: Timing waveforms: DSU signals timing

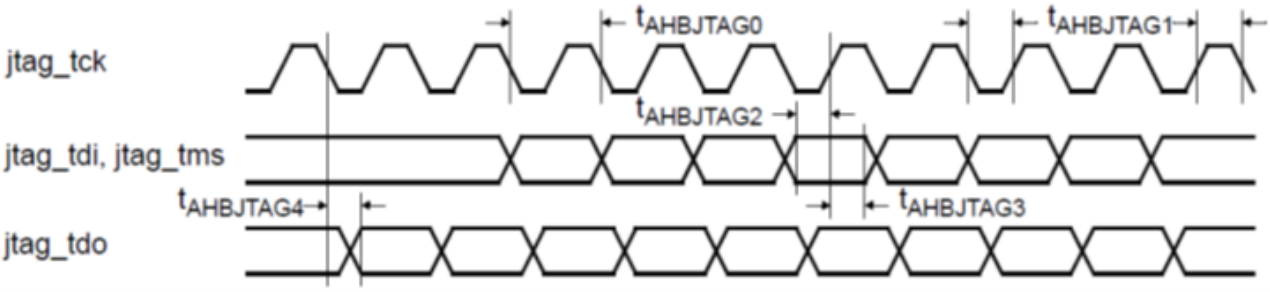


Figure 10: Timing waveforms: JTAG interface timing

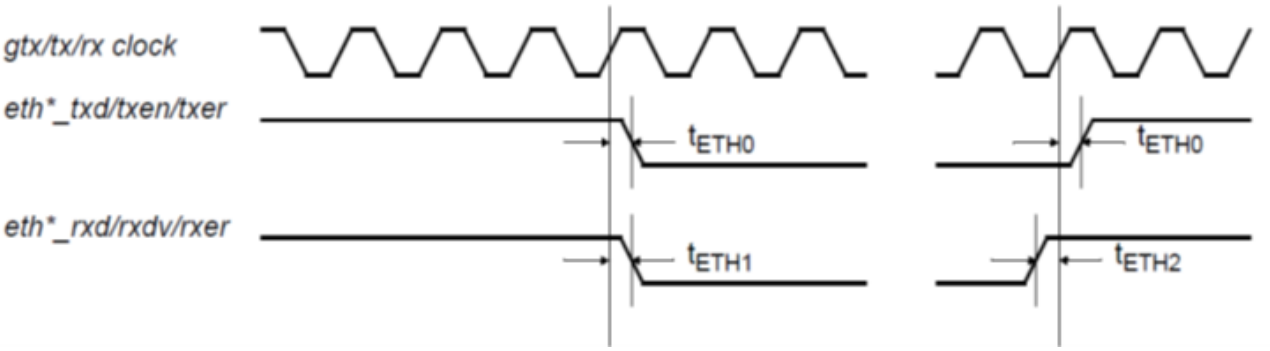


Figure 11: Timing waveforms: Gigabit Ethernet Media Access Controller (MAC) w. EDCL timing

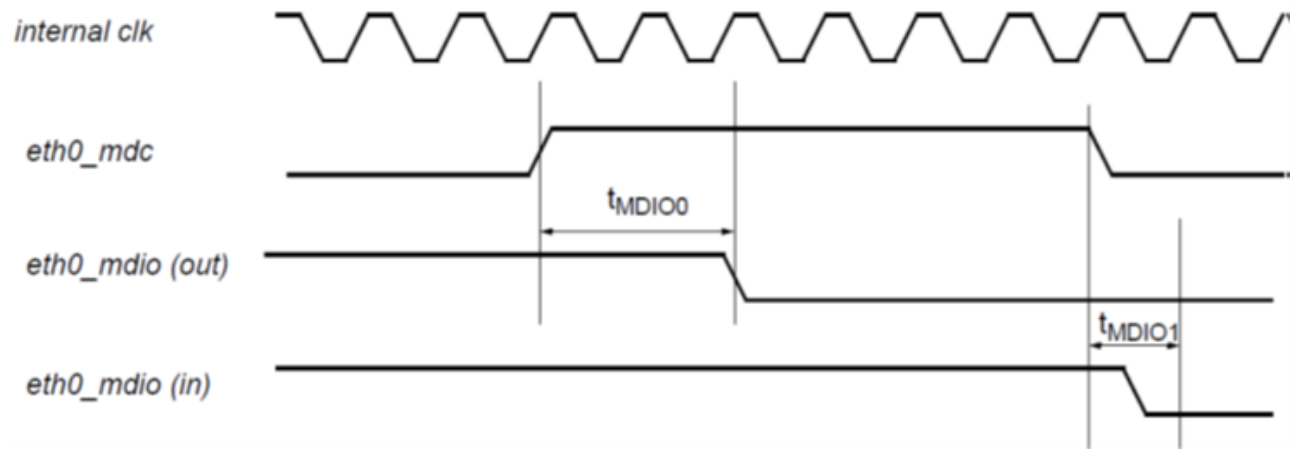


Figure 12: Timing waveforms: MDIO timing

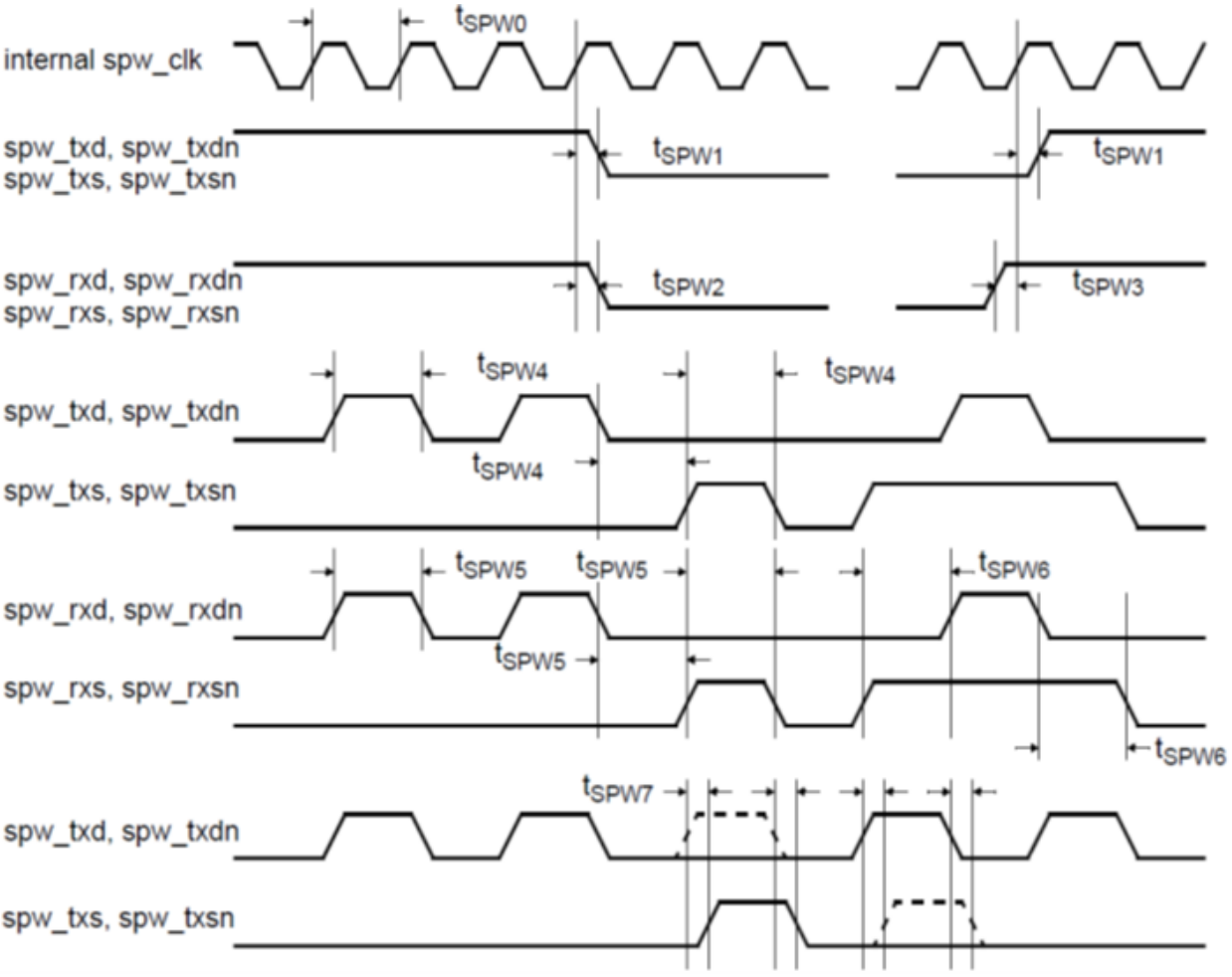


Figure 13: Timing waveforms: SpaceWire router interface timing

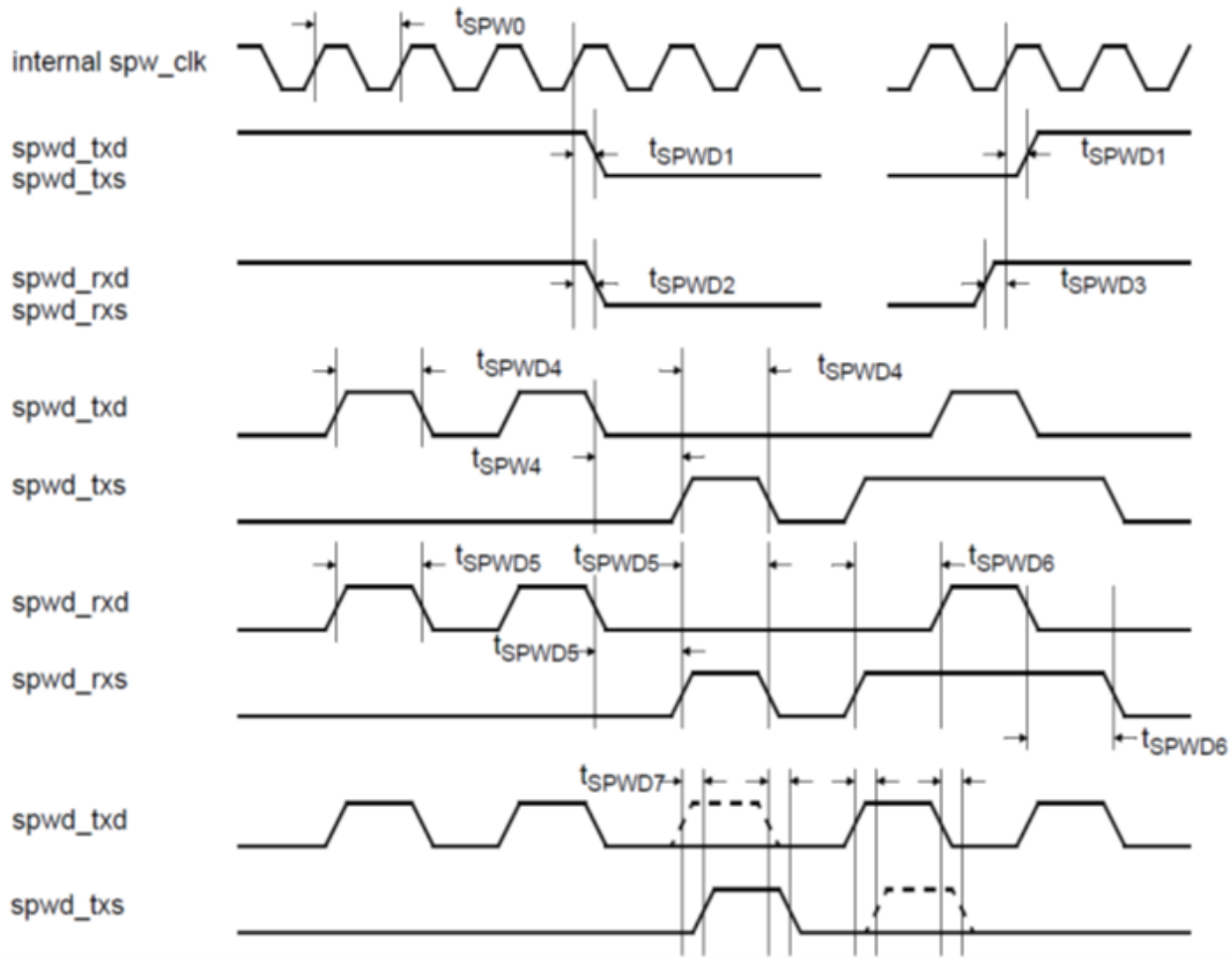


Figure 14: Timing waveforms: SpaceWire debug interface timing

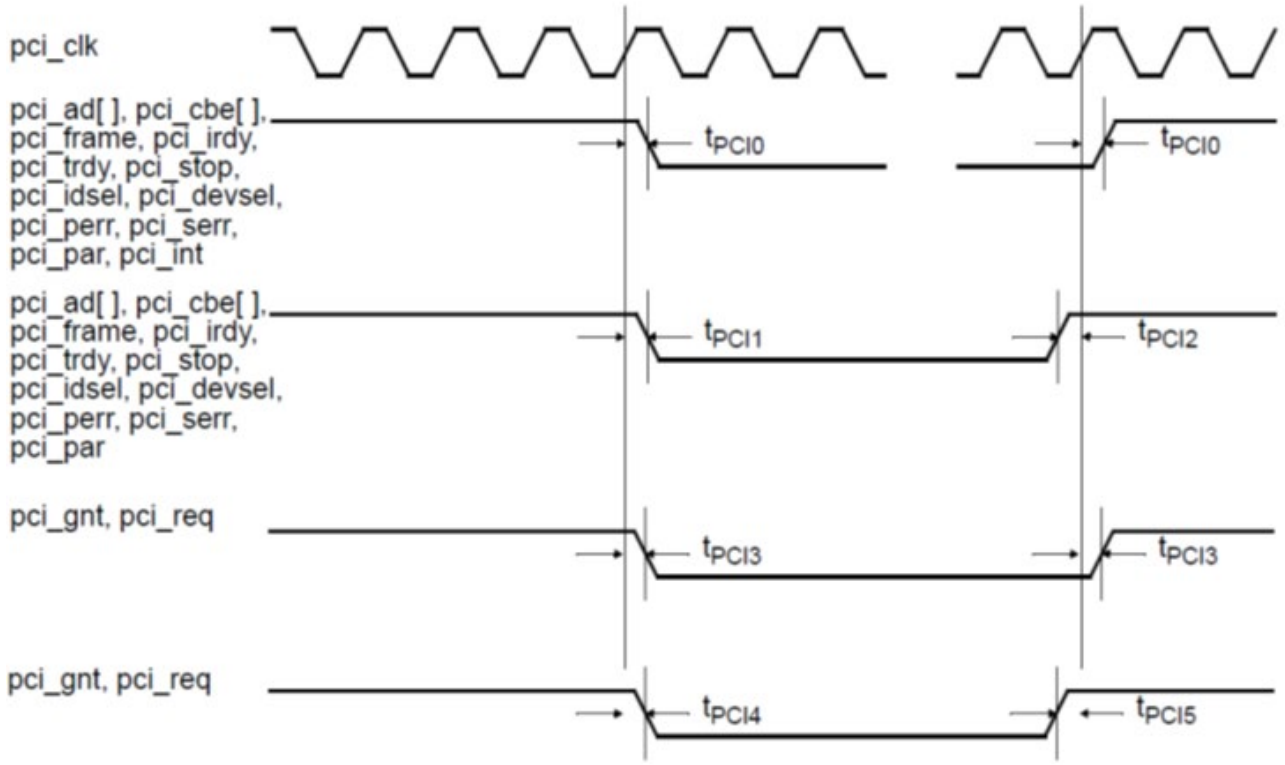


Figure 15: Timing waveforms: PCI interface timing

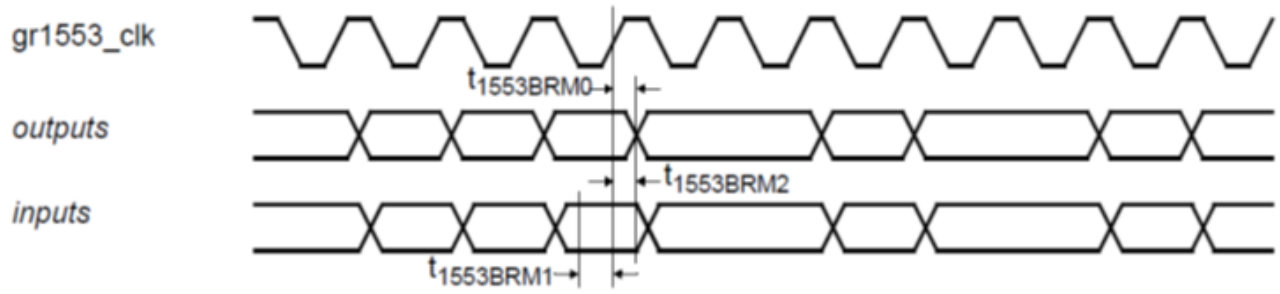


Figure 16: Timing waveforms: MIL-STD-1553B / AS15531 interface timing

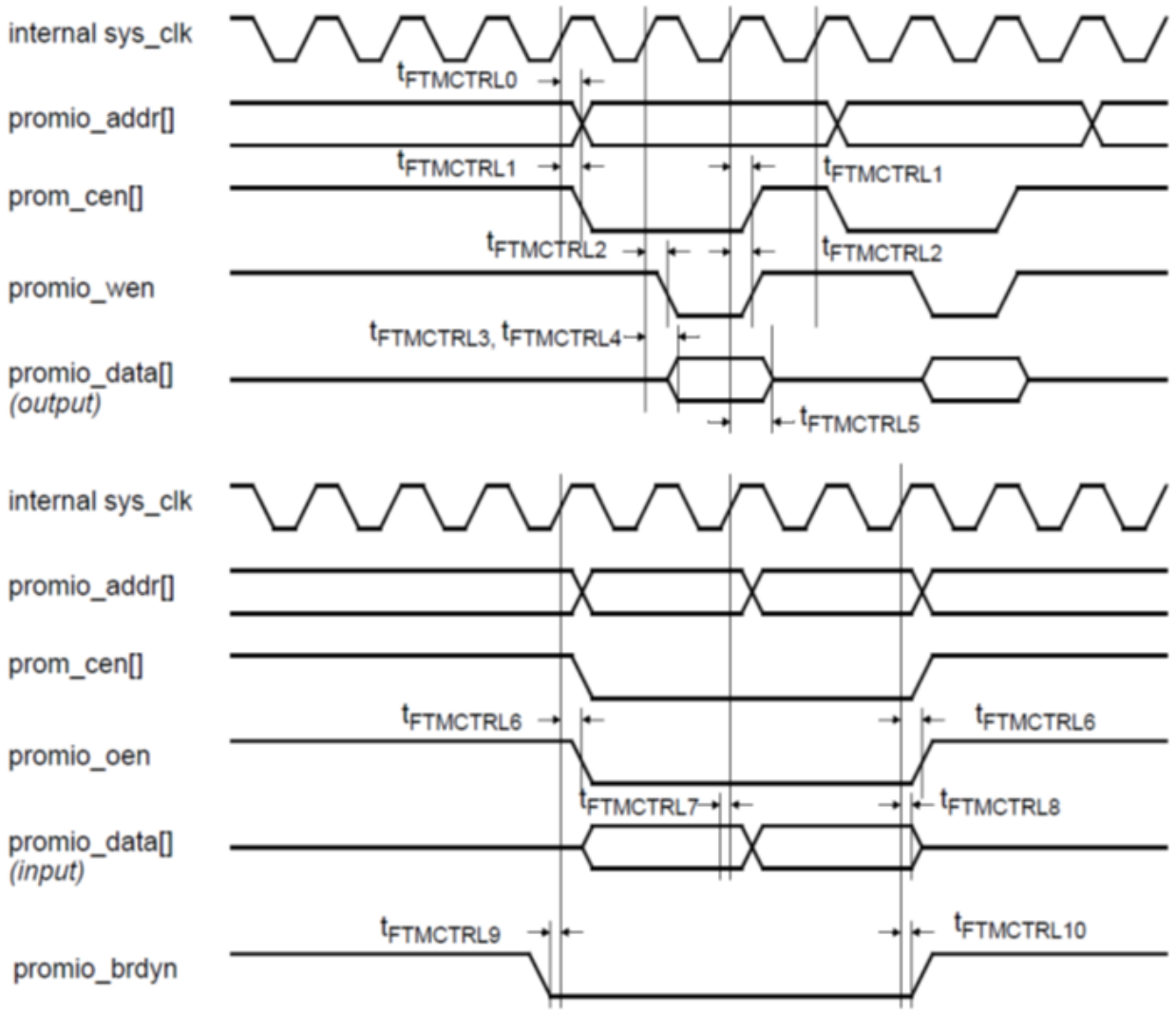


Figure 17: Timing waveforms: Fault-tolerant 8/16-bit PROM/IO memory interface timing (PROM accesses)

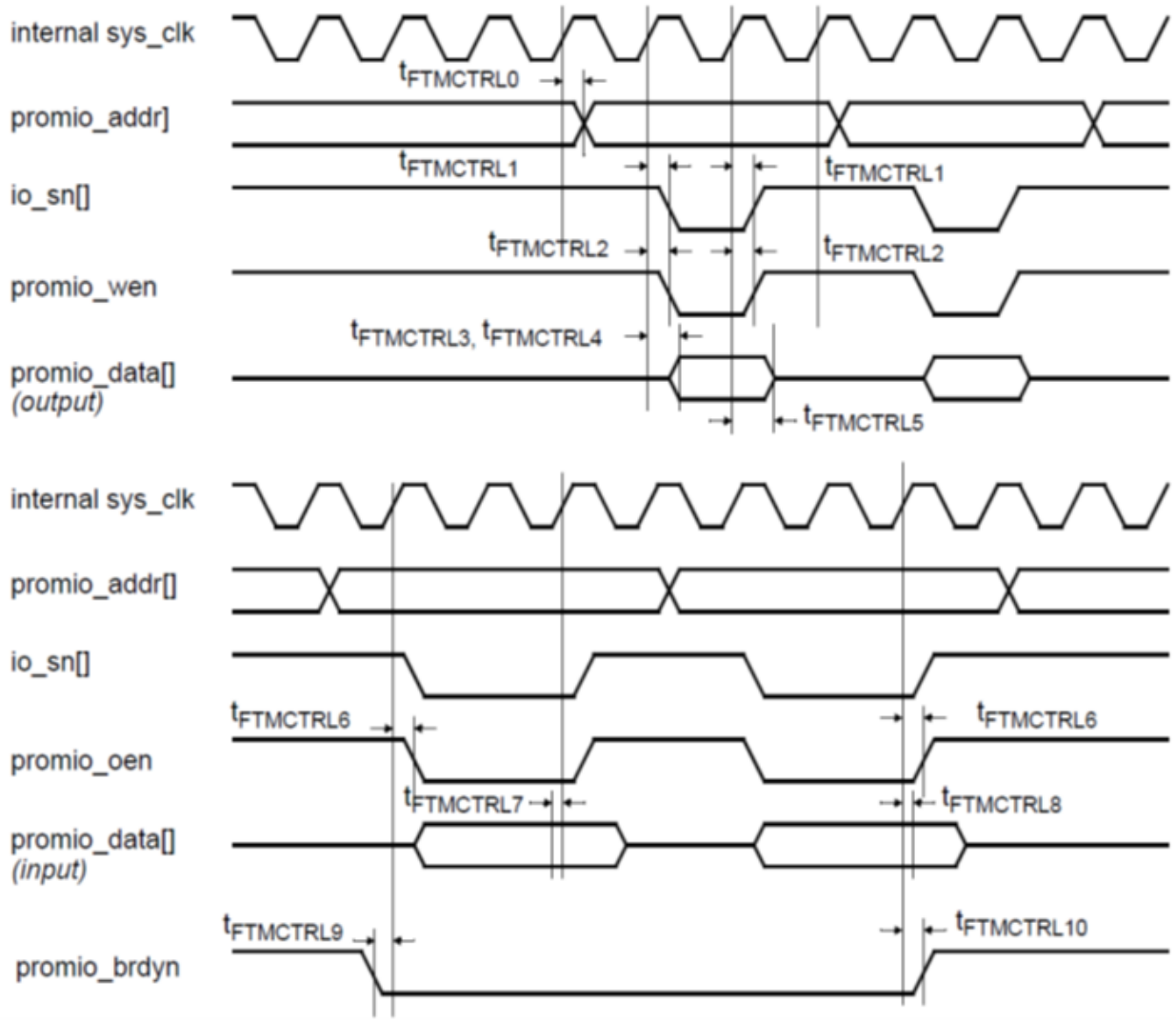


Figure 18: Timing waveforms: Fault-tolerant 8/16-bit PROM/IO memory interface timing (I/O accesses)

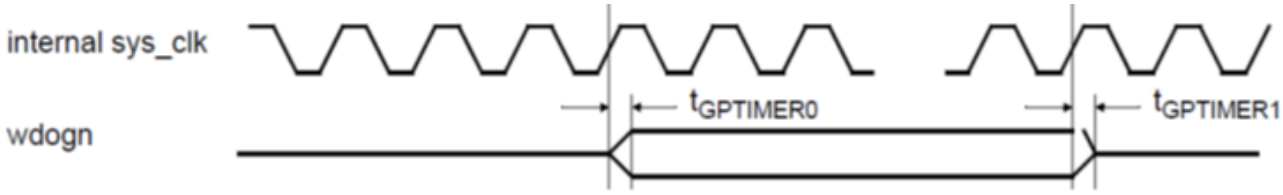


Figure 19: Timing waveforms: Watchdog signal timing

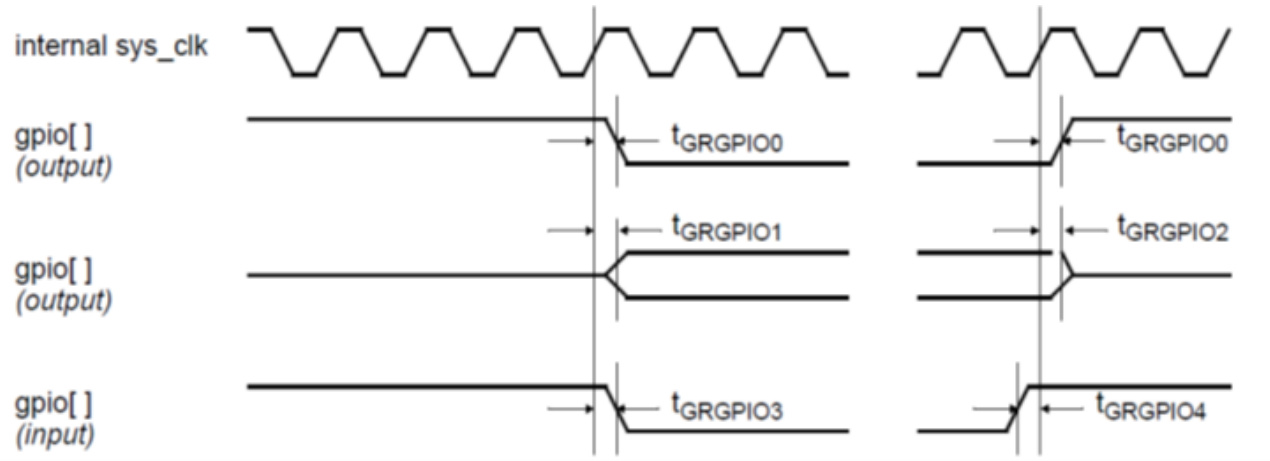


Figure 20: Timing waveforms: General purpose I/O interface timing

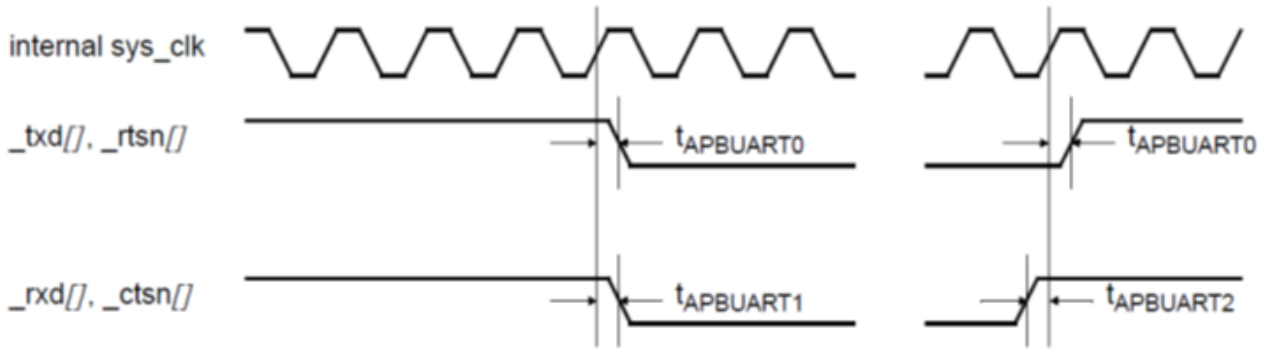


Figure 21: Timing waveforms: UART interface timing

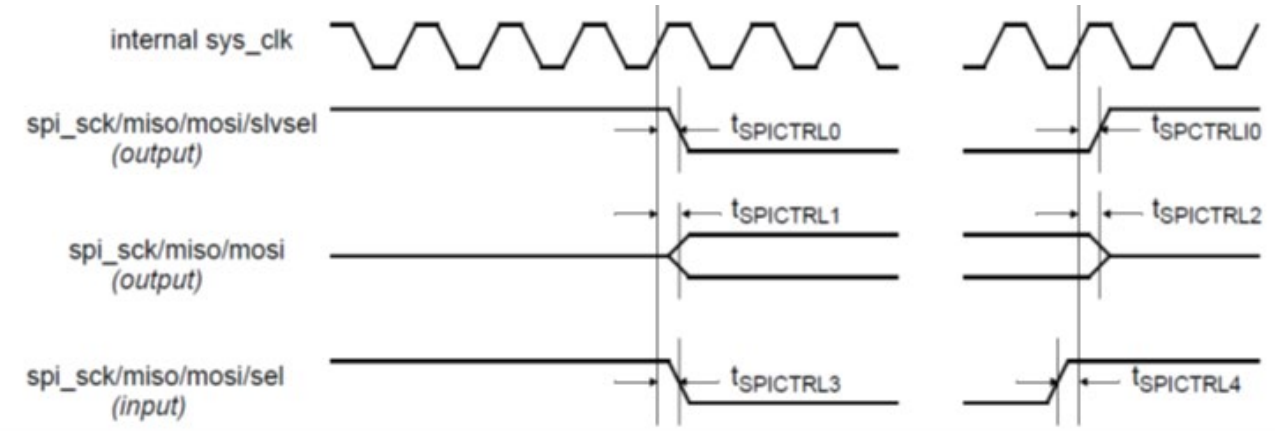


Figure 22: Timing waveforms: SPI controller timing

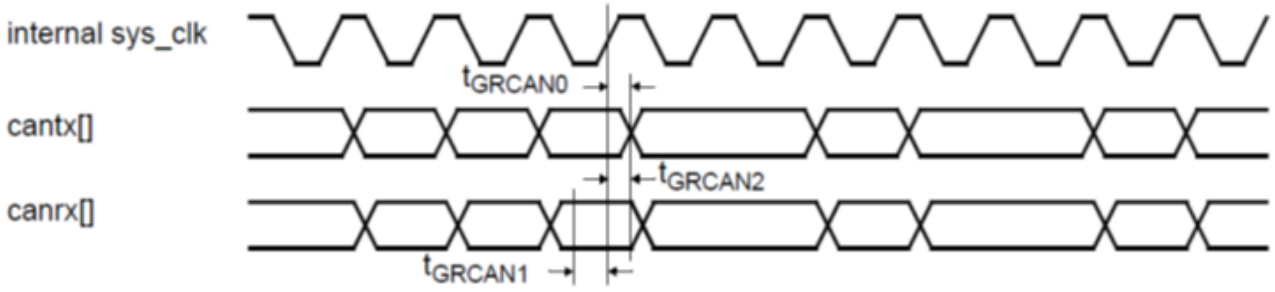


Figure 23: Timing waveforms: CAN controller interface timing

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

d. Unless otherwise specified in the QM plan, for devices class Q and V dynamic burn-in shall be performed with test condition D, method 1015 of MIL-STD-883.

e. For devices class V, interim and post burn-in final electrical test delta parameters shall be specified in delta burn-in table IIB herein.

f. Devices built with case outline X are equivalent to the same device built with case outline Z plus the solder column attachment. All required screening for devices built with case outline X are processed prior to the solder column attachment. After solder column attachment, Group A subgroup 1, as a minimum, shall be performed to verify device functionality.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. ESD CDM & HBM, and O/V (Latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on a minimum of three devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, TABLE III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 4, 7, 9	1, 4, 7, 9
Dynamic burn-in (method 1015)	Required	Required
Reverse bias burn-in (method 1015)	Not Required	Required
Post burn-in interim electrical parameters	1, 4, 7, 9 1/	1, 4, 7, 9 1/ 5/
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 7, 8a, 8b, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8a, 8b 9, 10, 11
Group A test requirements (see 4.4.1)	1, 2, 3, 4, 5, 6, 7, 8a, 8b, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8a, 8b 9, 10, 11
Group C end-point electrical parameters (see 4.4.2)	1, 2, 3, 4, 5, 6, 7, 8a, 8b, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8a, 8b 9, 10, 11 5/
Group D end-point electrical parameters (see 4.4.3) 6/	1, 4, 7, 9	1, 4, 7, 9
Group E end-point electrical parameters (see 4.4.4)	1, 4, 7, 9	1, 4, 7, 9
Post-column attach electrical parameters test (see 4.2) 7/	1	1

1/ PDA applies to subgroup 1 (see 4.2). For device class V, PDA applies to subgroups 1 and 7 (see 4.2).
2/ The burn-in shall meet the requirements of 4.2.1a herein.
3/ On all class V lots, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters (group A, subgroup 1), in accordance with MIL-PRF-38535. For pre-burn-in and interim electrical parameters, the read-and-record requirements are for delta measurements only.
4/ If the device operates in a dynamic mode, then dynamic burn-in test shall be performed per TM 1015 with test condition D (see MIL-PRF-38535 and JEDEC JEP163).
5/ Delta limits shall be required only on table IA, subgroup 1. The delta values shall be computed with reference to the previous interim electrical parameters. The delta limits are specified in table IIB.
6/ For CGA package, Group D test shall be performed all applicable LGA level test and in addition column destructive pull test and salt atmosphere test method (TM 1009) is required.
7/ For CGA package solderability test shall be performed in accordance with test method 2003.

TABLE IIB. Burn-in and operating life test delta parameters (+25°C).

Parameter 1/	Device electrical parameters	Delta limit
LVCMOS Output low voltage	V_{OL}	± 150mV
LVCMOS Output high voltage	V_{OH}	± 150mV
LVDS output difference	V_{ODIFF}	+/-50mV
LVDS output common mode voltage	V_{OCM}	± 100mV

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta (Δ) burn-in.

TABLE IIC. End-point electrical parameter per total ionizing dose. 1/

Parameter 2/	RHA level designator	Radiation and total dose	Limit	Unit
I_{DD1V2S}	F	300 krad(Si)	35 3/	mA

1/ Limits for parameters defined in this table supersede corresponding limits in table IA.
2/ Conditions as defined in table IA.
3/ This limit is exceeded at higher temperatures. At a junction temperature of +125°C, the maximum current consumption of I_{DD1V2S} is maximum 600mA (not tested) at the specified total ionizing dose.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

a. T_J = +125°C. To ensure junction temperature (T_J) is maintained at a minimum of 125°C during life test, the ambient temperature shall be controlled.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition B and as specified herein.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test 4 devices with zero failures. ASTM F1192 or JESD57 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 10^7 ions/cm^2.

c. The flux shall be maximum10^5 ions/cm^2/s.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be between +85°C. and the maximum rated operating junction temperature +125°C for the latch-up measurements.

f. Bias conditions shall be defined as per Table IB.

4.4.5 Additional criteria for conformance inspection. All required conformance inspection for devices built with case outline Z are processed without the solder column attachment

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Design characteristics. The complexity of the devices covered by this document, will require the user/designer to be familiar with additional design characteristics of the device. Contact the manufacturer for design and functional support. Updated versions of device manufacturer’s software, device data sheet, IBIS models, and application notes may be obtain directly from device manufacturer.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 22-04-18

Approved sources of supply for SMD 5962-21204 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F2120401QXF	F8859	GR740-MSQ-CG625
5962F2120401QZC	F8859	GR740-MSQ-LG625
5962F2120401VXF	F8859	GR740-MSV-CG625
5962F2120401VZC	F8859	GR740-MSV-LG625

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F8859	ST Microelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2-FRANCE

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.