REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to MIL-PRF-38535 requirements. – LTG	01-03-23	Thomas M. Hess
B	Change AC limits in table I. – LTG	01-05-04	Thomas M. Hess
C	Add device type 02. Update boilerplate to current MIL-PRF-38535 requirements. – CFS	04-07-06	Thomas M. Hess
D	Update boilerplate to current MIL-PRF-38535 requirements. – CFS	08-11-12	Thomas M. Hess
E	Add case outline Y. - PHN	09-07-28	Thomas M. Hess
F	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	18-07-24	Thomas M. Hess
G	Update boilerplate to MIL-PRF-38535 requirements. - DRH	23-11-21	Muhammad A. Akbar

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

REV	G	G	G	G																		
SHEET	45	46	47	48																		
REV	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
SHEET	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
REV	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
00-03-03

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

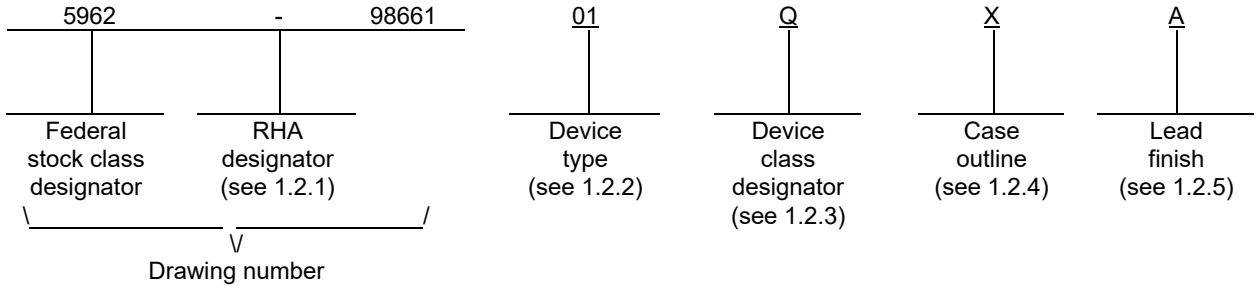
MICROCIRCUIT, DIGITAL, FLOATING-POINT DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL G	SIZE A	CAGE CODE **67268**	**5962-98661**
		SHEET	1 OF 48	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	320C6701	Floating-point digital signal processor
02	320C6701	Floating-point digital signal processor

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 2	429	Ball grid array 1/
Y	See figure 2	429	Land grid array

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Due to limitations of MIL-PRF-38535 at the time this document was prepared, this case outline is supplied using a tin lead alloy with bismuth and designated as lead finish A. The tin lead alloy described is Sn46, Pb46 and Bi8.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (CV_{DD}) ..... -0.3 V dc to +2.3 V dc
Supply voltage range (DV_{DD}) ..... -0.3 V dc to +4.0 V dc
Input voltage range (V_{IN}) ..... -0.3 V dc to +4.0 V dc
Output voltage range (V_{OUT}) ..... -0.3 V dc to +4.0 V dc
Storage temperature range ..... -55°C to +150°C
Maximum junction temperature (T_J) ..... +119°C at 140 MHz
Thermal resistance, junction-to-case (θ_{JC}) ..... 3°C/W
Solder ball reflow condition (Peak temperature) ..... +220°C ±10°C

1.4 Recommended operating conditions. 3/

Supply voltage range (CV_{DD}) ..... +1.81 V dc to +1.99 V dc
Supply voltage range (DV_{DD}) ..... +3.14 V dc to +3.46 V dc
Supply ground (V_{SS}) ..... +0.0 V dc
High level input voltage (V_{IH}) ..... 2.0 V
Low level input voltage (V_{IL}) ..... 0.8 V
High level output current (I_{OH}) ..... -12 mA
Low level output current (I_{OL}) ..... 12 mA
Case operating temperature range (T_C):
Device type 01 ..... -55°C to +115°C
Device type 02 ..... -55°C to +125°C

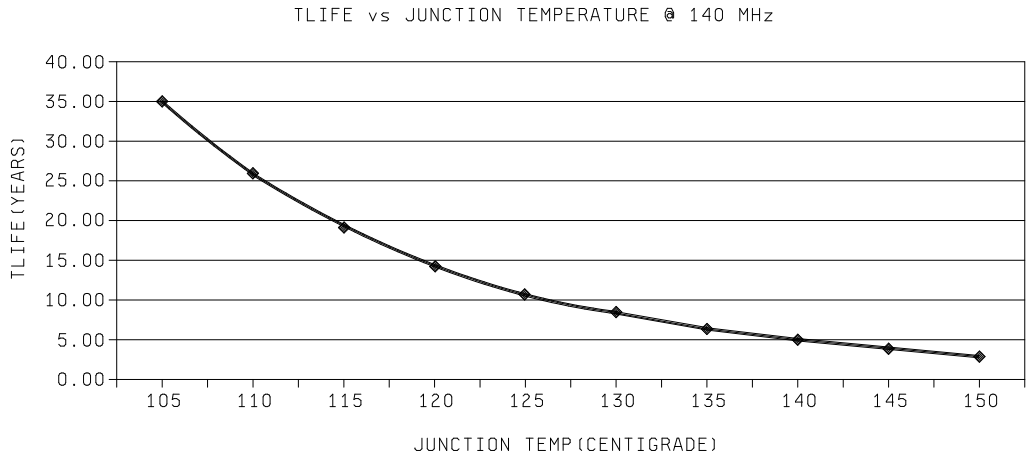


FIGURE 1. Impact of elevated temperature on device life.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltage values are with respect to V_{SS}.
3/ Extended use at maximum recommended operating temperature may result in reduction of overall device life. See figure 1 above for impact of elevated temperature on device life.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE 1149.1 - Standard Test Access Port and Boundary Scan Architecture.

(Copies of these documents are available online at https://www.ieee.org/.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 2.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.3 Block diagram(s). The block diagram(s) shall be as specified on figure 4.

3.2.4 Boundary scan instruction codes. The boundary scan instruction codes shall be as specified on figure 5.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 6.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 IEEE 1149.1 compliance. These devices shall be compliant to IEEE 1149.1.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low level output voltage	V_{OL} 2/	DV_{DD} = 3.14 V I_{OL} = 12 mA	1, 2, 3	All		0.6	V
High level output voltage	V_{OH} 2/	DV_{DD} = 3.14 V I_{OH} = -12 mA	1, 2, 3	All	2.4		V
Input current	I_{IN} 3/ 2/	V_{IN} = V_{SS} to DV_{DD}	1, 2, 3	All		±10	µA
Off-state output leakage current	I_{OZH}, I_{OZL} 2/	V_{OUT} = DV_{DD} or 0 V	1, 2, 3	All		±10	µA
Input capacitance	C_{IN}	f = 1 MHz at 0 V See 4.4.1b	4	All	10	15	pF
Output capacitance	C_{OUT}	f = 1 MHz at 0 V See 4.4.1b	4	All	10	15	pF
Functional tests	2/	CV_{DD} = 1.81 V to 1.99 V DV_{DD} = 3.14 V to 3.46 V See 4.4.1c	7,8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLKIN TIMINGS 4/							
Cycle time, CLKIN	1 2/	See figure 5, CLKMODE=x4	9, 10, 11	All	28.4		ns
		See figure 5, CLKMODE=x1			7.1		ns
Pulse duration, CLKIN high	2	See figure 5, CLKMODE=x4	9, 10, 11	All	0.4C		ns
		See figure 5, CLKMODE=x1			0.45C		ns
Pulse duration, CLKIN low	3	See figure 5, CLKMODE=x4	9, 10, 11	All	0.4C		ns
		See figure 5, CLKMODE=x1			0.45C		ns
Transition time, CLKIN	4	See figure 5, CLKMODE=x4	9, 10, 11	All		5.0	ns
		See figure 5, CLKMODE=x1				0.6	ns
CLKOUT1 TIMINGS 5/							
Cycle time, CLKOUT1	1	See figure 5, CLKMODE=x4	9, 10, 11	All	P – 0.7	P + 0.7	ns
		See figure 5, CLKMODE=x1			P – 0.7	P + 0.7	ns
Pulse duration, CLKOUT1 high	2	See figure 5, CLKMODE=x4	9, 10, 11	All	(P/2) - 0.5	(P/2) + 0.5	ns
		See figure 5, CLKMODE=x1			PH - 0.5	PH + 0.5	ns
Pulse duration, CLKOUT1 low	3	See figure 5, CLKMODE=x4	9, 10, 11	All	(P/2) - 0.5	(P/2) + 0.5	ns
		See figure 5, CLKMODE=x1			PL - 0.5	PL + 0.5	ns
Transition time, CLKOUT1	4	See figure 5, CLKMODE=x4	9, 10, 11	All		0.6	ns
		See figure 5, CLKMODE=x1				0.6	ns
CLKOUT2 TIMINGS 5/							
Cycle time, CLKOUT2	1	See figure 5	9, 10, 11	All	2P - 0.7	2P + 0.7	ns
Pulse duration, CLKOUT2 high	2		9, 10, 11	All	P – 0.7	P + 0.7	ns
Pulse duration, CLKOUT2 low	3		9, 10, 11	All	P – 0.7	P + 0.7	ns
Transition time, CLKOUT2	4		9, 10, 11	All		0.6	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
SSCLK, SDCLK, and CLKOUT2 to CLKOUT1 5/							
Delay time, CLKOUT1 edge to SSCLK edge	1 2/	See figure 5	9, 10, 11	All	-0.8	3.4	ns
Delay time, CLKOUT1 edge to SSCLK edge (1/2 clock rate)	2 2/		9, 10, 11	All	-1.0	3.0	ns
Delay time, CLKOUT1 edge to CLKOUT2 edge	3 2/		9, 10, 11	All	-1.5	2.5	ns
Delay time, CLKOUT1 edge to SDCLK edge	4 2/		9, 10, 11	All	-1.5	1.9	ns
ASYNCHRONOUS MEMORY READ and WRITE TIMING 6/ 7/							
Delay time, CLKOUT1 high to CEx valid	1 2/	See figure 5	9, 10, 11	All	-1.0	4.5	ns
Delay time, CLKOUT1 high to $\overline{BEx}$ valid	2 2/		9, 10, 11	All		4.5	ns
Delay time, CLKOUT1 high to $\overline{BEx}$ invalid	3 2/		9, 10, 11	All	-1.0		ns
Delay time, CLKOUT1 high to EAx valid	4 2/		9, 10, 11	All		4.5	ns
Delay time, CLKOUT1 high to EAx invalid	5 2/		9, 10, 11	All	-1.0		ns
Setup time, read EDx valid before CLKOUT1 high	6 2/		9, 10, 11	All	4.8		ns
Hold time, read EDx valid after CLKOUT1 high	7 2/		9, 10, 11	All	1.5		ns
Delay time, CLKOUT1 high to $\overline{AOE}$ valid	8 2/		9, 10, 11	All	-1.0	4.5	ns
Delay time, CLKOUT1 high to ARE valid	9 2/		9, 10, 11	All	-1.0	4.5	ns
Setup time, ARDY valid before CLKOUT1 high	10 2/		9, 10, 11	All	3.5		ns
Hold time, ARDY valid after CLKOUT1 high	11 2/		9, 10, 11	All	1.5		ns
Delay time, CLKOUT1 high to EDx valid	12 2/		9, 10, 11	All		4.5	ns
Delay time, CLKOUT1 high to EDx invalid	13 2/		9, 10, 11	All	-1.0		ns
Delay time, CLKOUT1 high to $\overline{AWE}$ valid	14 2/		9, 10, 11	All	-1.0	4.5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
SBSRAM READ and WRITE TIMING (Full-Rate SSCLK) 8/							
Output setup time, $\overline{CEx}$ valid before SSCLK high	1 2/	See figure 5	9, 10, 11	All	0.5P-1.5		ns
Output hold time, $\overline{CEx}$ valid after SSCLK high	2 2/		9, 10, 11	All	0.5P-2.5		ns
Output setup time, $\overline{BEx}$ valid before SSCLK high	3 2/		9, 10, 11	All	0.5P-1.6		ns
Output hold time, $\overline{BEx}$ invalid after SSCLK high	4 2/		9, 10, 11	All	0.5P-2.5		ns
Output setup time, EAx valid before SSCLK high	5 2/		9, 10, 11	All	0.5P-1.7		ns
Output hold time, EAx invalid after SSCLK high	6 2/		9, 10, 11	All	0.5P-2.5		ns
Setup time, read EDx valid before SSCLK high	7 2/		9, 10, 11	All	2.6		ns
Hold time, read EDx valid after SSCLK high	8 2/		9, 10, 11	All	1.5		ns
Output setup time, $\overline{SSADS}$ valid before SSCLK high	9 2/		9, 10, 11	All	0.5P-1.5		ns
Output hold time, $\overline{SSADS}$ valid after SSCLK high	10 2/		9, 10, 11	All	0.5P-2.5		ns
Output setup time, $\overline{SSOE}$ valid before SSCLK high	11 2/		9, 10, 11	All	0.5P-1.5		ns
Output hold time, $\overline{SSOE}$ valid after SSCLK high	12 2/		9, 10, 11	All	0.5P-2.5		ns
Output setup time, EDx valid before SSCLK high	13 2/		9, 10, 11	All	0.5P-1.5		ns
Output hold time, EDx invalid after SSCLK high	14 2/		9, 10, 11	All	0.5P-2.5		ns
Output setup time, $\overline{SSWE}$ valid before SSCLK high	15 2/		9, 10, 11	All	0.5P-1.5		ns
Output hold time, $\overline{SSWE}$ valid after SSCLK high	16 2/		9, 10, 11	All	0.5P-2.5		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
SBSRAM READ and WRITE TIMING (Half-Rate SSCLK) 9/							
Output setup time, $\overline{CE}$x valid before SSCLK high	1 2/	See figure 5	9, 10, 11	All	1.5P-5.5		ns
Output hold time, $\overline{CE}$x valid after SSCLK high	2 2/		9, 10, 11	All	0.5P-2.3		ns
Output setup time, $\overline{BE}$x valid before SSCLK high	3 2/		9, 10, 11	All	1.5P-5.5		ns
Output hold time, $\overline{BE}$x invalid after SSCLK high	4 2/		9, 10, 11	All	0.5P-2.3		ns
Output setup time, EAx valid before SSCLK high	5 2/		9, 10, 11	All	1.5P-5.5		ns
Output hold time, EAx invalid after SSCLK high	6 2/		9, 10, 11	All	0.5P-2.3		ns
Setup time, read EDx valid before SSCLK high	7 2/		9, 10, 11	All	3.8		ns
Hold time, read EDx valid after SSCLK high	8 2/		9, 10, 11	All	1.5		ns
Output setup time, $\overline{SSADS}$ valid before SSCLK high	9 2/		9, 10, 11	All	1.5P-5.5		ns
Output hold time, $\overline{SSADS}$ valid after SSCLK high	10 2/		9, 10,11	All	0.5P-2.3		ns
Output setup time, $\overline{SSOE}$ valid before SSCLK high	11 2/		9,10, 11	All	1.5P-5.5		ns
Output hold time, $\overline{SSOE}$ valid after SSCLK high	12 2/		9, 10, 11	All	0.5P-2.3		ns
Output setup time, EDx valid before SSCLK high	13 2/		9, 10, 11	All	1.5P-5.5		ns
Output hold time, EDx invalid after SSCLK high	14 2/		9, 10, 11	All	0.5P-2.3		ns
Output setup time, $\overline{SSWE}$ valid before SSCLK high	15 2/		9, 10, 11	All	1.5P-5.5		ns
Output hold time, $\overline{SSWE}$ valid after SSCLK high	16 2/		9, 10, 11	All	0.5P-2.3		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
SYNCHRONOUS DRAM TIMING 9/							
Output setup time, $\overline{CE}$x valid before SDCLK high	1 2/	See figure 5	9, 10, 11	All	1.5P-5.0		ns
Output hold time, $\overline{CE}$x valid after SDCLK high	2 2/		9, 10, 11	All	0.5P-1.9		ns
Output setup time $\overline{BE}$x valid before SDCLK high	3 2/		9, 10, 11	All	1.5P-5.0		ns
Output hold time, $\overline{BE}$x invalid after SDCLK high	4 2/		9, 10, 11	All	0.5P-1.9		ns
Output setup time, EAx valid before SDCLK high	5 2/		9, 10, 11	All	1.5P-5.0		ns
Output hold time, EAx invalid after SDCLK high	6 2/		9, 10, 11	All	0.5P-1.9		ns
Setup time, read EDx valid before SDCLK high	7 2/		9, 10, 11	All	2.0		ns
Hold time, read EDx valid after SDCLK high	8 2/		9, 10, 11	All	3.0		ns
Output setup time, $\overline{SDCAS}$ valid before SDCLK high	9 2/		9, 10, 11	All	1.5P-5.0		ns
Output hold time, $\overline{SDCAS}$ valid after SDCLK high	10 2/		9, 10, 11	All	0.5P-1.9		ns
Output setup time, EDx valid before SDCLK high	11 2/		9, 10, 11	All	1.5P-5.0		ns
Output hold time, EDx invalid after SDCLK high	12 2/		9, 10, 11	All	0.5P-1.9		ns
Output setup time, $\overline{SDWE}$ valid before DCLK high	13 2/		9, 10, 11	All	1.5P-5.0		ns
Output hold time, $\overline{SDWE}$ valid after SDCLK high	14 2/		9, 10, 11	All	0.5P-1.9		ns
Output setup time, SDA10 valid before SDCLK high	15 2/		9, 10, 11	All	1.5P-5.0		ns
Output hold time, SDA10 invalid after SDCLK high	16 2/		9, 10, 11	All	0.5P-1.9		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
SYNCHRONOUS DRAM TIMING - Continued 9/							
Output setup time, $\overline{SDRAS}$ valid before SDCLK high	17 2/	See figure 5	9, 10, 11	All	1.5P-5.0		ns
Output hold time, $\overline{SDRAS}$ valid after SDCLK high	18 2/		9, 10, 11	All	0.5P-1.9		ns
$\overline{HOLD}$/$\overline{HOLDA}$ TIMING 10/ 11/							
Setup time, $\overline{HOLD}$ high before CLKOUT1 high	1 2/	See figure 5	9, 10, 11	All	5.0		ns
Hold time, $\overline{HOLD}$ low after CLKOUT1 high	2 2/		9, 10, 11	All	2.0		ns
Response time, $\overline{HOLD}$ low to EMIF Bus high impedance	3 2/		9, 10, 11	All	4P		ns
Response time, EMIF Bus high impedance to $\overline{HOLDA}$ low	4 2/		9, 10, 11	All		2P	ns
Response time, $\overline{HOLD}$ high to $\overline{HOLDA}$ high	5 2/		9, 10, 11	All	4P	7P	ns
Delay time, CLKOUT1 high to $\overline{HOLDA}$ valid	6 2/		9, 10, 11	All	1.0	8.0	ns
Delay time, CLKOUT1 high to EMIF Bus high impedance	7		9, 10, 11	All	1.0	8.0	ns
Delay time, CLKOUT1 high to EMIF Bus low impedance	8		9, 10, 11	All	1.0	12.0	ns
Response time, $\overline{HOLD}$ high to EMIF Bus low impedance	9 2/		9, 10, 11	All	3P	6P	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
RESET TIMING							
Width of the $\overline{\text{RESET}}$ pulse (PLL stable) 12/	1	See figure 5	9, 10, 11	All	10		CLKOUT1 cycles
Width of the $\overline{\text{RESET}}$ pulse (PLL needs to sync up) 13/					250		μs
Response time to change of value in $\overline{\text{RESET}}$ signal	2		9, 10, 11	All	1		CLKOUT1 cycles
Delay time, CLKOUT1 high to CLKOUT2 invalid	3		9, 10, 11	All	-1.0		ns
Delay time, CLKOUT1 high to CLKOUT2 valid	4		9, 10, 11	All		10	ns
Delay time, CLKOUT1 high to SDCLK invalid	5		9, 10, 11	All	-1.0		ns
Delay time, CLKOUT1 high to SDCLK valid	6		9, 10, 11	All		10	ns
Delay time, CLKOUT1 high to SSCLK invalid	7		9, 10, 11	All	-1.0		ns
Delay time, CLKOUT1 high to SSCLK valid	8		9, 10, 11	All		10	ns
Delay time, CLKOUT1 high to low group invalid	9		9, 10, 11	All	-1.0		ns
Delay time, CLKOUT1 high to low group valid	10		9, 10, 11	All		10	ns
Delay time, CLKOUT1 high to high group invalid	11		9, 10, 11	All	-1.0		ns
Delay time, CLKOUT1 high to high group valid	12		9, 10, 11	All		10	ns
Delay time, CLKOUT1 high to Z group high impedance	13		9, 10, 11	All	-1.0		ns
Delay time, CLKOUT1 high to Z group valid	14		9, 10, 11	All		10	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
INTERRUPT TIMING 14/ 15/ 16/							
Response time, EXT_INTx high to IACK high	1 2/	See figure 5	9, 10, 11	All	9P		ns
Width of the interrupt pulse low	2		9, 10, 11	All	2P		ns
Width of the interrupt pulse high	3		9, 10, 11	All	2P		ns
Delay time, CLKOUT2 low to IACK valid.	4 2/		9, 10, 11	All	-0.5P	13-0.5P	ns
Delay time, CLKOUT2 low to INUMx valid	5 2/		9, 10, 11	All		10-0.5P	ns
Delay time, CLKOUT2 low to INUMx invalid	6 2/		9, 10, 11	All	-0.5P		ns
HOST-PORT INTERFACE (HPI) READ and WRITE TIMING 17/ 18/ 19/ 20/ 21/							
Setup time, select signals valid before $\overline{\text{HSTROBE}}$ low	1 2/	See figure 5	9, 10, 11	All	4.0		ns
Hold time, select signals valid after $\overline{\text{HSTROBE}}$ low	2 2/		9, 10, 11	All	2.0		ns
Pulse duration $\overline{\text{HSTROBE}}$ low	3		9, 10, 11	All	2P		ns
Pulse duration $\overline{\text{HSTROBE}}$ high between consecutive accesses	4		9, 10, 11	All	2P		ns
Delay time, $\overline{\text{HCS}}$ to $\overline{\text{HRDY}}$	5 2/		9, 10, 11	All	1.0	12.0	ns
Delay time, $\overline{\text{HSTROBE}}$ low to $\overline{\text{HRDY}}$ high	6 2/		9, 10, 11	All	1.0	12.0	ns
Output hold time, HD low impedance after $\overline{\text{HSTROBE}}$ low for an HPI read	7		9, 10, 11	All	4.0		ns
Delay time, HD valid $\overline{\text{HRDY}}$ low	8		9, 10, 11	All	P-3	P+3	ns
Output hold time, HD valid after $\overline{\text{HSTROBE}}$ high	9 2/		9, 10, 11	All	3.0	12.0	ns
Setup time, select signals valid before $\overline{\text{HAS}}$ low	10 2/		9, 10, 11	All	4.0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
HOST-PORT INTERFACE (HPI) READ and WRITE TIMING 17/ 18/ 19/ 20/ 21/ - Continued							
Hold time, select signals valid after $\overline{\text{HAS}}$ low	11 2/	See figure 5	9, 10, 11	All	2.0		ns
Setup time, host data valid before $\overline{\text{HSTROBE}}$ high	12 2/		9, 10, 11	All	3.0		ns
Hold time, host data valid after $\overline{\text{HSTROBE}}$ high	13 2/		9, 10, 11	All	2.0		ns
Hold time, $\overline{\text{HSTROBE}}$ low after $\overline{\text{HRDY}}$ low. $\overline{\text{HSTROBE}}$ should not be inactivated until $\overline{\text{HRDY}}$ is active (low): otherwise, HPI writes will not complete properly.	14		9, 10, 11	All	1.0		ns
Delay time, $\overline{\text{HSTROBE}}$ high to HD high impedance	15		9, 10, 11	All	3.0	12.0	ns
Delay time, $\overline{\text{HSTROBE}}$ low to HD valid	16 2/		9, 10, 11	All	3.0	12.0	ns
Delay time, $\overline{\text{HSTROBE}}$ high to $\overline{\text{HRDY}}$ high	17 2/		9, 10, 11	All	1.0	12.0	ns
Setup time, $\overline{\text{HAS}}$ low before $\overline{\text{HSTROBE}}$ low	18		9, 10, 11	All	2.0		ns
Hold time, $\overline{\text{HAS}}$ low after $\overline{\text{HSTROBE}}$ low	19		9, 10, 11	All	2.0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
MULTICHANNEL BUFFERED SERIAL PORT (McBSP) TIMING 22/ 23/							
Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input	1 2/	See figure 5	9, 10, 11	All	3.0	15.0	ns
Cycle time, CLKR/X	2	See figure 5, CLKR/X (INT)	9, 10, 11	All	2P		ns
		See figure 5, CLKR/X (EXT)			2P		
Pulse duration, CLKR/X high or CLKR/X low	3	See figure 5, CLKR/X (INT)	9, 10, 11	All	C-1.0	C+1.0	ns
		See figure 5, CLKR/X (EXT)			P-1		
Delay time, CLKR high to internal FSR valid	4	See figure 5, CLKR/X (INT)	9, 10, 11	All	-4.0	4.0	ns
Setup time, external FSR high before CLKR low	5	See figure 5, CLKR/X (INT)	9, 10, 11	All	13.0		ns
		See figure 5, CLKR/X (EXT)			4.0 2/		
Hold time, external FSR high after CLKR low	6	See figure 5, CLKR/X (INT)	9, 10, 11	All	7.0		ns
		See figure 5, CLKR/X (EXT)			4.0 2/		
Setup time, DR valid before CLKR low	7 2/	See figure 5, CLKR/X (INT)	9, 10, 11	All	10.0		ns
		See figure 5, CLKR/X (EXT)			1.0		
Hold time, DR valid after CLKR low	8 2/	See figure 5, CLKR/X (INT)	9, 10, 11	All	4.0		ns
		See figure 5, CLKR/X (EXT)			4.0		
Delay time, CLKX high to internal FSX valid	9	See figure 5, CLKR/X (INT)	9, 10, 11	All	-4.0 2/	5.0 2/	ns
		See figure 5, CLKR/X (EXT)			3.0	16.0	
Setup time, external FSX high before CLKX low	10	See figure 5, CLKR/X (INT)	9, 10, 11	All	13.0		ns
		See figure 5, CLKR/X (EXT)			4.0 2/		
Hold time external FSX high after CLKX low	11	See figure 5, CLKR/X (INT)	9, 10, 11	All	7.0		ns
		See figure 5, CLKR/X (EXT)			3.0 2/		
Disable time, DX high impedance following last data bit from CLKX high	12	See figure 5, CLKR/X (INT)	9, 10, 11	All	-3.0	2.0	ns
		See figure 5, CLKR/X (EXT)			2.0	9.0	
Delay time, CLKX high to DX valid	13 2/	See figure 5, CLKR/X (INT)	9, 10, 11	All	-2.0	4.0	ns
		See figure 5, CLKR/X (EXT)			3.0	16.0	
Delay time, FSX high to DX valid ONLY applies when in data delay 0 mode (XDATDLY = 00b)	14	See figure 5, FSX (INT)	9, 10, 11	All	-2.0	4.0	ns
		See figure 5, FSX (EXT)			2.0	10.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
FSR TIMING When GSYNC = 1							
Setup time, FSR high before CLKS high	1	See figure 5	9, 10, 11	All	4.0		ns
Hold time, FSR high after CLKS high	2		9, 10, 11	All	4.0		ns
McBSP TIMING as SPI MASTER or SLAVE: CLKSTP = 10b, CLKXP = 0		24/					
Hold time, FSX low after CLKX low	1 2/ 25/	See figure 5, Master 27/ See figure 5, Slave	9, 10, 11	All	T-4	T+4	ns
Delay time, FSX low to CLKX high	2 2/ 26/	See figure 5, Master 27/ See figure 5, Slave	9, 10, 11	All	L-4	L+4	ns
Delay time, CLKX high to DX valid	3 2/	See figure 5, Master 27/ See figure 5, Slave	9, 10, 11	All	-4.0 3P+1	4.0 5P+17	ns
Setup time, DR valid before CLKX low	4 2/	See figure 5, Master See figure 5, Slave	9, 10, 11	All	12.0 2-3P		ns
Hold time, DR valid after CLKX low	5 2/	See figure 5, Master See figure 5, Slave	9, 10, 11	All	4.0 5+6P		ns
Disable time, DX high impedance following last data bit from CLKX low	6	See figure 5, Master 27/ See figure 5, Slave	9, 10, 11	All	L-2	L+3	ns
Disable time, DX high impedance following last data bit from FSX high	7	See figure 5, Master 27/ See figure 5, Slave	9, 10, 11	All P+4		3P+17	ns
Delay time, FSX low to DX valid	8 2/	See figure 5, Master 27/ See figure 5, Slave	9, 10, 11	All	2P+1	4P+13	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
McBSP TIMING as SPI MASTER or SLAVE: CLKSTP = 11b, CLKXP = 0 24/							
Hold time, FSX low after CLKX low	1 2/ 25/	See figure 5, Master 27/	9, 10, 11	All	L-4	L+4	ns
		See figure 5, Slave					
Delay time, FSX low to CLKX high	2 2/ 26/	See figure 5, Master 27/	9, 10, 11	All	T-4	T+4	ns
		See figure 5, Slave					
Delay time, CLKX low to DX valid	3 2/	See figure 5, Master 27/	9, 10, 11	All	-4.0	4.0	ns
		See figure 5, Slave			3P+1	5P+17	
Setup time, DR valid before CLKX high	4 2/	See figure 5, Master	9, 10, 11	All	12.0		ns
		See figure 5, Slave			2-3P		
Hold time, DR valid after CLKX high	5 2/	See figure 5, Master	9, 10, 11	All	4.0		ns
		See figure 5, Slave			5+6P		
Disable time, DX high impedance following last data bit from CLKX low	6	See figure 5, Master 27/	9, 10, 11	All	2.0	4.0	ns
		See figure 5, Slave			3P+4	5P+17	
Delay time, FSX low to DX valid	7	See figure 5, Master 27/	9, 10, 11	All	H-2	H+3	ns
		See figure 5, Slave			2P+1 2/	4P+13 2/	
McBSP TIMING as SPI MASTER or SLAVE: CLKSTP = 10b, CLKXP = 1 24/							
Hold time, FSX low after CLKX high	1 2/ 25/	See figure 5, Master 27/	9, 10, 11	All	T-4	T+4	ns
		See figure 5, Slave					
Delay time, FSX low to CLKX low	2 2/ 26/	See figure 5, Master 27/	9, 10, 11	All	H-4	H+4	ns
		See figure 5, Slave					
Delay time, CLKX low to DX valid	3 2/	See figure 5, Master 27/	9, 10, 11	All	-4.0	4.0	ns
		See figure 5, Slave			3P+1	5P+17	
Setup time, DR valid before CLKX high	4 2/	See figure 5, Master	9, 10, 11	All	12.0		ns
		See figure 5, Slave			2-3P		
Hold time, DR valid after CLKX high	5 2/	See figure 5, Master	9, 10, 11	All	4.0		ns
		See figure 5, Slave			5+6P		
Disable time, DX high impedance following last data bit from CLKX high	6	See figure 5, Master 27/	9, 10, 11	All	H-2	H+3	ns
		See figure 5, Slave					
Disable time, DX high impedance following last data bit from FSX high	7	See figure 5, Master 27/	9, 10, 11	All			ns
		See figure 5, Slave			P+4	3P+17	
Delay time, FSX low to DX valid	8 2/	See figure 5, Master 27/	9, 10, 11	All			ns
		See figure 5, Slave			2P+1	4P+13	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
McBSP TIMING as SPI MASTER or SLAVE: CLKSTP = 11b, CLKXP = 1 24/							
Hold time, FSX low after CLKX high	1 2/ 25/	See figure 5, Master 27/	9, 10, 11	All	H-4	H+4	ns
		See figure 5, Slave					
Delay time, FSX low to CLKX low	2 2/ 26/	See figure 5, Master 27/	9, 10, 11	All	T-4	T+4	ns
		See figure 5, Slave					
Delay time, CLKX high to DX valid	3 2/	See figure 5, Master 27/	9, 10, 11	All	-4.0	4.0	ns
		See figure 5, Slave			3P+1	5P+17	
Setup time, DR valid before CLKX low	4 2/	See figure 5, Master	9, 10, 11	All	12.0		ns
		See figure 5, Slave			2-3P		
Hold time, DR valid after CLKX low	5 2/	See figure 5, Master	9, 10, 11	All	4.0		ns
		See figure 5, Slave			5+6P		
Disable time, DX high impedance following last data bit from CLKX high	6	See figure 5, Master 27/	9, 10, 11	All	-2.0	4.0	ns
		See figure 5, Slave			3P+4	5P+17	
Delay time, FSX low to DX valid	7	See figure 5, Master 27/	9, 10, 11	All	L-2	L+4	ns
		See figure 5, Slave			2P+1 2/	4P+13 2/	
DMAC TIMING							
Delay time, CLKOUT1 high to DMAC valid	1 2/	See figure 5	9, 10, 11	All	2.0	11.0 2/	ns
TIMER TIMING							
Pulse duration, TINP high or low	1 2/	See figure 5	9, 10, 11	All	2P		ns
Delay time, CLKOUT1 high to TOUT valid	2 2/		9, 10, 11	All	1.0	10.0	ns
POWER-DOWN TIMING							
Delay time, CLKOUT1 high to PD valid	1 2/	See figure 5	9, 10, 11	All	1.0	9.0	ns
JTAG TEST-PORT TIMING							
Cycle time, TCK	1 2/	See figure 5	9, 10, 11	All	35.0		ns
Delay time, TCK low to TDO valid	2		9, 10, 11	All	-3.0	15.0	ns
Setup time, TDI/TMS/ $\overline{\text{TRST}}$ valid before TCK high	3 2/		9, 10, 11	All	10.0		ns
Hold time, TDI/TMS/ $\overline{\text{TRST}}$ valid after TCK high	4 2/		9, 10, 11	All	9.0		ns

See footnotes on next page.

TABLE I. Electrical performance characteristics - Continued.

1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Unless otherwise specified, the operating temperature range for device type 01 is -55°C to +115°C, and the operating temperature range for device type 02 is -55°C to +125°C. Output terminals not designated shall be either high level logic, low level logic, or open.

2/ Tested parameters.

3/ TMS and TDI are not included due to internal pullups.

4/ C = CLKIN cycle time in ns. For example, when CLKIN Frequency is 10 MHz, use C = 100 ns.

5/ P = 1/CPU clock frequency in ns. When running parts at 140 MHz, use P = 7.1 ns. PH is the high period of CLKIN in ns and PL is the low period of CLKIN in ns.

6/ To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. If ARDY does meet setup or hold time, it may be recognized in the current cycle or the next cycle. Thus, ARDY can be an asynchronous input.

7/ The minimum delay is also the minimum output hold after CLKOUT1 high.

8/ When the PLL is used (CLKMODEx4), P = 1/CPU clock frequency; when running parts at 140 MHz, use P = 7.1 ns. For CLKMODEx1, 0.5P is defined as PH (pulse duration of CLKIN high) for all output setup times; 0.5P is defined as PL (pulse duration of CLKIN low) for all output hold times.

9/ For CLKMODEx1:
1.5P = P + PH, where P=1/CPU clock frequency, and PH = pulse duration of CLKIN high.
0.5P = PL, where PL = pulse duration of CLKIN low.

10/ $\overline{\text{HOLD}}$ is synchronized internally. If setup and hold times are not met, it will either be recognized in the current cycle or in the next cycle. $\overline{\text{HOLD}}$ can be an asynchronous input.

11/ All pending EMIF transactions are allowed to complete before $\overline{\text{HOLDA}}$ is asserted. The worst cases for this is an asynchronous read or write with external ARDY used or a minimum of eight consecutive SDRAM reads or writes when RBTR8 = 1. If no bus transactions are occurring, then the minimum delay time can be achieved. The bus hold can be indefinitely delayed by setting NOHOLD = 1.

12/ This parameter applies to CLKMODEx1 when CLKIN is stable and applies to CLKMODEx4 when CLKIN and PLL are stable.

13/ This parameter only applies to CLKMODEx4. The $\overline{\text{RESET}}$ signal is not connected internally to the clock PLL circuit. The PLL, however, may need up to 250 μs to stabilize following device power up or after PLL configuration has been changed. During that time, $\overline{\text{RESET}}$ must be asserted to ensure proper device operation.

14/ Interrupt signals are synchronized internally and are potentially recognized one cycle later if setup and hold time are violated. Also they can be connected to asynchronous inputs.

15/ When the PLL is used (CLKMODEx4), 0.5P = 1/(2x CPU clock frequency).

16/ For CLKMODEx1:0.5P = PH, where PH is the high period of CLKIN.

17/ $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.

18/ $\overline{\text{HCS}}$ enables $\overline{\text{HRDY}}$, and $\overline{\text{HRDY}}$ is always low when $\overline{\text{HCS}}$ is high. The case where $\overline{\text{HRDY}}$ goes high when $\overline{\text{HCS}}$ falls indicates that HPI is busy completing a previous HPID WRITE or READ autoincrement.

19/ The effects of internal clock jitter are included at test. There is no need to adjust timing numbers for internal clock jitter.

TABLE I. Electrical performance characteristics - Continued.

20/ This parameter is used during an HPID read. At the beginning of the first half -word transfer on the falling edge of $\overline{\text{HSTROBE}}$, the HPI sends the request to the DMA auxiliary channel, and HRDY remains high until the DMA auxiliary channel loads the requested data into HPID.

21/ This parameter is used after the second half-word of an HPID write autoincrement read. $\overline{\text{HRDY}}$ remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the $\overline{\text{HRDY}}$ signal.

22/ CLKRP = CLKXP =FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

23/ Minimum delay times also represent minimum output hold times.

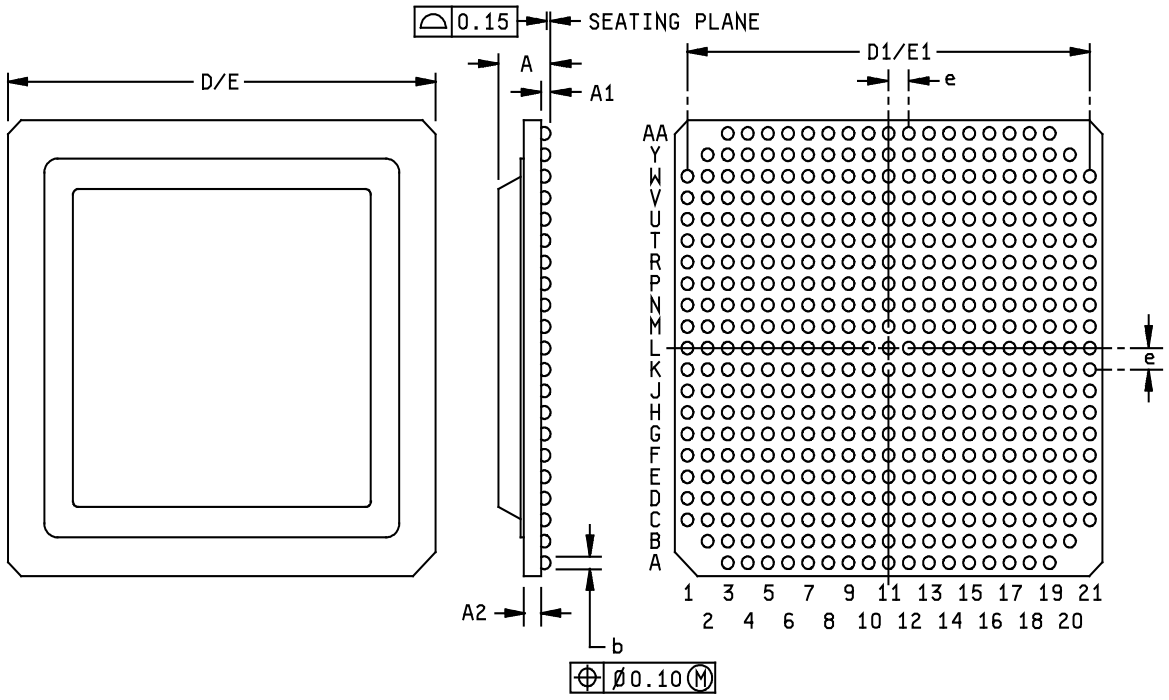
24/ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

25/ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP.
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP.

26/ FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

27/ S = sample rate generator input clock = P if CLKSM = 1 (P = 1/CPU clock frequency).
= sample rate generator input clock = P_clks if CLKSM = 0(P_clks = CLKS period).
T = CLKX period = (1 + CLKGDV)*S.
H = CLKX high pulse width = (CLKGDV/2 + 1)*S if CLKGDV is even.
= (CLKGDV + 1)2* S if CLKGDV is odd or zero.
L = CLKX low pulse width = (CLKGDV/2)*S if CLKGDV is even.
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero.

CASE X

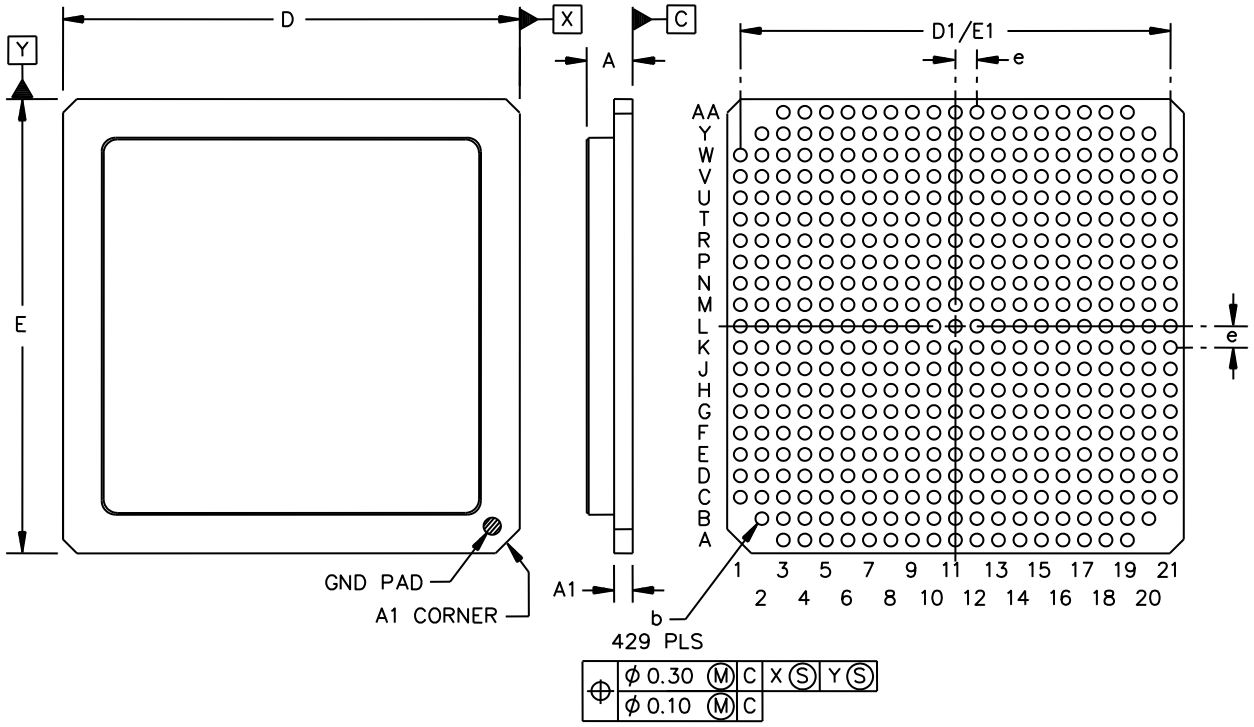


Case outline	X	
Symbol	Millimeters	
	Min	Max
A		3.30
A1	0.50	0.70
A2	1.00	1.22
b	0.60	0.90
D/E	26.80	27.20
D1/E1	25.40 BSC	
e	1.27 BSC	

NOTE: All dimensions are in Millimeters.

FIGURE 2. Case outlines.

CASE Y



Case outline	Y	
Symbol	Millimeters	
	Min	Max
A		2.70
A1	1.03	1.25
A2	0.81	0.91
b	26.80	27.20
D/E		2.70
D1/E1	25.40 BSC	
e	1.27 BSC	

NOTE: All dimensions are in Millimeters.

FIGURE 2. Case outlines - Continued.

Case outline:	X and Y				
Symbol number	Pin Symbol	Type	Symbol number	Pin Symbol	Type
A14	CLKIN	I	D8	HD2	I/O/Z
Y6	CLKOUT1	O	B7	HD1	I/O/Z
V9	CLKOUT2	O	C7	HD0	I/O/Z
B17	CLKMODE1	I	L6	HAS	I
C17	CLKMODE0	I	C5	HCS	I
C13	PLLFREQ3	I	C4	HDS1	I
G11	PLLFREQ2	I	K6	HDS2	I
F11	PLLFREQ1	I	H3	HRDY	O
D12	PLLV	A	B16	BOOTMODE4	I
G10	PLLG	A	G14	BOOTMODE3	I
C12	PLLF	A	F15	BOOTMODE2	I
K19	TMS	I	C18	BOOTMODE1	I
R12	TDO	O/Z	D17	BOOTMODE0	I
R13	TDI	I	Y5	CE3	O/Z
M20	TCK	I	V3	CE2	O/Z
N18	TRST	I	T6	CE1	O/Z
R20	EMU1	I/O/Z	U2	CE0	O/Z
T18	EMU0	I/O/Z	R8	BE3	O/Z
J20	RESET	I/O/Z	T3	BE2	O/Z
K21	NMI	I	T2	BE1	O/Z
R16	EXT_INT7	I	R2	BE0	O/Z
P20	EXT_INT6	I	L4	EA21	O/Z
R15	EXT_INT5	I	L3	EA20	O/Z
R18	EXT_INT4	I	J2	EA19	O/Z
R11	IACK	O	J1	EA18	O/Z
T19	INUM3	O	K1	EA17	O/Z
T20	INUM2	O	K2	EA16	O/Z
T14	INUM1	O	L2	EA15	O/Z
T16	INUM0	O	L1	EA14	O/Z
G20	LENDIAN	I	M1	EA13	O/Z
D19	PD	O	M2	EA12	O/Z
H2	HINT	O/Z	M6	EA11	O/Z
J6	HCNTL1	I	N4	EA10	O/Z
H6	HCNTL0	I	N1	EA9	O/Z
E4	HHWIL	I	N2	EA8	O/Z
G6	HBE1	I	N6	EA7	O/Z
F6	HBE0	I	P4	EA6	O/Z
D4	HR/W	I	P3	EA5	O/Z
D11	HD15	I/OZ	P2	EA4	O/Z
B11	HD14	I/O/Z	P1	EA3	O/Z
A11	HD13	I/O/Z	P6	EA2	O/Z
G9	HD12	I/O/Z	U18	ED31	I/O/Z
D10	HD11	I/O/Z	U20	ED30	I/O/Z
A10	HD10	I/O/Z	T15	ED29	I/O/Z
C10	HD9	I/O/Z	V18	ED28	I/O/Z
B9	HD8	I/O/Z	V17	ED27	I/O/Z
F9	HD7	I/O/Z	V16	ED26	I/O/Z
C9	HD6	I/O/Z	T12	ED25	I/O/Z
A9	HD5	I/O/Z	W17	ED24	I/O/Z
B8	HD4	I/O/Z	T13	ED23	I/O/Z
D9	HD3	I/O/Z	Y17	ED22	I/O/Z

I = Input, O = Output, Z = High Impedance, S = Supply voltage, GND = Ground.
PPLV and PLLG signals are not part of external voltage supply or ground. See the CLOCK/PLL documentation for information on how to connect those pins. A = Analog Signal (PLL Filter).

FIGURE 3. Terminal connections.

Case outline:	X and Y				
Symbol number	Pin Symbol	Type	Symbol number	Pin Symbol	Type
T11	ED21	I/O/Z	F4	CLKS1	I
Y16	ED20	I/O/Z	H4	CLKR1	I/O/Z
W15	ED19	I/OZ	J4	CLKX1	I/O/Z
V14	ED18	I/O/Z	E2	DR1	I
Y15	ED17	I/O/Z	G4	DX1	O/Z
R9	ED16	I/O/Z	F3	FSR1	I/O/Z
Y14	ED15	I/O/Z	F2	FSX1	I/O/Z
V13	ED14	I/O/Z	K18	CLKS0	I
AA13	ED13	I/O/Z	L21	CLKR0	I/O/Z
T10	ED12	I/O/Z	K20	CLKX0	I/O/Z
Y13	ED11	I/O/Z	J21	DR0	I
W12	ED10	I/O/Z	M21	DX0	O/Z
Y12	ED9	I/O/Z	P16	FSR0	I/O/Z
Y11	ED8	I/O/Z	N16	FSX0	I/O/Z
V10	ED7	I/O/Z	N21	RSV0	I
AA10	ED6	I/O/Z	K16	RSV1	I
Y10	ED5	I/O/Z	B13	RSV2	I
W10	ED4	I/O/Z	B14	RSV3	I
Y9	ED3	I/O/Z	F13	RSV4	I
AA9	ED2	I/O/Z	C15	RSV5	O
Y8	ED1	I/O/Z	F7	RSV6	I
W9	ED0	I/O/Z	D7	RSV7	I
R7	$\overline{\text{ARE}}$	O/Z	B5	RSV8	I
T7	$\overline{\text{AOE}}$	O/Z	F16	RSV9	O
V5	$\overline{\text{AWE}}$	O/Z	C14	DV_{DD}	S
R4	ARDY	I	C8	DV_{DD}	S
V8	$\overline{\text{SSADS}}$	O/Z	E19	DV_{DD}	S
W7	$\overline{\text{SSOE}}$	O/Z	E3	DV_{DD}	S
Y7	$\overline{\text{SSWE}}$	O/Z	H11	DV_{DD}	S
AA8	SSCLK	O/Z	H13	DV_{DD}	S
V7	SDA10	O/Z	H9	DV_{DD}	S
V6	$\overline{\text{SDRAS}}$	O/Z	J10	DV_{DD}	S
W5	$\overline{\text{SDCAS}}$	O/Z	J12	DV_{DD}	S
T8	$\overline{\text{SDWE}}$	O/Z	J14	DV_{DD}	S
T9	SDCLK	O/Z	J19	DV_{DD}	S
R6	HOLD	I	J3	DV_{DD}	S
B15	HOLDA	O	J8	DV_{DD}	S
G2	TOUT1	O/Z	K11	DV_{DD}	S
K3	TINP1	I	K13	DV_{DD}	S
M18	TOUT0	O/Z	K15	DV_{DD}	S
J18	TINP0	I	K7	DV_{DD}	S
E18	DMAC3	O	K9	DV_{DD}	S
F19	DMAC2	O	L10	DV_{DD}	S
E20	DMAC1	O	L12	DV_{DD}	S
G16	DMAC0	O	L14	DV_{DD}	S
			L8	DV_{DD}	S

I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground
DV_{DD} = 3.3 V supply voltage

FIGURE 3. Terminal connections - Continued.

Case outline:	X and Y				
Symbol number	Pin Symbol	Type	Symbol number	Pin Symbol	Type
M11	DV_{DD}	S	C3	CV_{DD}	S
M13	DV_{DD}	S	C20	CV_{DD}	S
M15	DV_{DD}	S	D2	CV_{DD}	S
M7	DV_{DD}	S	D21	CV_{DD}	S
M9	DV_{DD}	S	E1	CV_{DD}	S
N0	DV_{DD}	S	E6	CV_{DD}	S
N12	DV_{DD}	S	E8	CV_{DD}	S
N14	DV_{DD}	S	E10	CV_{DD}	S
N19	DV_{DD}	S	E12	CV_{DD}	S
N3	DV_{DD}	S	E14	CV_{DD}	S
N8	DV_{DD}	S	E16	CV_{DD}	S
P11	DV_{DD}	S	F5	CV_{DD}	S
P13	DV_{DD}	S	F17	CV_{DD}	S
P9	DV_{DD}	S	F21	CV_{DD}	S
U19	DV_{DD}	S	G1	CV_{DD}	S
U3	DV_{DD}	S	H5	CV_{DD}	S
W14	DV_{DD}	S	H17	CV_{DD}	S
W8	DV_{DD}	S	K5	CV_{DD}	S
A12	CV_{DD}	S	K17	CV_{DD}	S
A13	CV_{DD}	S	M5	CV_{DD}	S
B10	CV_{DD}	S	M17	CV_{DD}	S
B12	CV_{DD}	S	P5	CV_{DD}	S
B6	CV_{DD}	S	P17	CV_{DD}	S
D15	CV_{DD}	S	R21	CV_{DD}	S
D16	CV_{DD}	S	T1	CV_{DD}	S
F10	CV_{DD}	S	T5	CV_{DD}	S
F14	CV_{DD}	S	T17	CV_{DD}	S
F8	CV_{DD}	S	U6	CV_{DD}	S
G13	CV_{DD}	S	U8	CV_{DD}	S
G7	CV_{DD}	S	U10	CV_{DD}	S
G8	CV_{DD}	S	U12	CV_{DD}	S
K4	CV_{DD}	S	U14	CV_{DD}	S
M3	CV_{DD}	S	U16	CV_{DD}	S
M4	CV_{DD}	S	U21	CV_{DD}	S
A3	CV_{DD}	S	V1	CV_{DD}	S
A5	CV_{DD}	S	V20	CV_{DD}	S
A7	CV_{DD}	S	W2	CV_{DD}	S
A16	CV_{DD}	S	W19	CV_{DD}	S
A18	CV_{DD}	S	W21	CV_{DD}	S
AA4	CV_{DD}	S	Y3	CV_{DD}	S
AA6	CV_{DD}	S	Y18	CV_{DD}	S
AA15	CV_{DD}	S	Y20	CV_{DD}	S
AA17	CV_{DD}	S	AA11	CV_{DD}	S
AA19	CV_{DD}	S	AA12	CV_{DD}	S
B2	CV_{DD}	S	F20	CV_{DD}	S
B4	CV_{DD}	S	G18	CV_{DD}	S
B19	CV_{DD}	S	H16	CV_{DD}	S
C1	CV_{DD}	S			

I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground
DV_{DD} = 3.3 V supply voltage, CV_{DD} = 1.9 V supply voltage

FIGURE 3. Terminal connections - Continued.

Case outline:	X and Y				
Symbol number	Pin Symbol	Type	Symbol number	Pin Symbol	Type
H18	CV_{DD}	S	AA18	V_{SS}	GND
L18	CV_{DD}	S	B3	V_{SS}	GND
L19	CV_{DD}	S	B18	V_{SS}	GND
L20	CV_{DD}	S	B20	V_{SS}	GND
N20	CV_{DD}	S	C2	V_{SS}	GND
P18	CV_{DD}	S	C19	V_{SS}	GND
P19	CV_{DD}	S	C21	V_{SS}	GND
R10	CV_{DD}	S	D1	V_{SS}	GND
R14	CV_{DD}	S	D20	V_{SS}	GND
U4	CV_{DD}	S	E5	V_{SS}	GND
V11	CV_{DD}	S	E7	V_{SS}	GND
V12	CV_{DD}	S	E9	V_{SS}	GND
V15	CV_{DD}	S	E11	V_{SS}	GND
W13	CV_{DD}	S	E13	V_{SS}	GND
C11	V_{SS}	GND	E15	V_{SS}	GND
C16	V_{SS}	GND	E17	V_{SS}	GND
C6	V_{SS}	GND	E21	V_{SS}	GND
D5	V_{SS}	GND	F1	V_{SS}	GND
G3	V_{SS}	GND	G5	V_{SS}	GND
H10	V_{SS}	GND	G17	V_{SS}	GND
H12	V_{SS}	GND	G21	V_{SS}	GND
H14	V_{SS}	GND	H1	V_{SS}	GND
H7	V_{SS}	GND	J5	V_{SS}	GND
H8	V_{SS}	GND	J17	V_{SS}	GND
J11	V_{SS}	GND	L5	V_{SS}	GND
J13	V_{SS}	GND	L17	V_{SS}	GND
J7	V_{SS}	GND	N5	V_{SS}	GND
J9	V_{SS}	GND	N17	V_{SS}	GND
K8	V_{SS}	GND	P21	V_{SS}	GND
L7	V_{SS}	GND	R1	V_{SS}	GND
L9	V_{SS}	GND	R5	V_{SS}	GND
M8	V_{SS}	GND	R17	V_{SS}	GND
N7	V_{SS}	GND	T21	V_{SS}	GND
R3	V_{SS}	GND	U1	V_{SS}	GND
A4	V_{SS}	GND	U5	V_{SS}	GND
A6	V_{SS}	GND	U7	V_{SS}	GND
A8	V_{SS}	GND	U9	V_{SS}	GND
A15	V_{SS}	GND	U11	V_{SS}	GND
A17	V_{SS}	GND	U13	V_{SS}	GND
A19	V_{SS}	GND	U15	V_{SS}	GND
AA3	V_{SS}	GND	U17	V_{SS}	GND
AA5	V_{SS}	GND	V2	V_{SS}	GND
AA7	V_{SS}	GND	V21	V_{SS}	GND
AA14	V_{SS}	GND	W1	V_{SS}	GND
AA16	V_{SS}	GND	W3	V_{SS}	GND
			W20	V_{SS}	GND
			Y2	V_{SS}	GND
			Y4	V_{SS}	GND
			Y19	V_{SS}	GND

I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground
CV_{DD} = 1.9 V supply voltage

FIGURE 3. Terminal connections - Continued.

Case outline:	X and Y				
Symbol number	Pin Symbol	Type	Symbol number	Pin Symbol	Type
F18	V_{SS}	GND	D13	NC	
G19	V_{SS}	GND	D14	NC	
H15	V_{SS}	GND	D18	NC	
J15	V_{SS}	GND	D3	NC	
J16	V_{SS}	GND	D6	NC	
K10	V_{SS}	GND	F12	NC	
K12	V_{SS}	GND	G12	NC	
K14	V_{SS}	GND	G15	NC	
L11	V_{SS}	GND	H19	NC	
L13	V_{SS}	GND	H20	NC	
L15	V_{SS}	GND	H21	NC	
M10	V_{SS}	GND	L16	NC	
M12	V_{SS}	GND	M16	NC	
M14	V_{SS}	GND	M19	NC	
N11	V_{SS}	GND	V19	NC	
N13	V_{SS}	GND	V4	NC	
N15	V_{SS}	GND	W18	NC	
N9	V_{SS}	GND	W4	NC	
P10	V_{SS}	GND			
P12	V_{SS}	GND			
P14	V_{SS}	GND			
P15	V_{SS}	GND			
P7	V_{SS}	GND			
P8	V_{SS}	GND			
R19	V_{SS}	GND			
T4	V_{SS}	GND			
W11	V_{SS}	GND			
W16	V_{SS}	GND			
W6	V_{SS}	GND			

I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, NC = No connection

FIGURE 3. Terminal connections - Continued.

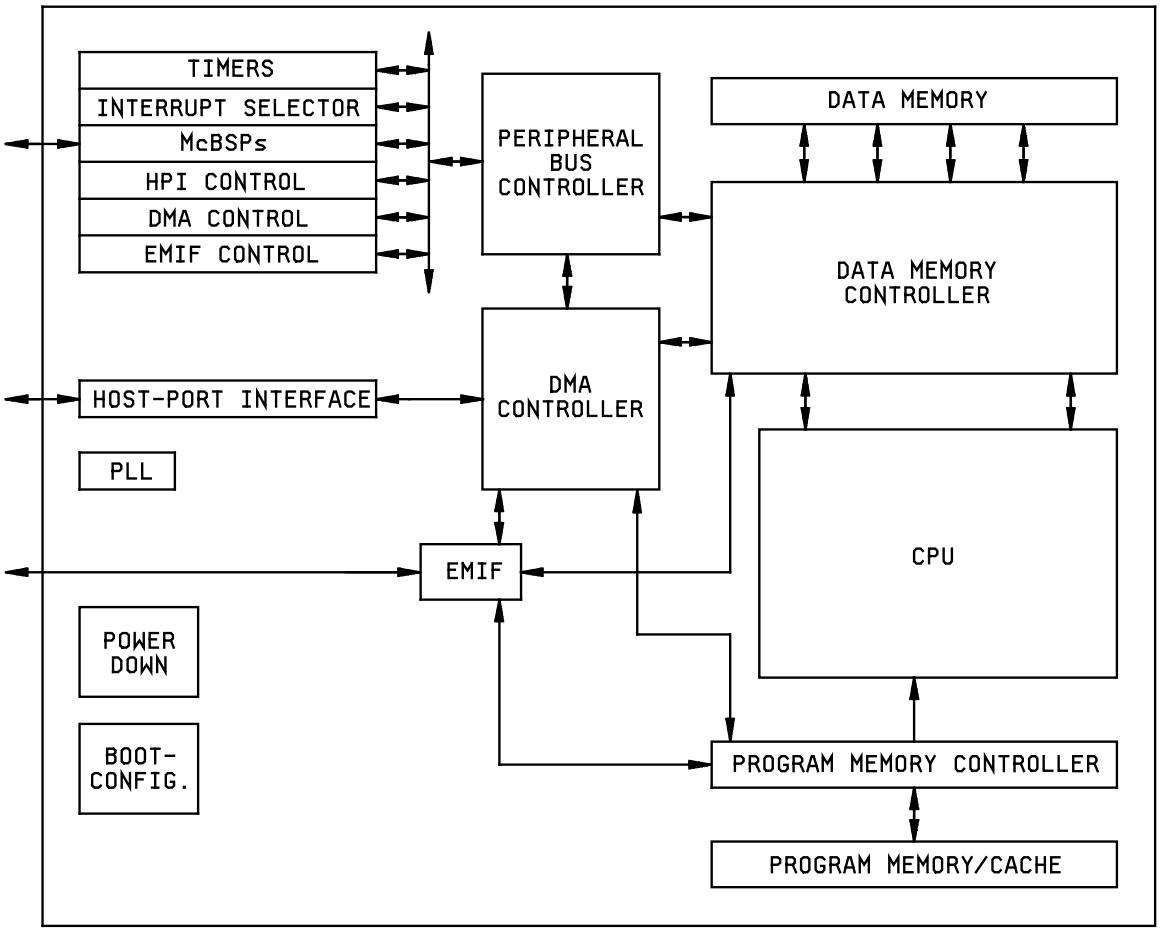
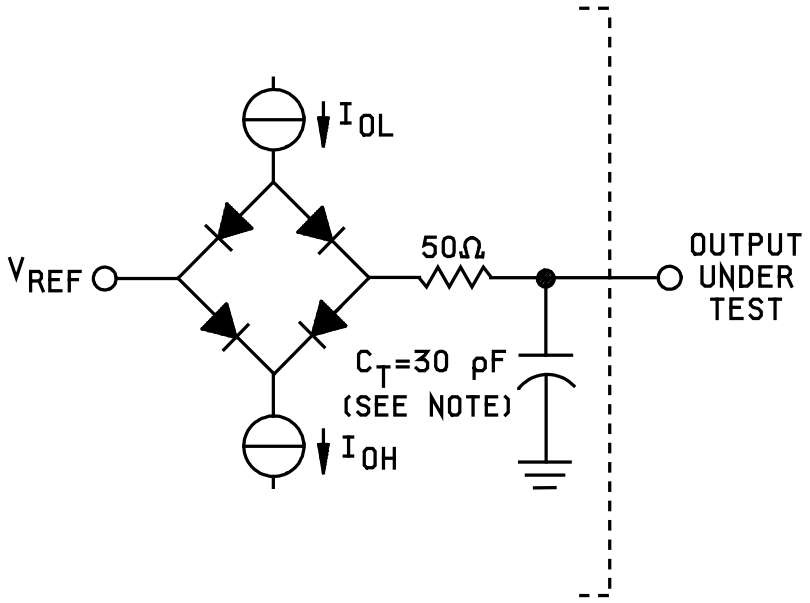


FIGURE 4. Block diagram.

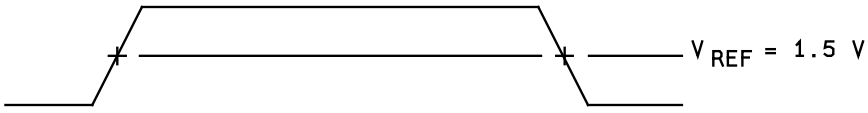
Instruction name	Instruction code
IDCODE	0100
INT_SCAN	0111
EXTEST	0000
SAMPLE	0001
BYPASS	1111

FIGURE 5. Boundary scan instruction codes.



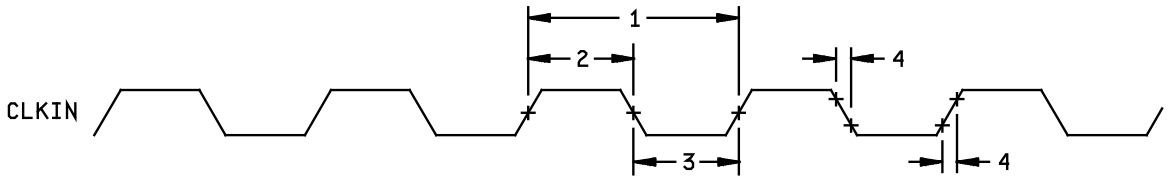
TTL-LEVEL OUTPUTS

NOTE: All input and output timing parameters are referenced to 1.5 V for both “0” and “1” logic levels.

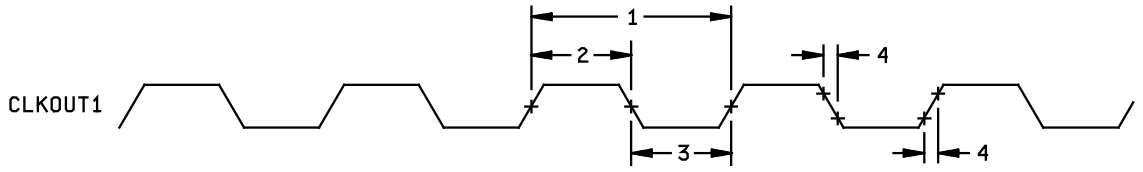


INPUT AND OUTPUT VOLTAGE REFERENCE LEVELS FOR AC TIMING MEASUREMENTS

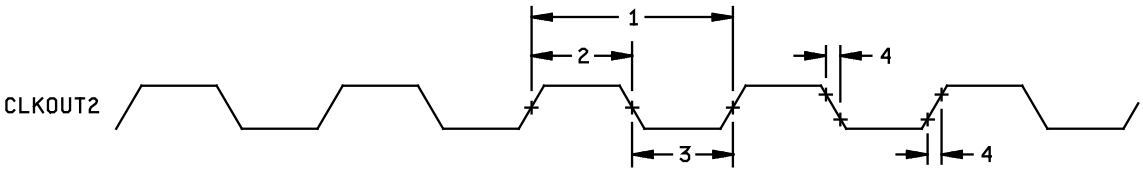
FIGURE 6. Timing waveforms.



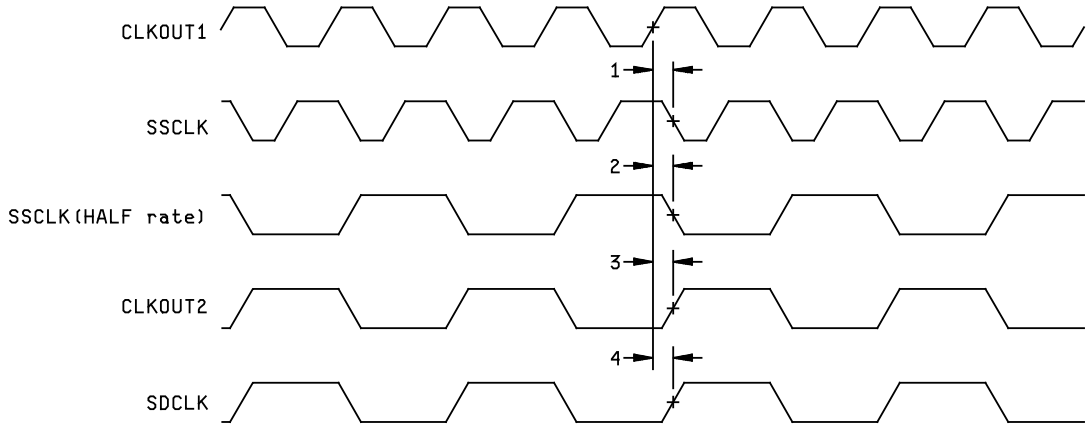
CLKIN TIMINGS



CLKOUT1 TIMINGS

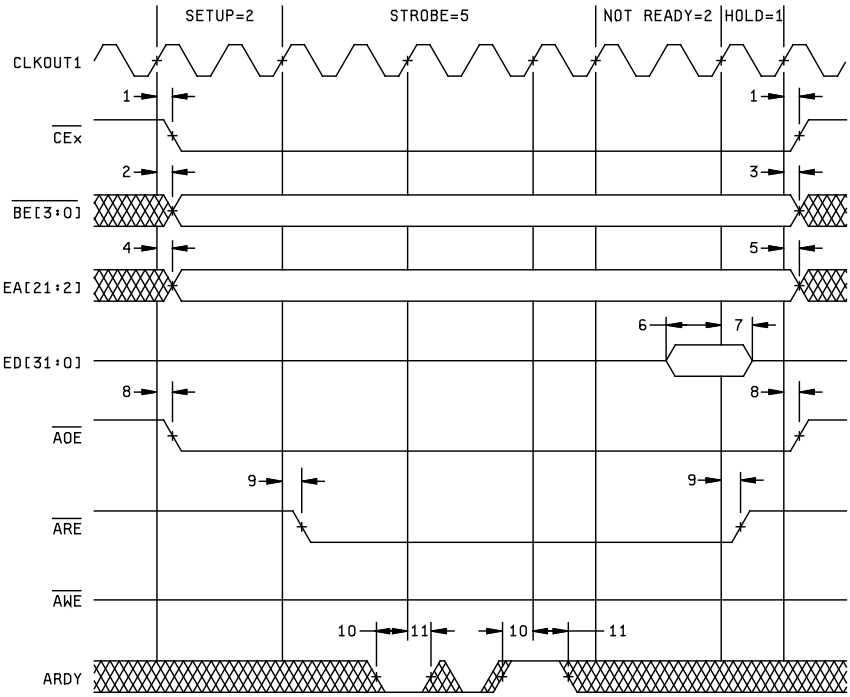


CLKOUT2 TIMINGS

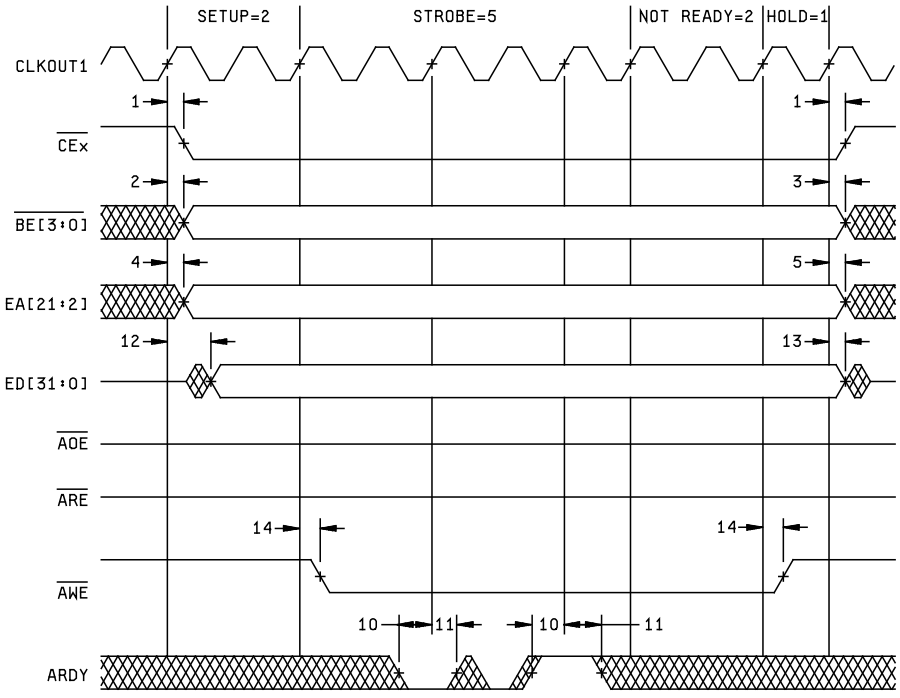


RELATION OF CLKOUT2,SDCLK,AND SSCLK TO CLKOUT1

FIGURE 6. Timing waveforms - Continued.

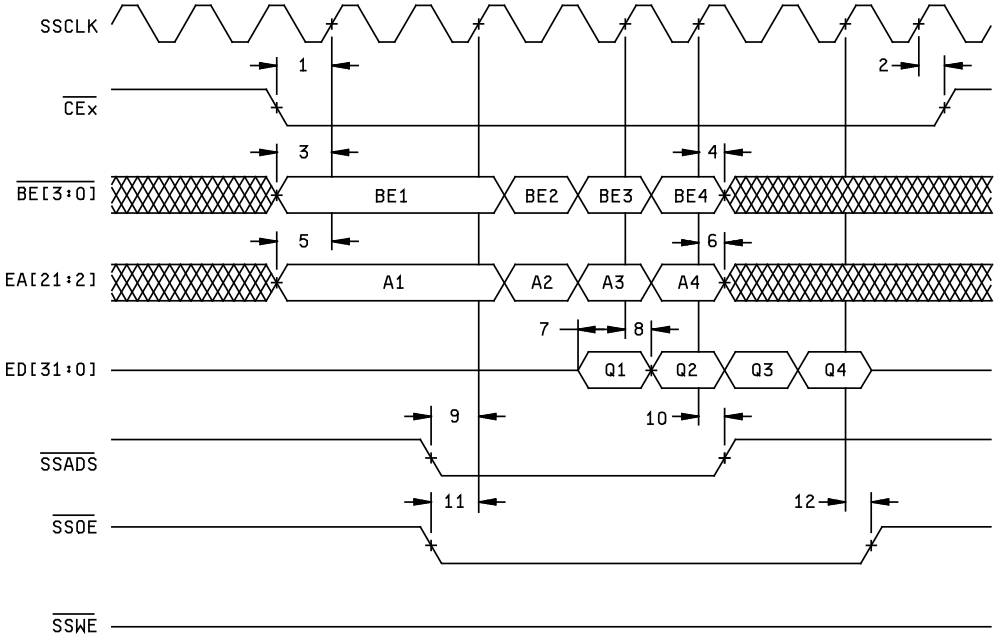


ASYNCHRONOUS MEMORY READ TIMING

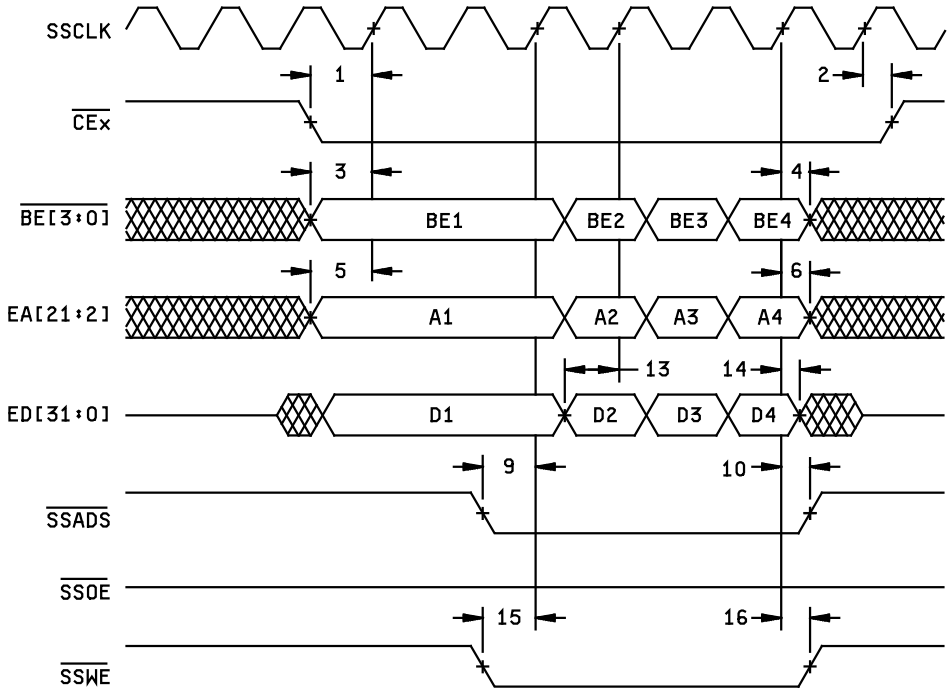


ASYNCHRONOUS MEMORY WRITE TIMING

FIGURE 6. Timing waveforms - Continued.

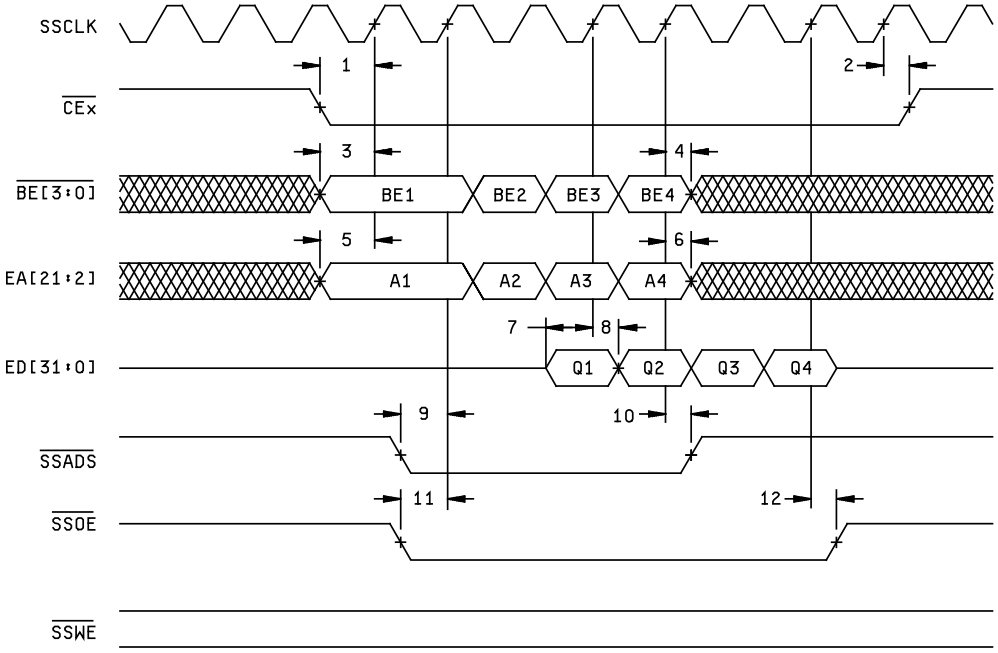


SBSRAM READ TIMING(FULL-RATE SSCLK)

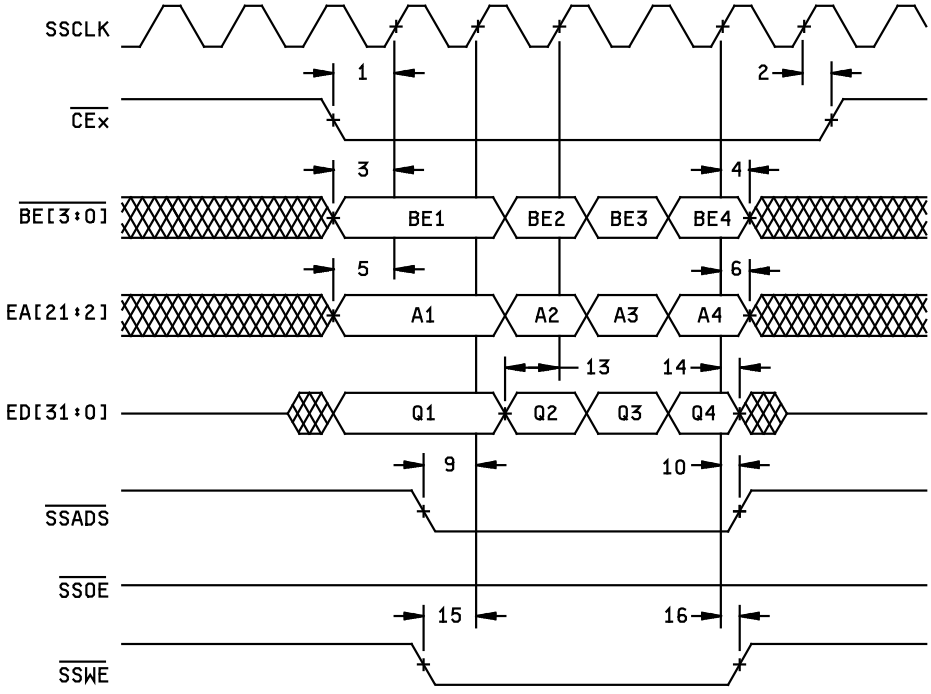


SBSRAM WRITE TIMING(FULL-RATE SSCLK)

FIGURE 6. Timing waveforms - Continued.

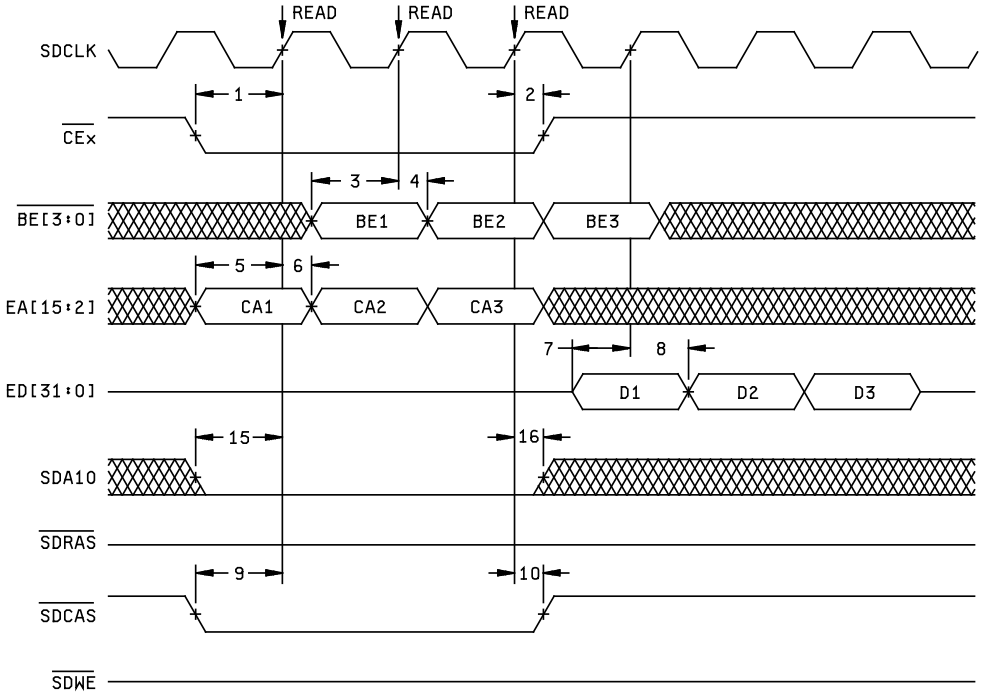


SBSRAM READ TIMING(HALF-RATE SSCLK)

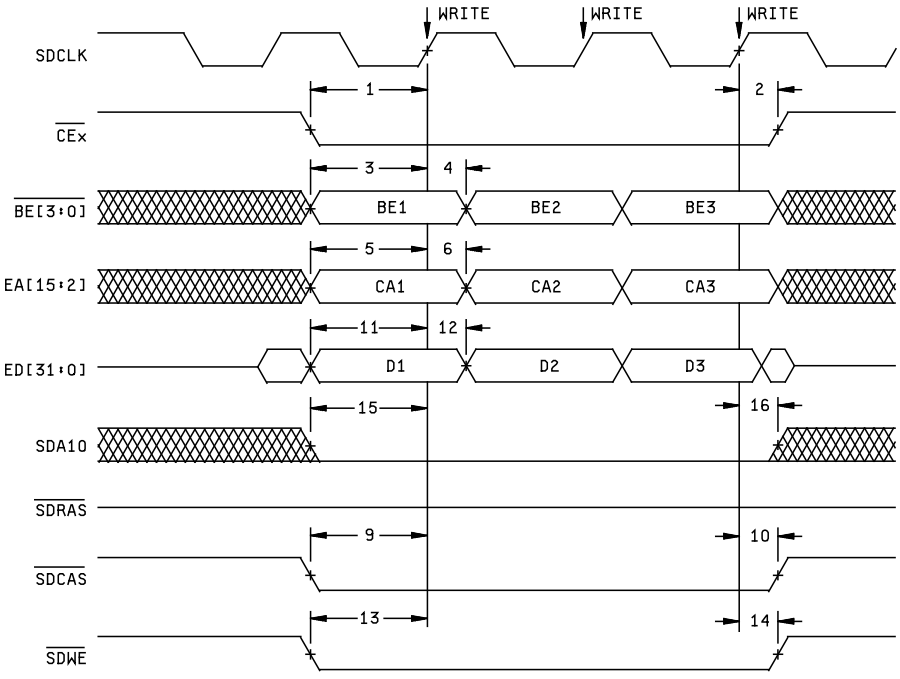


SBSRAM WRITE TIMING(HALF-RATE SSCLK)

FIGURE 6. Timing waveforms - Continued.



THREE SDRAM READ COMMANDS



THREE SDRAM WRT COMMANDS

FIGURE 6. Timing waveforms - Continued.

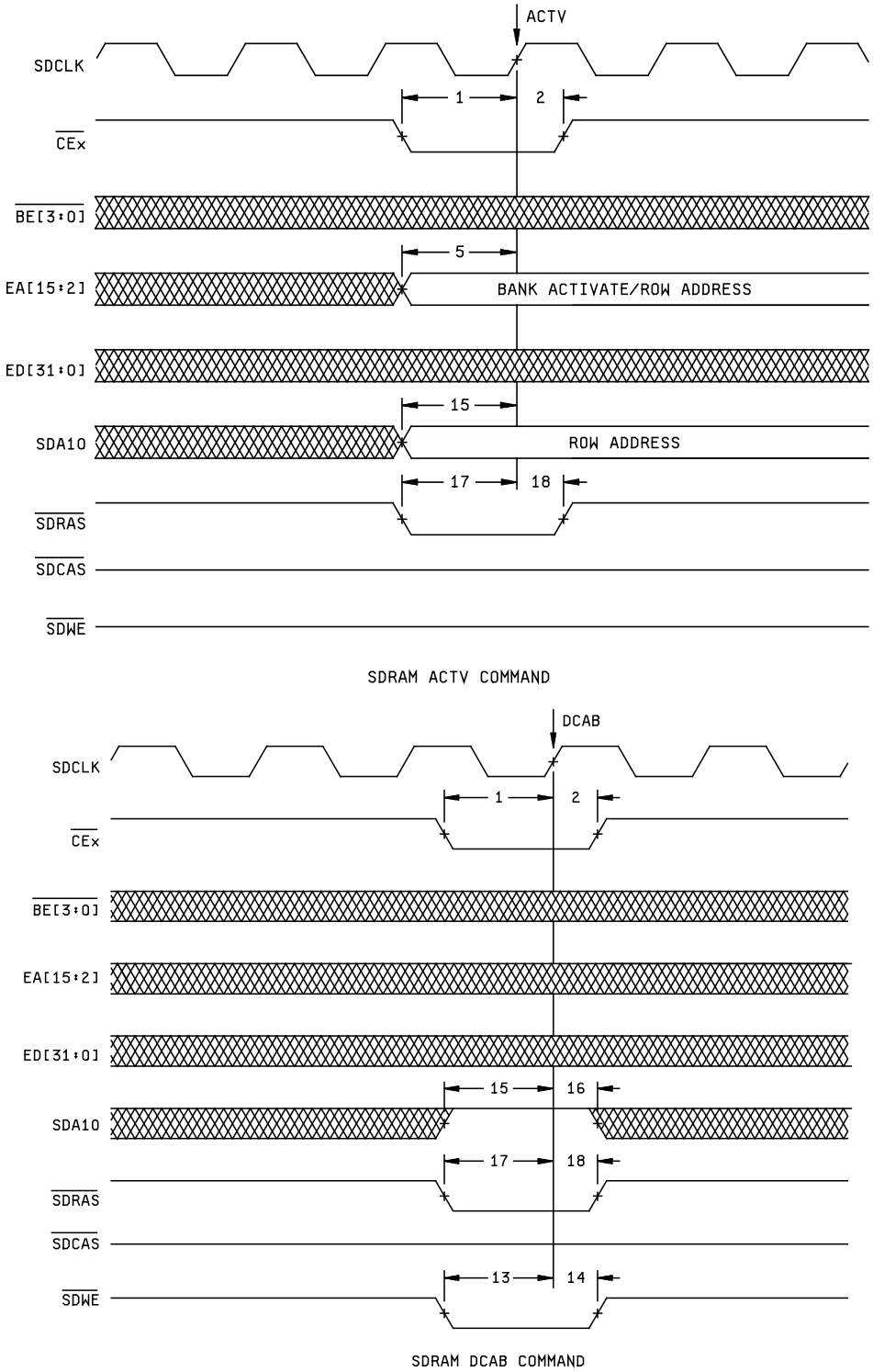


FIGURE 6. Timing waveforms - Continued.

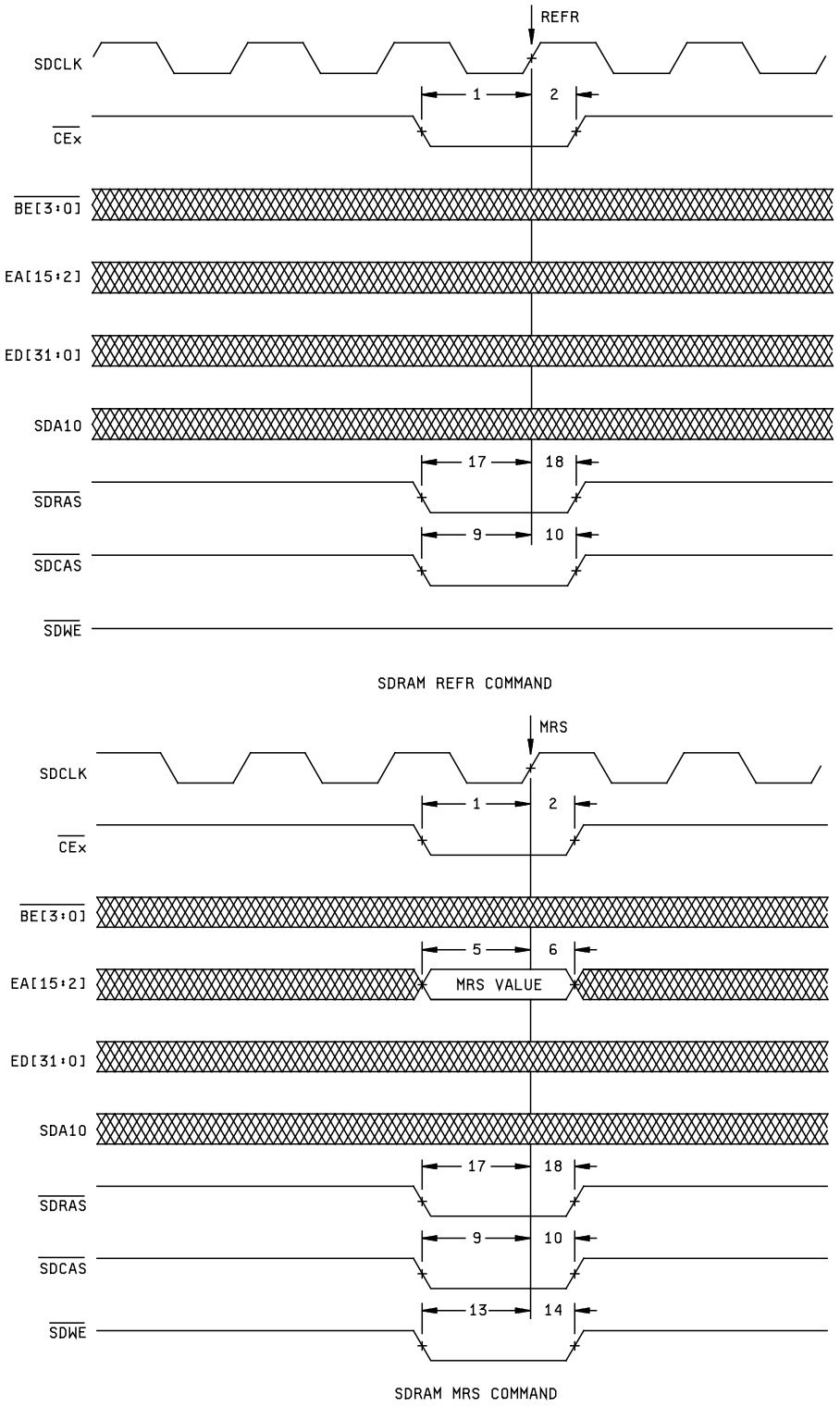
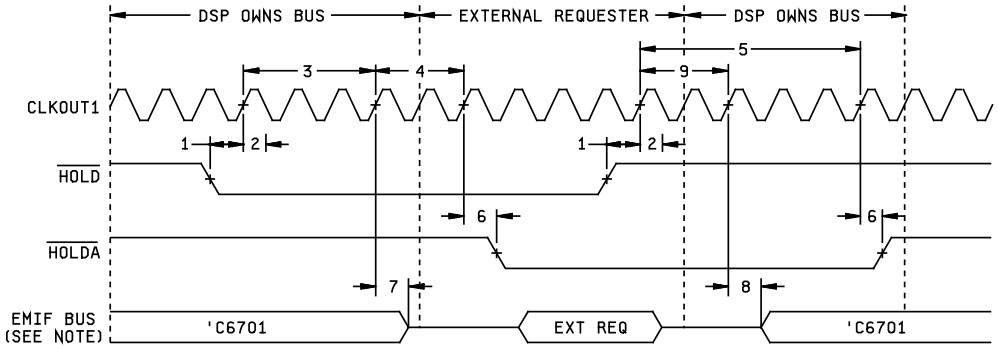
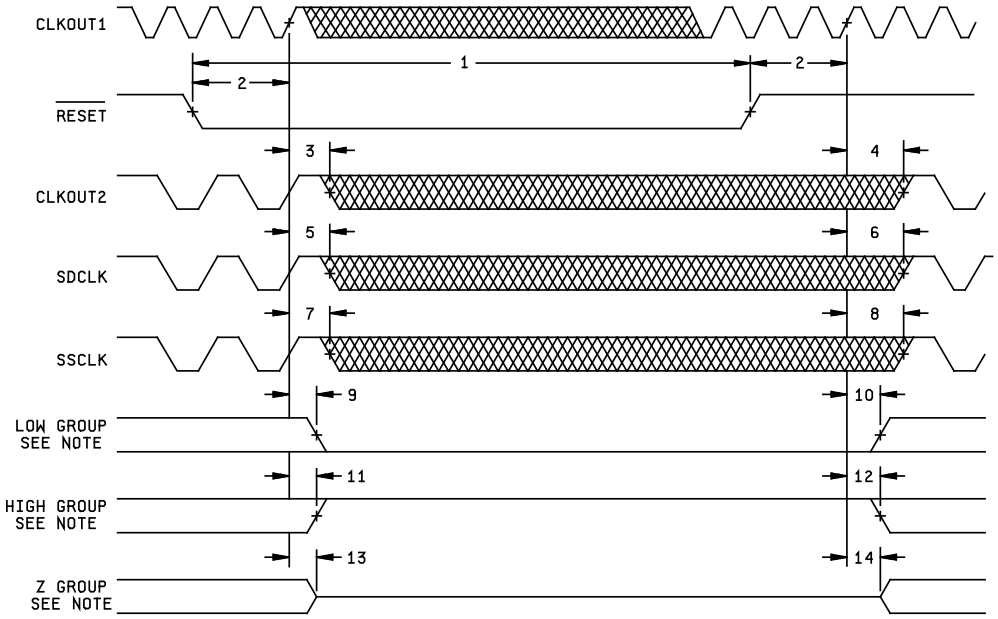


FIGURE 6. Timing waveforms - Continued.



HOLD/HOLDA TIMING

NOTE:
EMIF Bus consists of CE[3:0], BE[3:0], ED[31:0], EA[21:2], ARE, AOE, AWE, SSADS, SSOE, SSWE, SDA10, SDRAS, SDCAS, and SDWE.

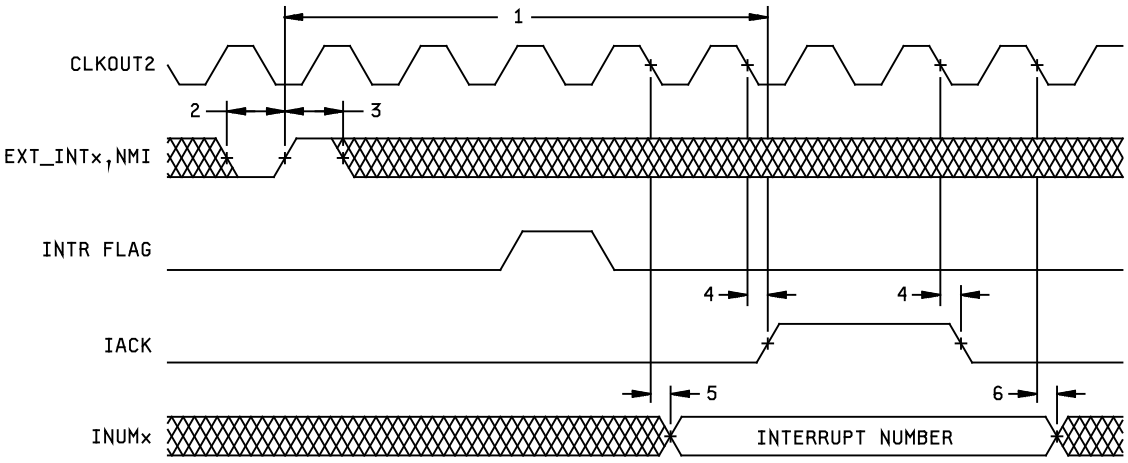


RESET TIMING

NOTES:

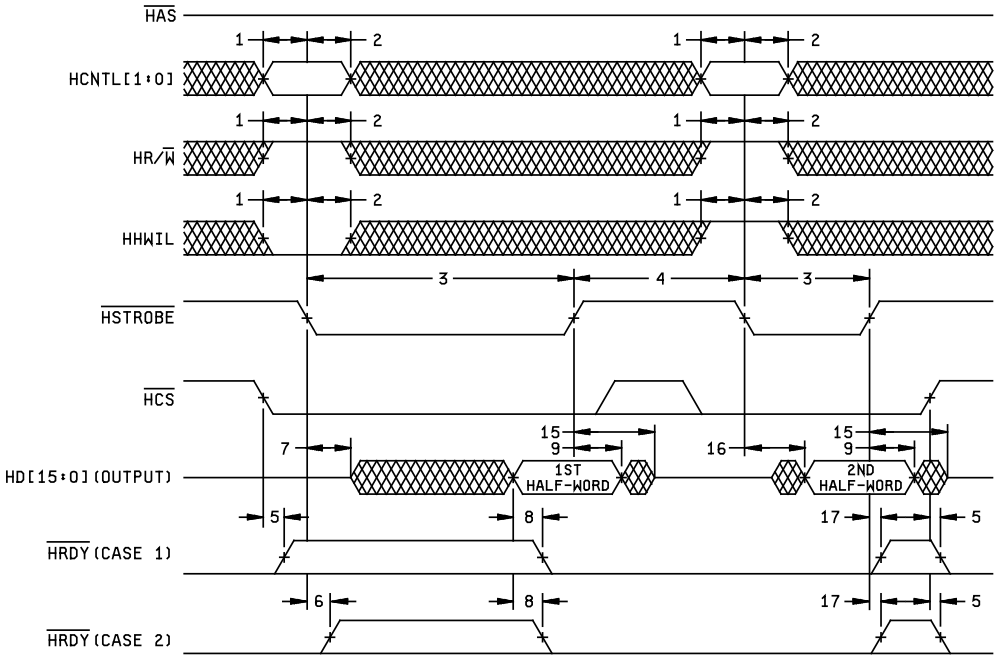
Low group consists of: IACK, INUM[3:0], DMAC[3:0], PD, TOUT0, and TOUT1.
High group consists of: HINT.
Z group consists of: EA[21:2], ED[31:0], CE[3:0], BE[3:0], ARE, AWE, AOE, SSADS, SSOE, SSWE, SDA10, SDRAS, SDCAS, SDWE, HD[15:0], CLKX0, CLKX1, FSX0, FSX1, DX0,DX1, CLKR0, CLKR1, FSR0, and FSR1.

FIGURE 6. Timing waveforms - Continued.

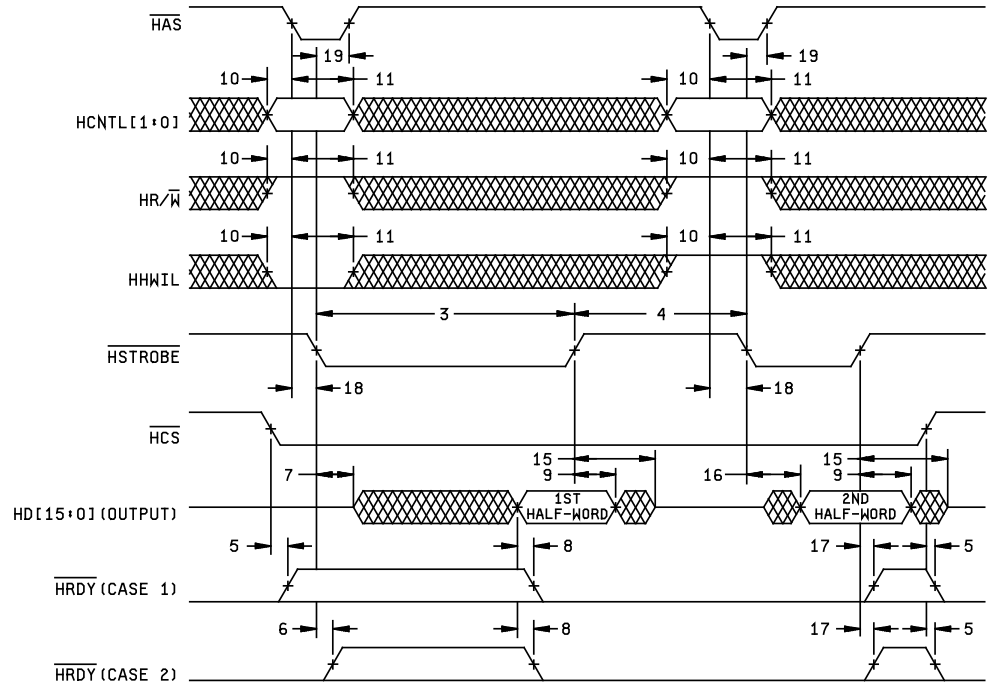


INTERRUPT TIMING

FIGURE 6. Timing waveforms - Continued.

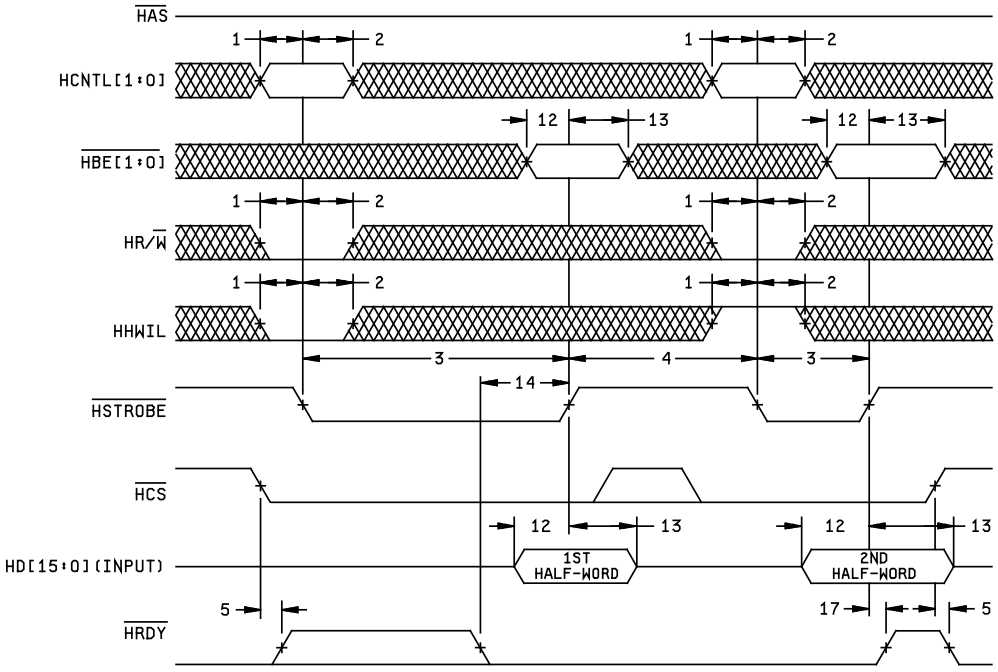


HPI READ TIMING ($\overline{HAS}$ NOT USED,TIED HIGH)

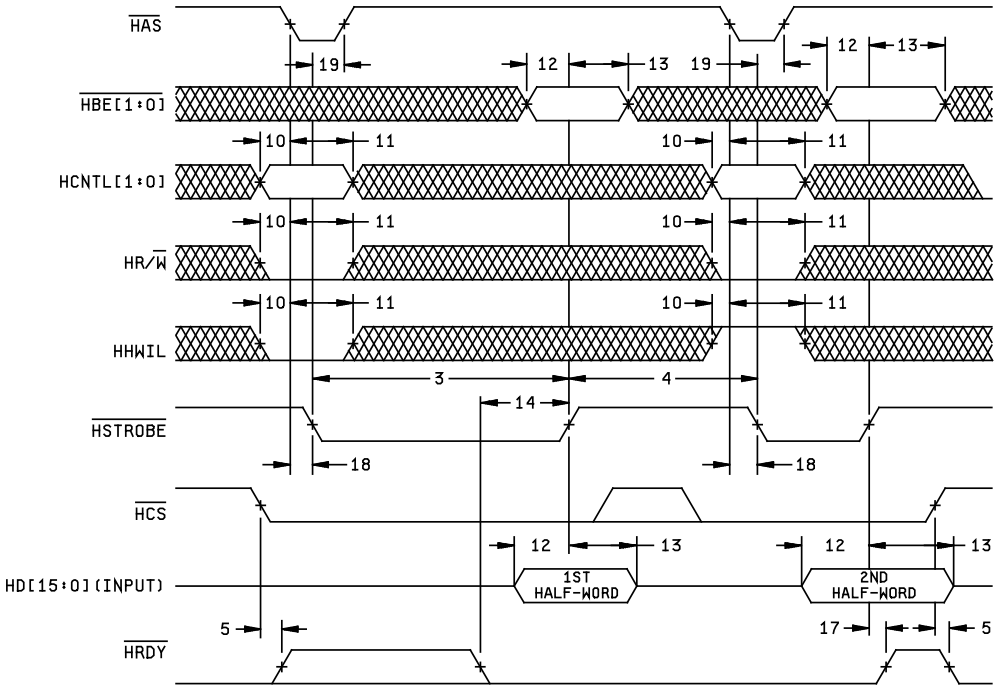


HPI READ TIMING ($\overline{HAS}$ USED)

FIGURE 6. Timing waveforms - Continued.

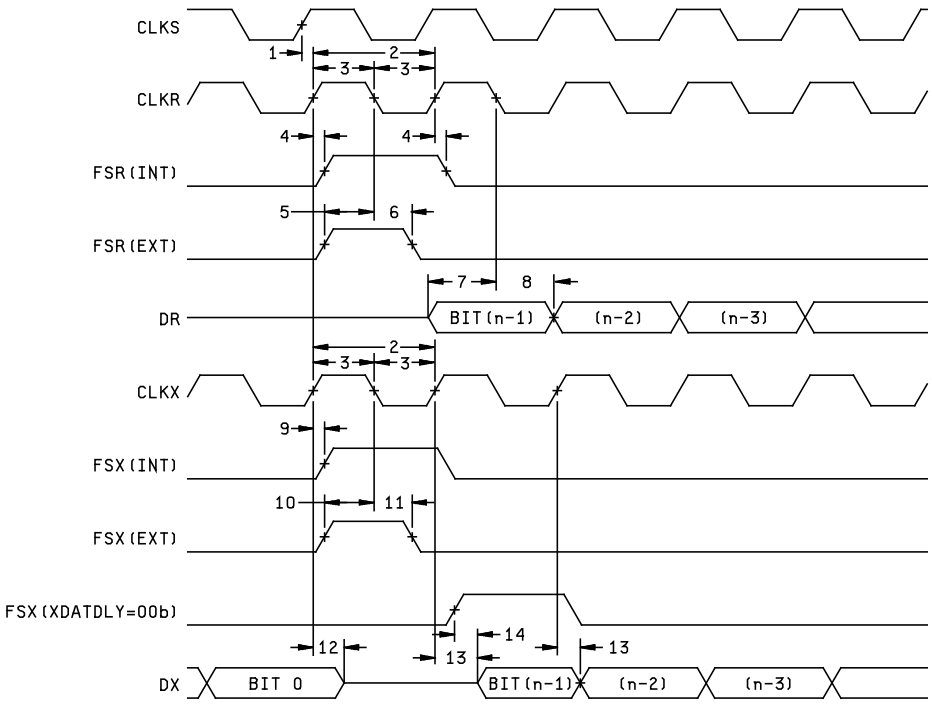


HPI WRITE TIMING (HAS NOT USED, TIED HIGH)

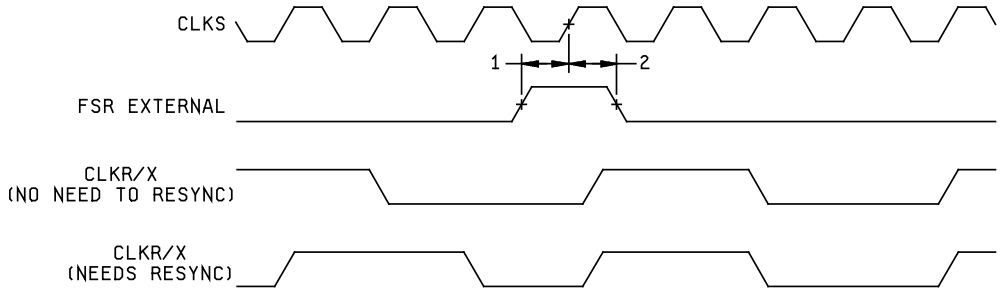


HPI WRITE TIMING (HAS USED)

FIGURE 6. Timing waveforms - Continued.

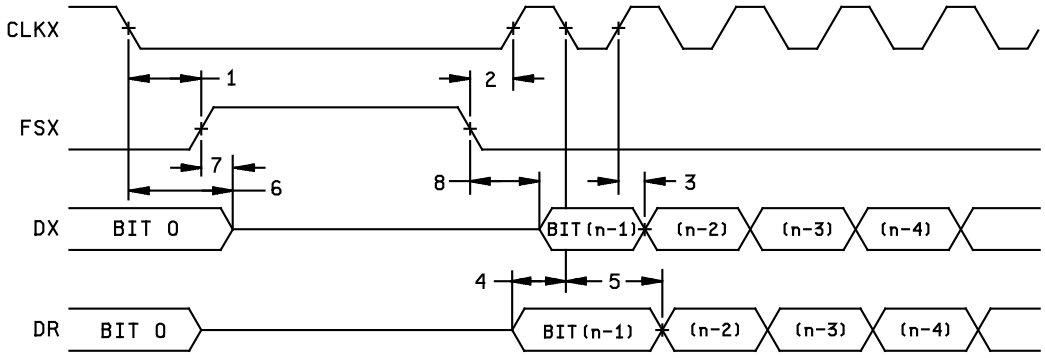


McBSP TIMINGS

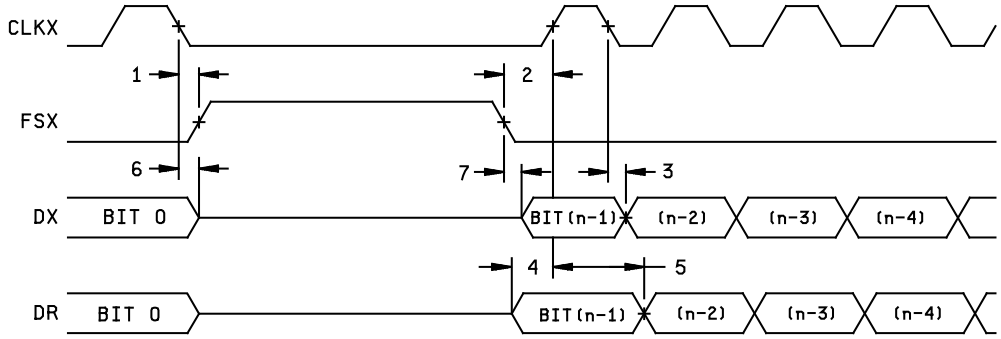


FSR TIMING WHEN GSYNC=1

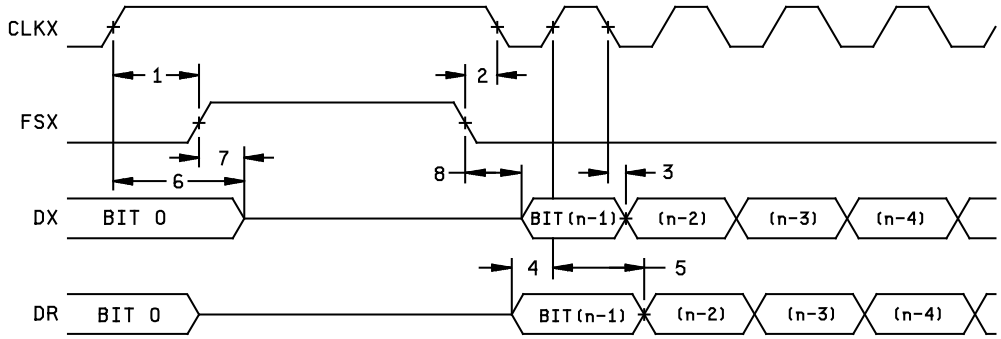
FIGURE 6. Timing waveforms - continued.



McBSP TIMING AS SPI MASTER OR SLAVE:CLKSTP=10b,CLKXP=0

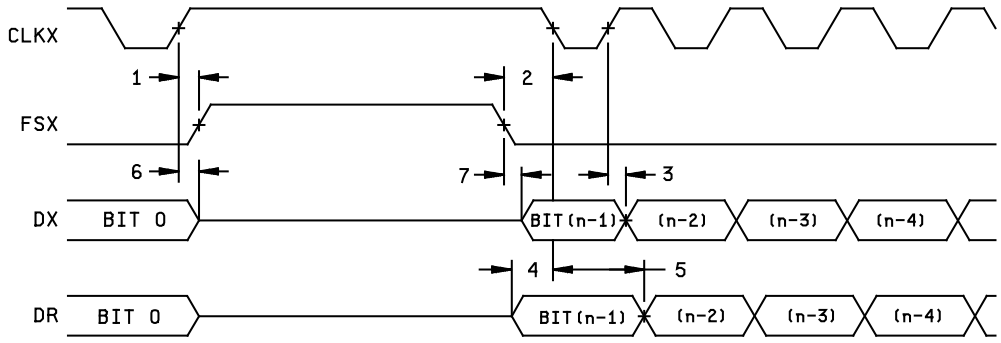


McBSP TIMING AS SPI MASTER OR SLAVE:CLKSTP=11b,CLKXP=0

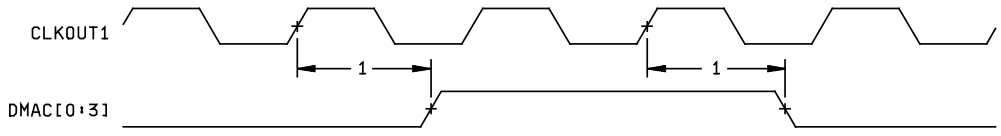


McBSP TIMING AS SPI MASTER OR SLAVE:CLKSTP=10b,CLKXP=1

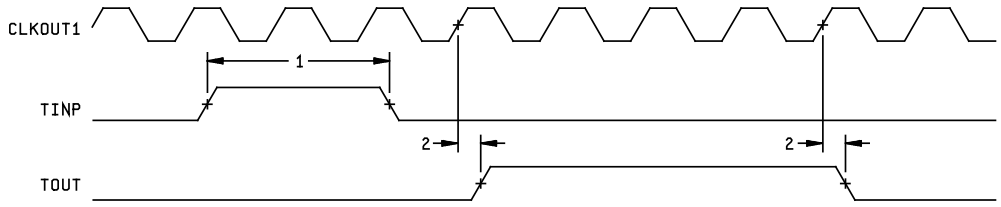
FIGURE 6. Timing waveforms - Continued.



McBSP TIMING AS SPI MASTER OR SLAVE:CLKSTP=11b,CLKXP=1

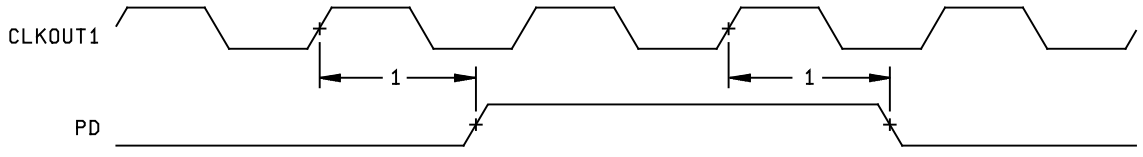


DMAC TIMING

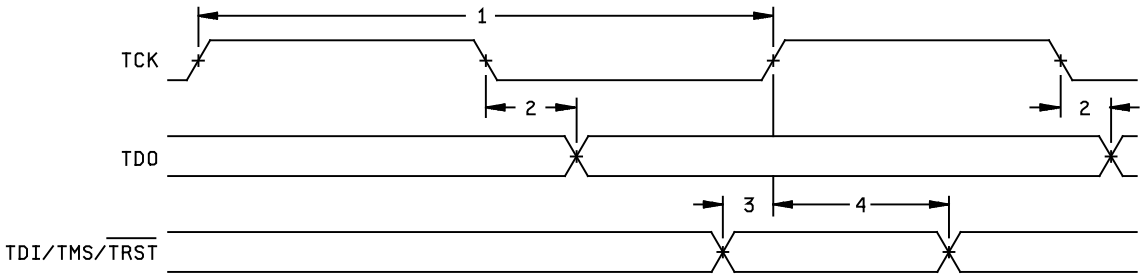


TIMER TIMING

FIGURE 6. Timing waveforms - Continued.



POWER-DOWN TIMING



JTAG TEST-PORT TIMING

FIGURE 6. Timing waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 4 (C_{IN}, C_{OUT}) shall be measured only for the initial test and after process or design changes which may affect input capacitance. One pin of each input/output driver (buffer) type shall be tested on each sample device. A minimum sample size of 5 devices with zero rejects shall be required.

c. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7	1, 7
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	---	---

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-11-21

Approved sources of supply for SMD 5962-98661 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9866101QXA	01295	SMJ320C6701GLPW14
5962-9866101VXA	01295	SMV320C6701GLPW14
5962-9866102QXA	3/	SMJ320C6701
5962-9866102VXA	01295	SMV320C6701GLPM14
5962-9866102VYC	01295	SMV320C6701ZMBM14

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243