Integrated Circuits and Systems

Series Editor
Anantha Chandrakasan
Massachusetts Institute of Technology
Cambridge, Massachusetts

For further volumes, go to
http://www.springer.com/series/7236

Masashi Horiguchi • Kiyoo Itoh

Nanoscale Memory Repair

Springer

Dr. Masashi Horiguchi
Renesas Electronics Corporation
5-20-1, Josuihon-cho
Kodaira-shi, Tokyo, 187-8588
Japan
masashi.horiguchi.kc@renesas.com

Dr. Kiyoo Itoh
Hitachi Ltd.
Central Research Laboratory
1-280, Higashi-Koigakubo
Kokubunji-shi, Tokyo, 185-8601
Japan
kiyoo.itoh.pt@hitachi.com

ISSN 1558-9412
ISBN 978-1-4419-7957-5 e-ISBN 978-1-4419-7958-2
DOI 10.1007/978-1-4419-7958-2
Springer New York Dordrecht Heidelberg London

Preface

Repair techniques for nanoscale memories are becoming more important to cope with ever-increasing "errors" causing degraded yield and reliability. In fact, without repair techniques, even modern CMOS LSIs, such as MPUs/SoCs, in which memories have dominated the area and performances, could not have been successfully designed. Indeed, various kinds of errors have been prominent with larger capacity, smaller feature size, and lower voltage operations of such LSIs. The errors are categorized as hard/soft errors, timing/voltage margin errors, and speed-relevant errors. Hard/soft errors and timing/voltage margin errors, which occur in a chip, are prominent in a memory array because the array comprises memory cells having the smallest size and largest circuit count in the chip. In particular, coping with the margin errors is vital for low-voltage nanoscale LSIs, since the errors rapidly increase with device and voltage scaling. Increase in operating voltage is one of the best ways to tackle the issue. However, this approach is unacceptable due to intolerably increased power dissipation, calling for other solutions by means of devices and circuits. Speed-relevant errors, which are prominent at a lower voltage operation, comprise speed-degradation errors of the chip itself and intolerably wide chip-to-chip speed-variation errors caused by the ever-larger interdie design-parameter variation. They must also be solved with innovative devices and circuits. For the LSI industry, in order to flourish and proliferate, the problems must be solved based on in-depth investigation of the errors.

Despite the importance, there are few authoritative books on repair techniques because the solutions to the problems lie across different fields, e.g., mathematics and engineering, logic and memories, and circuits and devices. This book systematically describes the issues, based on the authors' long careers in developing memories and low-voltage CMOS circuits. This book is intended for both students and engineers who are interested in the yield, reliability, and low-voltage operation of nanoscale memories. Moreover, it is instructive not only to memory designers, but also to all digital and mixed-signal LSI designers who are at the leading edge of such LSI developments.

Chapter 1 describes the basics of repair techniques. First, after categorizing sources of hard/soft errors, the reductions by means of redundancy, error checking

and correction (ECC), and their combination are comprehensively described. Second, after defining the minimum operating voltage V_{min}, reductions of timing/voltage margin errors are described in terms of V_{min}. Finally, reduction techniques for speed-relevant errors are briefly discussed.

Chapter 2 deals with a detailed explanation of the redundancy techniques for repairing hard errors (faults), where faulty memory cells are replaced by spare memory cells provided on the chip in advance. Various yield models and calculations are introduced and various practical circuits and architectures that the authors regard as important for higher yield and reliability are discussed. The chapter also describes the devices for memorizing the addresses of faults and testing techniques for redundancy.

Chapter 3 describes the details of the ECC techniques to cope with both hard and soft errors, where extra bits (check bits) are added to original data bits, thereby enabling error detection and/or correction. After mathematical preparations, various error-correcting codes used for the techniques and their practical implementations in various memory LSIs are discussed. This is followed by the estimation of the reduction in hard-error and soft-error rates using ECC. Testing techniques for ECC are also described.

Chapter 4 deals with the combination of the redundancy and ECC. Combining both the techniques generates a synergistic effect and dramatically enhances the repair capability. It is especially effective for random-bit errors. After quantitative estimation of the synergistic effect, the application to the repair of faults due to device mismatch is discussed as a promising application of the effect.

Chapter 5 systematically describes challenges to ultra-low-voltage nanoscale memories and the repair techniques to accomplish the issues. After clarifying that reduction in the minimum operating voltage V_{DD} (i.e., V_{min}) is the key to reducing the voltage and timing margin error, adaptive circuits and relevant technologies to reduce V_{min} are proposed, and the general features are described. Then, the V_{min}s of logic gates, SRAMs, and DRAMs are compared. After that, devices (e.g., fully depleted planar SOI and FinFET structures), circuits (e.g., gate-source reverse biasing schemes accepting low threshold voltage (V_t) MOSFETs), and subsystems to widen the margins through reducing V_{min} are described.

Chapter 6 briefly describes device/circuit techniques to cope with two kinds of speed-relevant errors, namely, the speed degradation error and the interdie speed variation error. After specifying reduced gate-over-drive voltage of MOSFETs as the source of the speed degradation error, some solutions (e.g., using low-V_{t0} circuits and dynamic V_t circuits utilizing double-gate FD-SOI structures) are exemplified. Moreover, after specifying the so-called global variation of design parameters in the wafer as the source of the interdie speed variation error, some solutions such as power management for compensating for the variation with static or quasi-static controls of internal supply voltages are presented.

Tokyo, Japan

Masashi Horiguchi
Kiyoo Itoh

Contents

1 An Introduction to Repair Techniques 1
1.1 Introduction 1
1.2 Hard and Soft Errors and Repair Techniques 1
1.2.1 Hard and Soft Errors 2
1.2.2 Redundancy 3
1.2.3 ECC 5
1.2.4 Combination of Redundancy and ECC 8
1.2.5 Others 8
1.3 Margin Errors and Repair Techniques 9
1.3.1 Device and Process Variations 11
1.3.2 Timing and Voltage Margin Errors 11
1.3.3 Reductions of Margin Errors 14
1.4 Speed-Relevant Errors and Repair Techniques 15
References 16

2 Redundancy 19
2.1 Introduction 19
2.2 Models of Fault Distribution 20
2.2.1 Poisson Distribution Model 20
2.2.2 Negative-Binomial Distribution Model 22
2.3 Yield Improvement Through Redundancy 25
2.4 Replacement Schemes 29
2.4.1 Principle of Replacement 29
2.4.2 Circuit Implementations 30
2.5 Intrasubarray Replacement 36
2.5.1 Simultaneous and Individual Replacement 39
2.5.2 Flexible Replacement 42
2.5.3 Variations of Intrasubarray Replacement 49
2.6 Intersubarray Replacement 52
2.7 Subarray Replacement 54

2.8 Devices for Storing Addresses 56
2.8.1 Fuses 56
2.8.2 Antifuses 58
2.8.3 Nonvolatile Memory Cells 60
2.9 Testing for Redundancy 61
References 64

3 Error Checking and Correction (ECC) 69
3.1 Introduction 69
3.2 Linear Algebra and Linear Codes 70
3.2.1 Coding Procedure 70
3.2.2 Decoding Procedure 72
3.3 Galois Field 75
3.4 Error-Correcting Codes 77
3.4.1 Minimum Distance 78
3.4.2 Number of Check Bits 79
3.4.3 Single Parity Check Code 82
3.4.4 Hamming Code 82
3.4.5 Extended Hamming Code and Hsiao Code 84
3.4.6 Bidirectional Parity Code 85
3.4.7 Cyclic Code 86
3.4.8 Nonbinary Code 89
3.5 Coding and Decoding Circuits 92
3.5.1 Coding and Decoding Circuits for Hamming Code 92
3.5.2 Coding and Decoding Circuits for Cyclic Hamming Code 97
3.5.3 Coding and Decoding Circuits for Nonbinary Code 102
3.6 Theoretical Reduction in Soft-Error and Hard-Error Rates 105
3.6.1 Reduction in Soft-Error Rate 105
3.6.2 Reduction in Hard-Error Rate 108
3.7 Application of ECC 111
3.7.1 Application to Random-Access Memories 112
3.7.2 Application to Serial-Access Memories 126
3.7.3 Application to Multilevel-Storage Memories 130
3.7.4 Application to Other Memories 133
3.8 Testing for ECC 135
References 136

4 Combination of Redundancy and Error Correction 139
4.1 Introduction 139
4.2 Repair of Bit Faults Using Synergistic Effect 139
4.2.1 Principle of Synergistic Effect 139
4.2.2 Yield Estimation 144
4.3 Application of Synergistic Effect 149
4.3.1 Threshold-Voltage Variations 149
4.3.2 Estimated Effect 151
References 155

5 Reduction Techniques for Margin Errors of Nanoscale Memories .. 157
5.1 Introduction . . . 157
5.2 Definition of V_{min} . . . 159
5.3 Reduction of V_{min} for Wider Margins . . . 160
5.3.1 General Features of V_{min} . . . 160
5.3.2 Comparison of V_{min} for Logic Block, SRAMs, and DRAMs . . . 165
5.4 Advanced MOSFETs for Wider Margins . . . 165
5.4.1 Planar FD-SOI MOSFETs . . . 167
5.4.2 FinFETs . . . 169
5.5 Logic Circuits for Wider Margins . . . 173
5.5.1 Gate-Source Offset Driving . . . 174
5.5.2 Gate-Source Differential Driving . . . 178
5.5.3 Combined Driving . . . 180
5.5.4 Instantaneous Activation of Low-V_{t0} MOSFETs . . . 181
5.5.5 Gate Boosting of High-V_{t0} MOSFETs . . . 181
5.6 SRAMs for Wider Margins . . . 182
5.6.1 Ratio Operations of the 6-T Cell . . . 182
5.6.2 Shortening of Datalines and Up-Sizing of the 6-T Cell . . . 183
5.6.3 Power Managements of the 6-T Cell . . . 185
5.6.4 The 8-T Cell . . . 187
5.7 DRAMs for Wider Margins . . . 188
5.7.1 Sensing Schemes . . . 188
5.7.2 V_{min}(SA) of Sense Amplifier . . . 189
5.7.3 V_{min}(Cell) of Cell . . . 190
5.7.4 Comparison Between V_{min}(SA) and V_{min}(Cell) . . . 190
5.7.5 Low-V_{t0} Sense Amplifier . . . 191
5.7.6 FD-SOI Cells . . . 192
5.8 Subsystems for Wider Margins . . . 194
5.8.1 Improvement of Power Supply Integrity . . . 194
5.8.2 Reduction in V_{t0} at Subsystem Level . . . 195
5.8.3 Low-V_{t0} Power Switches . . . 196
References . . . 198

6 Reduction Techniques for Speed-Relevant Errors of Nanoscale Memories . . . 203
6.1 Introduction . . . 203
6.2 Reduction Techniques for Speed-Degradation Errors . . . 204
6.3 Reduction Techniques for Interdie Speed-Variation Errors . . . 205
6.3.1 On-Chip V_{BB} Compensation . . . 207
6.3.2 On-Chip V_{DD} Compensation and Others . . . 211
References . . . 212

Index . . . 213