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Dynamic Analysis of Extendable Hybrid Voltage Lift DC–DC Converter for DC Microgrid

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Abstract: This paper proposes a novel non-isolated high voltage gain dc–dc converter with a boost^2 (B^2) technique. The derived single-switch hybrid voltage-lift topology generates a higher voltage conversion ratio with less component counts than traditional voltage-lift converters. Furthermore, to show its superiority, the proposed topology is compared with other recent non-isolated dc–dc converters in terms of the number of power components such as inductors, capacitors, diodes, and switches. Moreover, the voltage stress across the power switch is less than the output voltage, which results in using low-rated components and reducing the converter cost. The steady-state analysis of the proposed topology is carried out with the operating modes in continuous and discontinuous conduction modes. The critical inductance for the proposed converter is derived for design considerations. Compared to the other traditional step-up converters, the stresses across the power diodes are highly reduced. The analysis related to the addition of an expander cell with the topology is performed concerning boundary conditions. An efficiency model with loss calculation is presented. Furthermore, the reliability analysis is performed with the military handbook to determine the failure rate of the converter's components. Finally, the simulation and 50 W prototype model for experimental validation prove the strength of the proposed topology.

Keywords: dc–dc converter; high gain; hybrid; switched inductor; voltage-lift; voltage stress

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1. Introduction

Nowadays, energy sources such as Photovoltaic (PV) and fuel cells have attracted research attention due to the depletion of fossil fuels. The usage of a grid-connected PV system, standalone residential PV system, electric vehicle, LED lighting systems, etc., are increasing. The main limitation in many renewable energy sources is the low output voltage and, therefore, there is a need for the power converter to increase the gain [1,2]. Due to this low voltage, the high gain dc–dc converter is a primary component in the Microgrid system, depicted in Figure 1. It is mainly required to boost the low PV source and battery voltage (12–48 V) to the required voltage level to invert it into AC and feed it into the grid system [3,4]. In this regard, a highly efficient and reliable power converter is essential to integrate a sustainable source into the electric grid [5]. The several different types of PV panels in series or parallel are not the innovative solution to boost the voltage to the required load level. Hence, a front-end high gain dc–dc converter plays a vital role in reducing the cost incurred in adding more PV panels [6]. The DC microgrid has more advantages, such as enhanced power quality and supply security [7,8]. Additionally, the energy storage system is gaining popularity in DC microgrid systems due to the intermittent nature of sustainable energy sources [9].

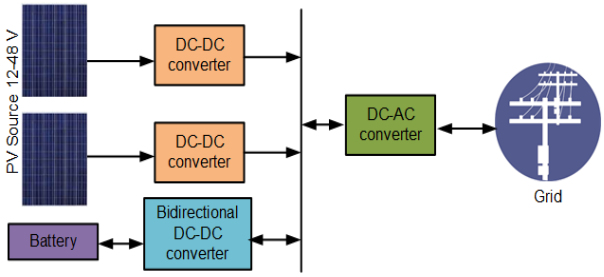


Figure 1. High gain DC–DC converter in Microgrid system.

For a standalone application, the battery is needed to provide an uninterruptable power supply to the loads in this mode. Due to the variation of the PV source, maximum power point tracking (MPPT) is essential for PV powered applications. For MPPT tracking, a battery backup is needed. From Figure 1, high step-up dc–dc converters are required with a high voltage gain, efficiency, and power density for the distributed power generation system [10]. DC–DC converters are categorized into the transformer and transformer less converters [11]. DC–DC converters with transformers are primarily employed for interfacing the renewable energy sources. By increasing the turns ratio of the transformer, the voltage gain of the converters increases. However, unfortunately, the weight of the converter increases with a decrease in efficiency and the pulsed current produced in the converters with the transformer reduces the lifetime of the PV and occupies more space. The non-isolated converters such as conventional boost dc–dc converters have high current ripples and conduction losses with high conversion ratios [12]. An interleaved structure can reduce the input current ripple and can be employed to increase the power level. The voltage multiplier cells coupled inductor and switched passive components are added to boost the gain in dc–dc converters [13]. However, these methods increase the number of passive components and switches. The most commonly used method in non-isolated converters to boost the gain is the voltage-lift method [14]. In 2018, a non-isolated dc converter was proposed with a voltage-lift technique with a component count of nine [15]. However, the voltage gain is boosted only three for D = 0.5. In [16–20], a high gain topology is derived with very high component counts such as 14 and 18. Various high gain concepts are proposed in the literature [20–31]. In these topologies, the voltage gain is expandable by adding more inductors, increasing the converter's size and complexity. Based on the literature, the main limitations in the existing topologies are pulsed input current, more component count, leakage inductance, more voltage, and current stresses across switches and diodes, voltage spikes, etc. [32–34]. More switches and passive components increase the bulkiness of the converter and the complexity [35–48]. All these issues are considered for which a new dc–dc converter without a transformer is proposed by integrating the switched inductor and voltage-lift cell into a common branch to obtain a Hybrid Switched Inductor based Voltage-Lift (HSIVL) converter. The proposed converter has the following advantages and is also listed as shown in Table 1:

i. Single switch converter with reduced complexity for controller design.
ii. Less number of passive components, which reduces the volume of the converter.
iii. Low voltage stress, which reduces the conduction loss and cost of the converter.
iv. Output diode voltage stress is less than the output voltage, which minimizes the cost.
v. Efficiency is higher due to fewer component counts.

The derivation of the proposed topology is discussed in Section 2.1. Section 2.2 presents the operating principle of the derived topology. The steady-state analysis of the proposed converter in both continuous and discontinuous conduction modes are dealt with in Sections 3.1 and 3.2, respectively. The detailed analysis of the converter with a critical inductance analysis is depicted in Section 4. The power loss analysis of the converter is elaborated in Section 5. The dynamic behavior of the derived topology is analyzed by obtaining a frequency response plot and the inference from the study is presented

in Section 6. The reliability study is performed and the failure rate of the component is analyzed in Section 7. Section 8 presents the comparative study of the suggested topology with the similar topology reported in the literature. The simulation and experimental study are performed and the results are discussed in Section 9. Section 10 summarizes the inferences and discusses the future scope. Finally, the paper is concluded with the research findings.

Table 1. Comparison of proposed converter with the literature.

Ref	Number of Components Remarks
Proposed topology	• One switch is required with two capacitors • Total component is less • Higher voltage gain • Switch voltage stress reduced
Super-lift [18]	• One switch is required with one capacitor • Total component is less • Higher voltage gain is less than the proposed topology • Switch voltage stress is higher than the proposed topology
Active–passive SL [19]	• Switch count is high • Total component is high • Higher voltage gain is less than the proposed topology • Switch voltage stress is higher than the proposed topology
AH-SLC [20]	• It uses two switches and four diodes. Further the capacitor count is high for lower voltage gain • High voltage stress and no possible to expand the structure

2. Proposed High Voltage DC–DC Converter

2.1. Description of Proposed HSIVL Topology

Figure 1 presents three dc–dc converter topologies. The Switched Inductor (SI) cell in Figure 2a is combined with the Voltage-Lift (VL) cell in Figure 2b to derive a Hybrid Switched Inductor-based Voltage-Lift (HSIVL) converter, which is illustrated in Figure 2c.

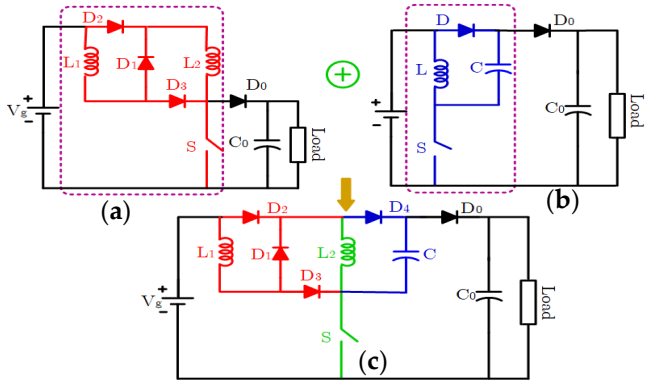


Figure 2. DC–DC converter topologies (**a**) Super-lift boost converter (**b**) Elementary Luo converter (**c**) Hybrid switched inductor-based voltage-lift converter.

The gain of the super-lift boost converter is (1 + D/(1 − D) and the gain of elementary Luo converter is (2 − D/(1 − D). The voltage conversion ratio of both the converters depicted in Figure 2a,b is less than the proposed topology. The switch voltage stress of the super-lift boost converter is equal to the output voltage. The extendable capability is not possible in an elementary Luo converter. The special features of the suggested topology by the integration of the topologies are in Figure 2a,b.

- The voltage gain is high compared to super-lift boost and elementary Luo converter.
- The switch voltage stress is not equal to the output voltage, which reduces the Rds (on) and increases the efficiency of the converter.
- Extension of the voltage gain is feasible without increasing the power switch count.

2.2. Modes and Operating Principle of the HSIVL Topology

2.2.1. Mode I

When the switch is conducting, the diodes D_2, D_3, and D_4 will be forward biased and due to the topology, switched inductors will be connected in parallel. The inductors L_1 and L_2 will be charged simultaneously along with the capacitor to the full supply voltage. At the same time, diodes D_1 and D_0 will be reverse biased and C_0 will be supplying the load Considering Kirchhoff's Voltage Law in Figure 3a, the inductor voltage is obtained as:

$$V_{L1} = V_{L2} = V_C = V_g \tag{1}$$

$$I_C = \frac{I_g}{3} \tag{2}$$

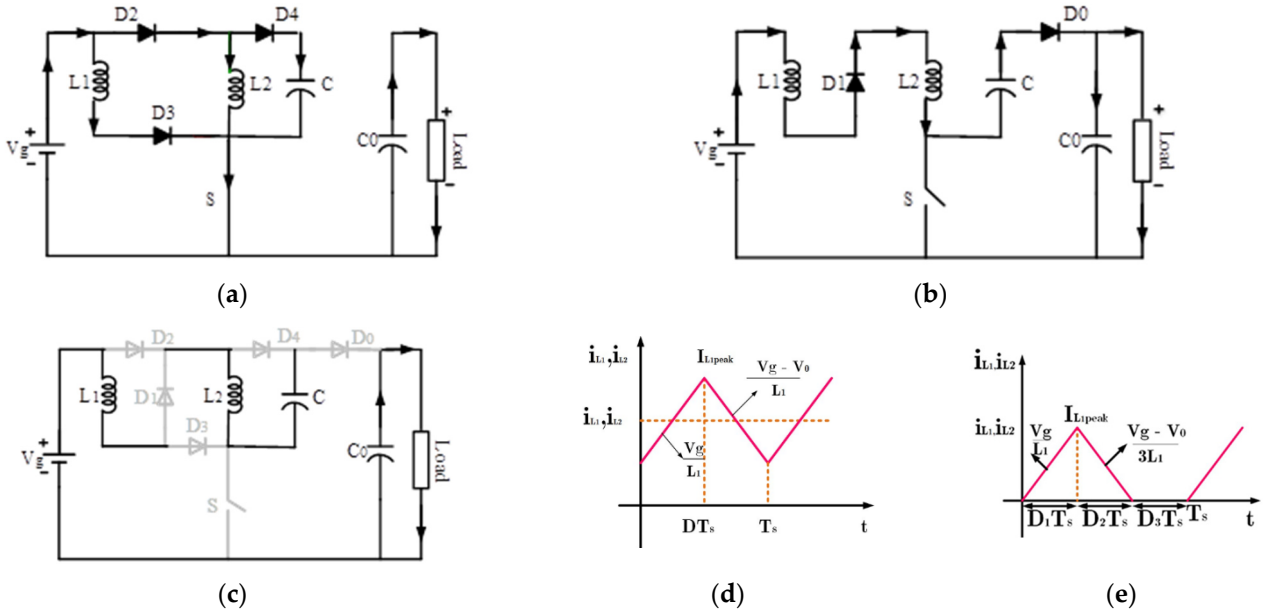


Figure 3. Operating modes (**a**) Mode I, (**b**) Mode II, (**c**) DCM, (**d**,**e**) Inductor waveform at CCM and DCM.

2.2.2. Mode II

When the switch is in the non-conducting state, diodes D_1 and D_0 will be forward biased and, due to this, the switched inductors will be connected in series. The energy stored in inductors L_1 and L_2 will be discharged along with the capacitor C to the load and charge capacitor C_0. At the same time, diodes D_2, D_3, and D_4 will be reverse biased. Figure 4a,b depict the key waveforms of the HSIVL converter. Similar to the ON condition (Mode I), the inductor voltage is acquired from Figure 3b.

$$V_{L1} = V_{L2} = V_C = \frac{V_g - V_o}{3} \tag{3}$$

$$I_C = I_{L1} = I_{L2} = I_g \tag{4}$$

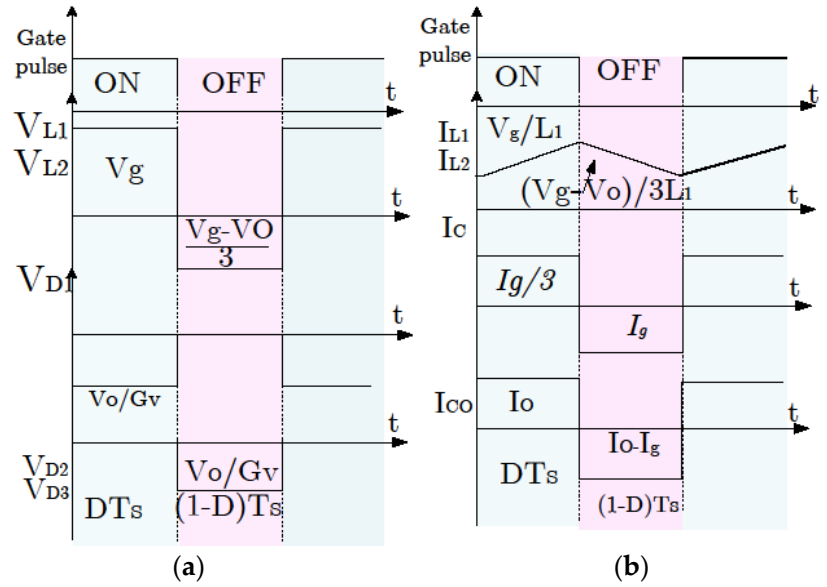


Figure 4. Key waveforms of HSIVL converter: (**a**) Voltage waveforms and (**b**) current waveforms.

2.2.3. Mode III

When the switches and diodes are not conducting, it will lead to a discontinuous mode of operation. This mode might occur due to large current ripple at light load conditions.

The capacitor C_O alone supplies the load and starts discharging. The voltage gain of the converter in this mode not only depends on the duty cycle, but also becomes load dependent.

3. Steady-State Analysis

3.1. Continuous Conduction Mode

The voltage balance law is applied to Equations (1) and (3) and the following relationship is obtained:

$$\int_0^{DT} V_g dt + \int_{DT}^{T} \frac{V_g - V_O}{3} dt \tag{5}$$

By simplifying (5), the voltage conversion ratio is determined as:

$$G_{V-CCM} = \frac{V_O}{V_g} = \frac{1+2D}{1-D} \tag{6}$$

The general voltage gain expression for the derived topology with N, which is the number of expander cells:

$$G_{V-CCM} = \frac{V_O}{V_g} = \frac{1+2ND}{1-D} \tag{7}$$

The ampere second balance law is applied to Equations (2) and (4) and the following relationship is obtained:

$$I_{L1(avg)} = I_{L2(avg)} = \frac{I_O G_{V-CCM}}{1+2D} \tag{8}$$

The sensitivity of the output voltage with respect to duty cycle is:

$$S = \frac{dV_O}{dD} = \frac{V_g}{[1-D]^2} \tag{9}$$

The value of sensitivity is just similar to the conventional boost converter. The sensitivity, S, remains the same for N number of expander cells. The output-power capability of the proposed topology is:

$$C_P = \frac{P_O}{V_{SW} I_{SW}} = \frac{1-D}{3D} \tag{10}$$

If D increases, the output-power capability, C_p starts to decrease.

3.2. Stress across the Semiconductor Devices

From the steady-state analysis, the stresses across all the components of the derived topology with average and Root Mean Square (RMS) currents of the semiconductor devices are obtained and listed below.

The maximum voltage stress across the switch is not equal to the output voltage and it is expressed as:

$$V_{SW(max)} = \frac{V_O(2G_V + 1)}{3G_V} \tag{11}$$

The RMS current through the switch is determined as:

$$I_{SW(RMS)} = I_O G_V \sqrt{D} \tag{12}$$

Similarly, the diodes voltage and currents are determined as:

$$V_{D1(max)} = V_{D2(max)} = V_{D3(max)} = V_{D4(max)} = \frac{V_O}{G_V}; V_{DO(max)} = \frac{3VgD}{1-D} \tag{13}$$

$$I_{D1(RMS)} = I_{DO(RMS)} = \frac{I_O G_V \sqrt{1-D}}{1+2D} \tag{14}$$

$$I_{D2(RMS)} = I_{D3(RMS)} = \frac{I_O G_V \sqrt{D}}{1+2D} \tag{15}$$

3.3. Stress across the Passive Components across the Semiconductor Devices

The voltage across the capacitors (C and Co) and current through the inductors (L_1 and L_2) are acquired and presented for the design of the passive components.

$$V_{C(max)} = \frac{V_O}{G_V} \tag{16}$$

$$I_{L1(RMS)} = I_{L2(RMS)} = \frac{I_O G_V}{1+2D} \tag{17}$$

$$I_{CO(RMS)} = I_O \sqrt{\frac{G_V D}{1+2D}} \tag{18}$$

Switchs (9)–(16) are used to find the ratings of semiconductor devices and passive components.

The design guidelines for the components are presented in the later section.

The switch and output diode voltage stress depend on three parameters: input voltage, duty cycle, and the number of expander cells, N. To find the greater influencing factor on the switch, a graph is plotted in Figure 5. It is observed from the figure that the switch voltage stress is directly proportional to the input voltage and expander cell and both these factors are great at influencing compared to the duty cycle. The output diode, Do, has the similar voltage stress as the switch and it is equal to $V_O - Vg$. Hence, this analysis will help in the selection of the number of expander cells and input voltage. To find the impact of expander cells on the voltage stress on the component, the stress on the switch and diodes are tabulated for various numbers of expander cells (1, 2, . . . , N) and presented in Table 2.

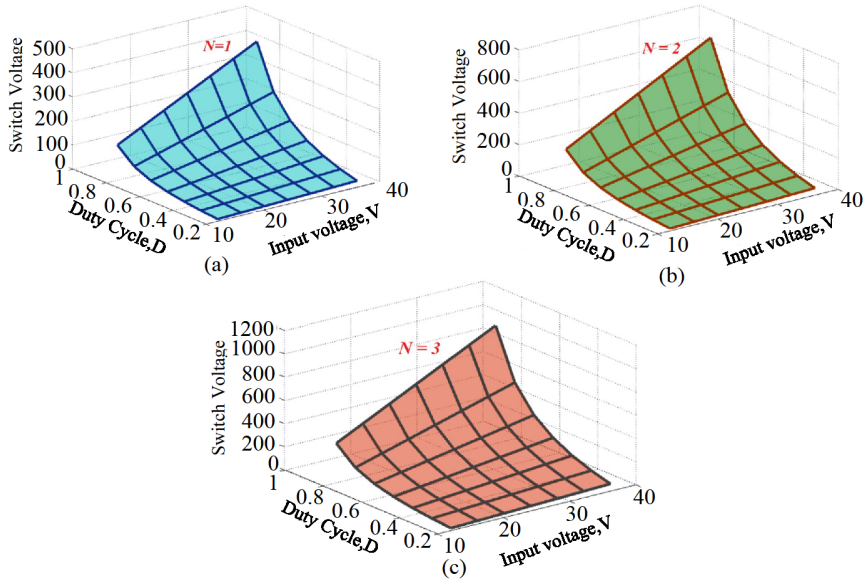


Figure 5. Analysis on switch voltage stress (**a**) N = 1 (**b**) N = 2 (**c**) N = 3.

Table 2. Correlations for 1, 2, . . . , N expander cell configuration.

Number of Expander Cell	Voltage Gain	Voltage Stress on Switch	Voltage Stress on Output Diode	Voltage Stress on Other Diodes (D_1–D_4)
1	$\frac{1+2D}{(1-D)}$	$\frac{3DV_g}{(1-D)}$		
2	$\frac{1+4D}{(1-D)}$	$\frac{5DV_g}{(1-D)}$		Vg
3	$\frac{1+6D}{(1-D)}$	$\frac{7DV_g}{(1-D)}$		
4	$\frac{1+8D}{(1-D)}$	$\frac{9DV_g}{(1-D)}$		
N	$\frac{1+2ND}{(1-D)}$	$\frac{V_gD(1+2N)}{(1-D)}$		N

Figure 2c depicts the operating mode of HSIVL converter in DCM. Using Figure 2d, the average value of inductor (L_1) current in DCM is obtained by the Volt-second balance principle.

$$\langle V_{L1}(t)\rangle = D_1V_g + D_2\left(\frac{V_g - V_O}{3}\right) + D_3(0) = 0 \tag{19}$$

Simplifying (19), the output voltage in DCM condition is determined as:

$$V_O = \left[1 + \frac{3D_1}{D_2}\right]V_g \tag{20}$$

The diode (D_1) current is identical to the inductor (L_1) current during the non-conducting state of switch S. The dc component of diode (D_1) current is:

$$\langle i_{D1}(t)\rangle = \frac{1}{T_S}\int_0^{T_S} i_{L1-Peak}D_2T_Sdt \tag{21}$$

It is observed that in the second interval, the dc component of the inductor (L_1) current is equal to the dc component of the diode (D_1) current. Therefore:

$$\frac{V_O}{R_O(1-D_1)} = \frac{V_gD_1D_2T_S}{2L_1} \tag{22}$$

To eliminate D_2, (22) is simplified to be:

$$D_2 = \frac{3D_1V_g}{V_O - V_g} \tag{23}$$

Using Equation (23) in (20), the following quadratic expression is obtained.

$$V_O{}^2 - V_gV_O - \frac{3V_g{}^2D_1{}^2(1-D_1)}{K_{L1}} = 0 \tag{24}$$

Solving the above equation, the voltage conversion ratio of the HSIVL converter in DCM is acquired as:

$$\frac{V_O}{V_g} = G_{V-DCM}(D_1,\ K_{L1}) = 1 \pm \sqrt{\frac{1+\frac{12D_1{}^2(1-D_1)}{K_{L1}}}{2}} \tag{25}$$

where $K_{L1} = \frac{2L_1}{R_OT_S}$.

Equation (25) presents the voltage conversion ratio of the HSIVL converter in DCM. To analyze the voltage, gain in DCM, a plot is drawn for various values of K_{L1}. It is noted from Figure 6 that the voltage gain decreases with the increase in the value of K_{L1}.

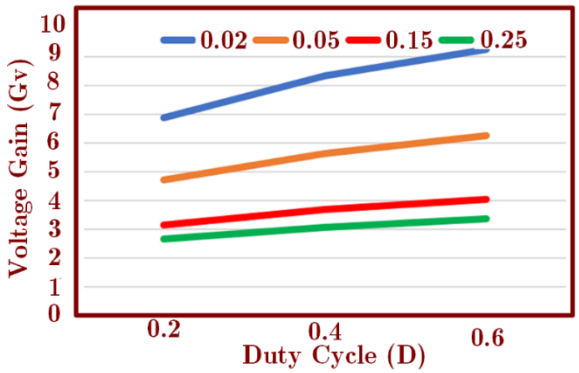


Figure 6. DCM analysis voltage gain vs. duty cycle.

4. Discussion

The design of inductors and capacitors are critical in predicting the performance of the converter, voltage, and current ripples, compactness, losses, filter size, and efficiency. The topology proposed is designed for a normal condition as well as for a worst condition case where the converter can be operated without crossing the limitations. The inductor value is selected based on the desired current ripple and the capacitor values are based on the desired voltage ripple. The average inductor current is larger than the ripples in the inductor (L_1) current and then the converter operates in CCM.

$$I_{L1} > \Delta i_L \tag{26}$$

By substituting the value of the average inductor current and the ripple current in Equation (26), it provides:

$$\frac{V_0}{R_0(1-D)} > \frac{V_O(1-D)D}{2(1+2D)f_sL_1} \tag{27}$$

Solving the above expression to derive the value of inductor will provide:

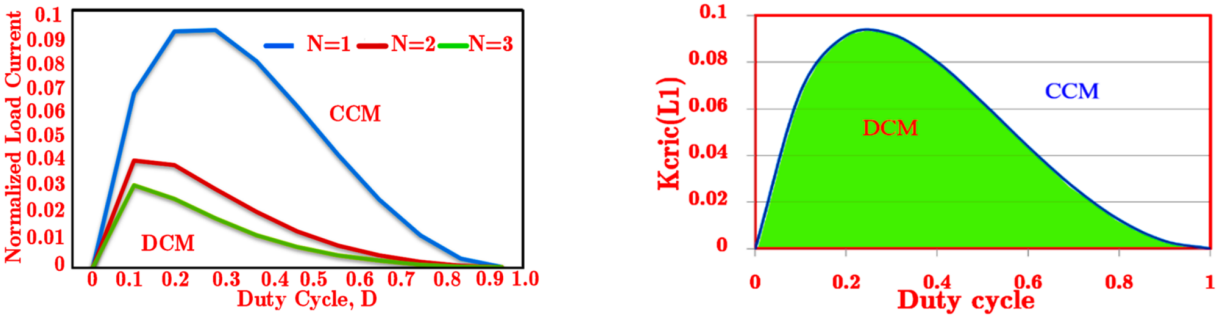
$$\frac{2L_1f_s}{R_o} > \frac{D}{G_V{}^2} \tag{28}$$

$$L_1, L_2 > \frac{R_0(1-D)^2 D}{2(1+2D)f_s} \tag{29}$$

where $K_{cric(L1)}(D) = \frac{D(1-D)}{G_V}$

$$K_{L1} > K_{cric(L1)}(D) \ \ldots\ldots\ldots\ldots \text{CCM} \tag{30}$$

$K_{cric(L1)}$ depends on duty cycle and decides the transition from CCM to DCM mode. Figure 7 illustrates the operation of HSIVL converter concerning critical inductance, which is the boundary between the continuous and discontinuous region. K_{L1} is used to verify the operation of the converter in continuous or discontinuous modes.



(**a**) (**b**)

Figure 7. (**a**) Critical Inductor ($K_{cric(L1)}$) vs. different duty cycle (D) for HSIVL converter. (**b**) Normalized load current at the boundary between CCM and DCM for HSIVL converter.

The output current at the boundary condition of CCM and DCM is provided as:

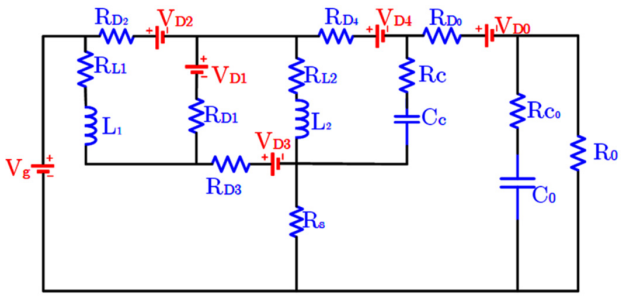
$$I_{OB} = \frac{V_O D(1-D)^2}{2f_s L(1+2D)^2} \tag{31}$$

Figure 7b presents the normalized load current at the boundary between CCM and DCM for N = 1, 2, and 3. From this graph, it is observed that the CCM region can be extended with the increase in the number of expander cell, N.

5. Efficiency Analysis

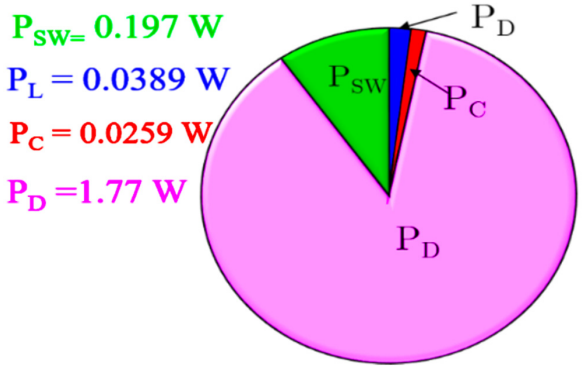
For efficiency analysis, the ripples of inductors and capacitors are neglected for the HSIVL converter. All through this derivation, the MOSFET drain-source resistance is taken as R_S, the forward voltage and forward resistance of the diodes are considered as R_D and V_D, respectively. The DC resistances of the inductors are taken as R_L. Similarly, the Equivalent Series Resistance (ESR) of capacitors C and C_O are assumed to be R_C and R_{CO}, respectively.

The equivalent circuit for the HSIVL converter is presented in Figure 8a to carry out efficiency analysis.



(**a**)

Figure 8. *Cont.*



(**b**)

Figure 8. (**a**) Equivalent circuit for efficiency analysis. (**b**) Loss distribution of HSIVL converter at 50 W.

The parameters chosen to calculate the efficiency of the HSIVL converter are Vg = 12 V, V_O = 48 V, f_S = 10 kHz, D = 0.5, R_O = 50 Ω, R_S = 9 mΩ, V_D = 0.42 V, R_D = 2.1 mΩ, R_L = 4.5 mΩ, and R_C = R_{CO} = 12 mΩ. Table 3 presents the loss equations of all the components in the converter. Figure 8b summarizes the losses distribution in various components of the proposed HSIVL converter. The conversion efficiency is 95.8% at 50 W.

Table 3. Power loss equations of the proposed topology.

Parameters	Power Loss Equations
Inductor loss, P_L	$2\left\{\frac{I_O G_V}{1+2D}\right\}^2 R_L$
Capacitor loss, P_C	$I_O{}^2\left\{\frac{G_V D}{1+2D} R_{CO} + \frac{(4D^2(D-1)+1)^2}{(1-D)^2} R_C\right\}$
Diode Loss, P_D	$I_O V_D\left\{\frac{3G_V D}{1+2D}+1\right\} + I_O{}^2 R_D\left\{\frac{1}{1-D} + \frac{3G_V{}^2}{(1+2D)^2}\right\}$
Switch Loss, P_{SW}	$I_O{}^2 G_V{}^2 D R_S + \frac{f_S I_O}{2}\left(\left(t_r + t_f\right) G_V D\left(V_O - V_g\right)\right)$

6. Dynamic Analysis of the Converter

In this section, the dynamic characteristics of the proposed topology are studied with the derivation of the input to output and control to output transfer function. The converter is modeled with state-space modeling technique and the following transfer functions are obtained.

In this dynamic analysis, the inductor (L_1, L_2, and C) are parallelly charged in ON mode and discharged serially in the subsequent mode. Hence, all these passive components are considered as single component, L. The proposed topology is reduced to a two-order system due to this assumption.

The derived input to output transfer function is expressed as:

$$\frac{\widetilde{V_O(s)}}{\widetilde{V_g(s)}} = \frac{R_O(1+2D)(1-D)}{3LC_O R_O s^2 + 3Ls + (1-D)^2 R_O} \tag{32}$$

The control to output transfer function is obtained as:

$$\frac{\widetilde{V_O(s)}}{\widetilde{d(s)}} = \frac{\left[(1+2D)(1-D)V_g - 3LI_O s\right](R_O/(1-D))}{3LC_O R_O s^2 + 3Ls + (1-D)^2 R_O} \tag{33}$$

From (32) and (33), the frequency response plot is acquired using the same specifications used for simulation and experimental study. After substituting the values of the element, the following expressions are obtained:

$$\frac{\widetilde{V_O(s)}}{\widetilde{V_g(s)}} = \frac{217.5}{2.6e^{-6}s^2 + 3e^{-4}s + 21.75} \tag{34}$$

$$\frac{\widetilde{V_O(s)}}{\widetilde{d(s)}} = \frac{2088 - 0.03966s}{2.6e^{-6}s^2 + 3e^{-4}s + 21.75} \tag{35}$$

The frequency response plots of (29) and (30) are obtained and presented in Figure 9a–d. From these figures, it is noted that the derived topology is a non-minimum phase system because the zero lie in the right half of the s-plane. However, in the case of the control to output transfer function, the poles lie in the jω axis of the s-plane. Hence, the system may fall under marginally stable. These observations recommend designing a controller for the converter to handle the perturbation in input and output voltage condition. The above section explains the dynamic study of the HSIVL converter. The additional feature of the converter with respect to the dynamic analysis is the derivation of the extendable topology's transfer function since the topology is considered with equal inductance and also the voltage across the inductors and capacitors are assumed to be equal for the analysis. In this regard, it will be easier in designing the passive components of the converter and also the controller design.

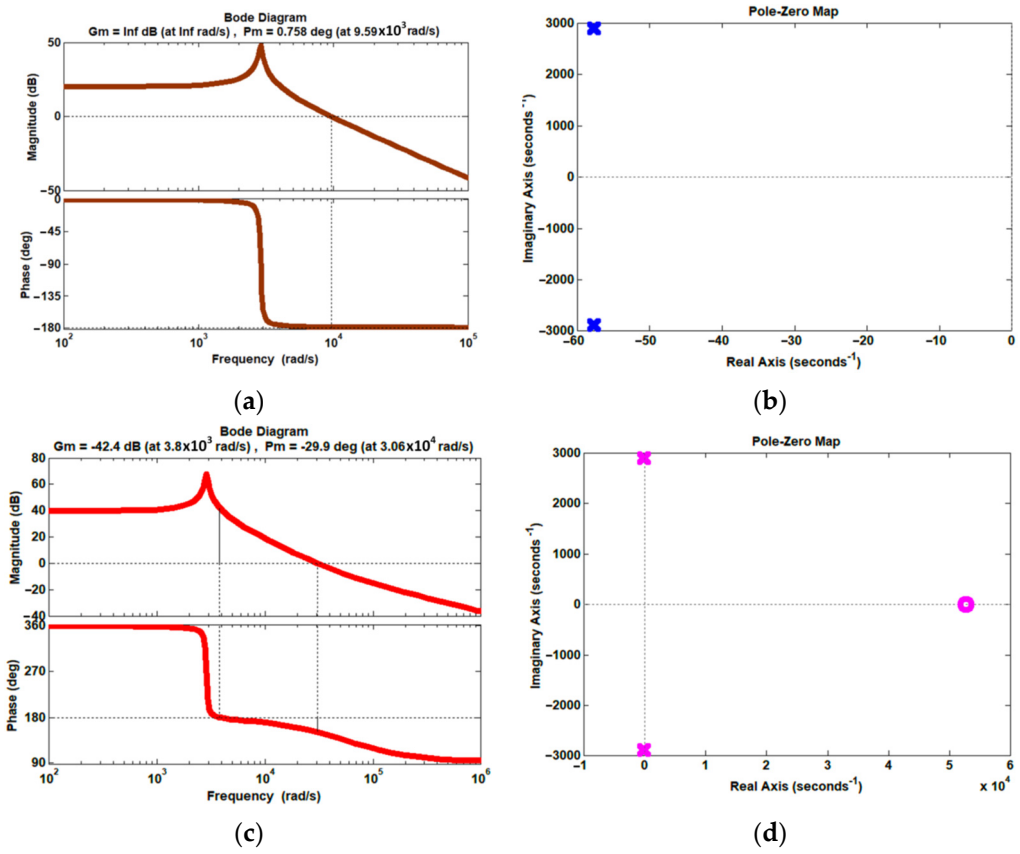


Figure 9. (**a**) Frequency response plot of derived topology; (**a**,**c**) Bode of Vo(s)/Vg(s) and Vo(s)/d(s); (**b**,**d**) Pole-zero plot of Vo(s)/Vg(s) and Vo(s)/d(s).

7. Reliability Analysis

7.1. Factors Affecting the Converter's Lifetime

More than 80% of the system cost is spent on the converter if a failure occurs. Therefore, estimating the reliability of the converter is requisite before the installation of the system. This section introduces the role and impact of various components of the system in the reliability study. This provides a deep insight into the parameters involved in the reliability estimation of the system. The reliability, as mentioned earlier, revolves around the failure rate of the different components in the converter circuit provided in Figure 10a,b. The power semiconductor devices and its failure rate play a vital role and have a greater impact on the system's entire reliability depending majorly on the converter reliability. This, in turn, depends on the components connected. Therefore, the calculation of the component's failure rate and the converter's reliability is the main objective of this section.

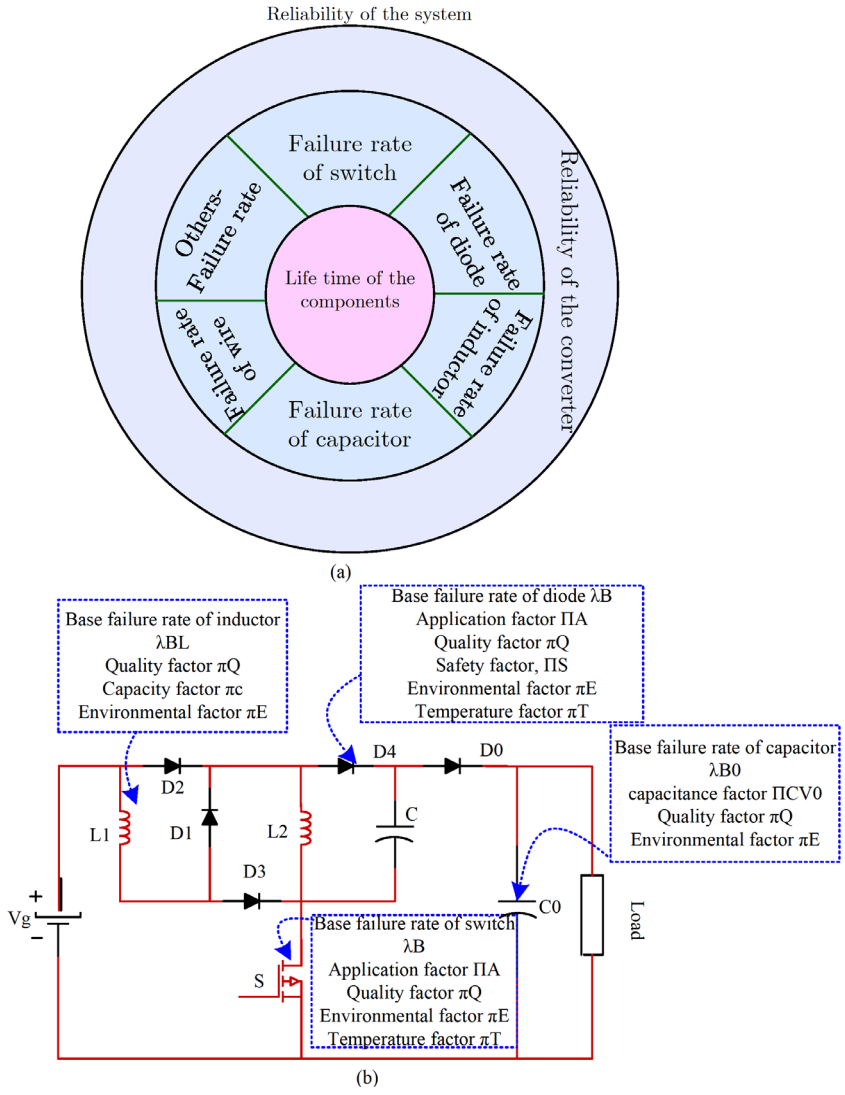


Figure 10. (**a**) Factors affecting the lifetime of the system and (**b**) Parameters influencing converter component's reliability.

The study carried out on the reliability predetermines the lifetime of the system using the equations as presented in (36)–(45).

Switch:

$$\lambda_{SW} = \lambda_B * \pi_T * \pi_A * \pi_S * \pi_Q * \pi_E \quad (36)$$

$$T_j = T_c + \theta_{jc} P_{SW} \quad (37)$$

$$\pi_T = e^{-1925\left(\frac{1}{T_j+278}-\frac{1}{298}\right)} \tag{38}$$

$$\lambda_{SW} = 1.38e^{-1925\left(\frac{1}{318+25.7\left(\frac{D^2}{(1-D)^2}\left(\frac{0.093(1+2D)^4}{(1-D)^2}+\frac{1}{61.7}\right)\right)}-\frac{1}{298}\right)} \tag{39}$$

Diode:

$$\lambda_D = \lambda_B * \pi_T * \pi_A * \pi_S * \pi_Q * \pi_E \tag{40}$$

$$\pi_T = e^{-3091\left(\frac{1}{T_j+273}-\frac{1}{298}\right)} \tag{41}$$

$$\lambda_D = 0.0147e^{-3091\left(\frac{1}{98+P_D}-\frac{1}{298}\right)} \tag{42}$$

$$P_D = \frac{1+2D}{1-D}\left(\left(\frac{1+2.5D}{1-D}\right)11.4+\left(\frac{4-D}{1-D}\right)1.14\left(\frac{1+2D}{1-D}\right)\right) \tag{43}$$

Inductor:

$$\lambda_L = 0.0014e^{\frac{\left(298+0.08\frac{(1+2D)^2}{(1-D)^4}\right)}{409}} \tag{44}$$

Capacitor:

$$\lambda_C = 0.028 * 10^{-6} \text{ hours} \tag{45}$$

7.2. Impact of Failure Rate of Switch and Diode

The impact of varying the duty cycle on the failure rate of the switch and diode is shown in the graph below. The optimum selection and operation of the duty cycle are vital in deciding the lifetime of the power semiconductor devices, as shown in Figure 11a,b. The failure rate switch and diode characteristics are plotted for various values of duty cycle.

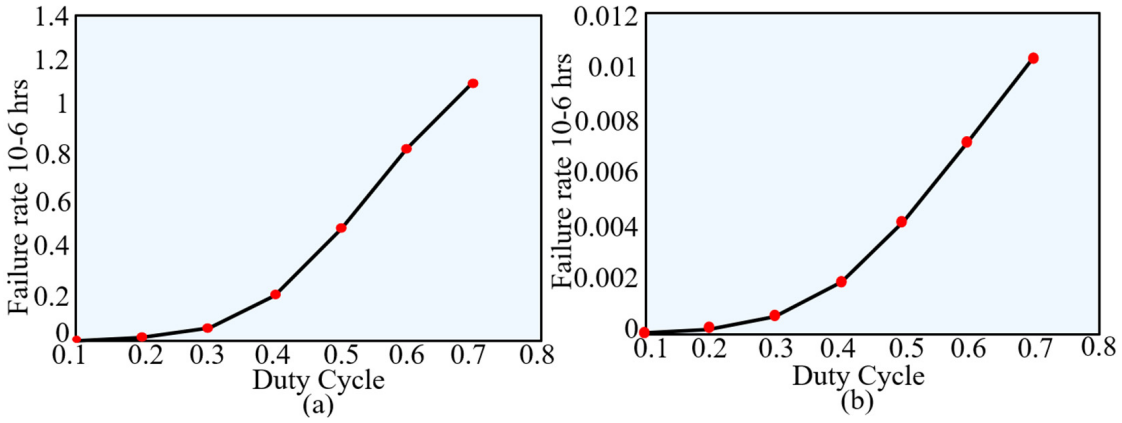


Figure 11. Failure rate (**a**) Switch; (**b**) Diode.

The analysis shows that the failure rate of the power switch in the converter has the highest rate of failure compared to the other components in the circuit. Therefore, to achieve better reliability, the failure rate of the switch must be reduced. The failure rate of the switch depends on the power loss in the switch, voltage, and current stress across the switch. Selecting the proper rating of the switch can avoid the losses and derating of the converter. This also reduces the failure rate of the switch. Thus, this section provides information about the reliability analysis of the converter and its importance. Further investigation and necessary actions to be performed to improve reliability are the future scopes of this study.

8. Comparative Analysis

The comparative analysis of the key performance metric parameters considered in the proposed converter and the existing converters are listed in Table 4. It is seen that the

proposed converter has fewer component counts and switch voltage stress compared to super lift converter [18] and AH-SLC [20]. As the voltage gain increases, the number of inductors required in the proposed converter is half of that required for converters in [10,11] as shown in Figure 12a.

Table 4. Comparison of HSIVL converter with few high gain converters in the literature.

Ref	Number of Components				Voltage Gain	Switch Voltage Stress	Voltage Gain Expansion
	Diode	Switch	Capacitor	Inductor			
Proposed topology	2 + 3N	1	2	1 + N	$\frac{1+2ND}{1-D}$	$V_O - V_g$	Yes
Super-lift	1 + 3N	1	1	1 + N	$\frac{1+ND}{1-D}$	V_O	Yes
Active–passive SL	2N	N + 2	1	2 + N	$\frac{1+(1+N)D}{1-D}$	$\frac{V_O}{1+2D}$	Yes
AH-SLC	4	2	1	3	$\frac{1+2D}{1-D}$	$\frac{1+2G_V V_g}{3}$	No
PSL converter	4	1	1	2	$\frac{1+D}{1-D}$	V_O	Yes
Modified SL Boost	3	2	1	2	$\frac{1+D}{1-D}$	$\frac{V_O}{2}$	Yes
Hybrid SL	4	2	1	3	$\frac{1+2D}{1-D}$	$\frac{V_O}{3G_V}(2+G_V)$	Yes
Active SL	2	2	2	2	$\frac{2}{1-D}$	$\frac{V_O}{2}$	Yes

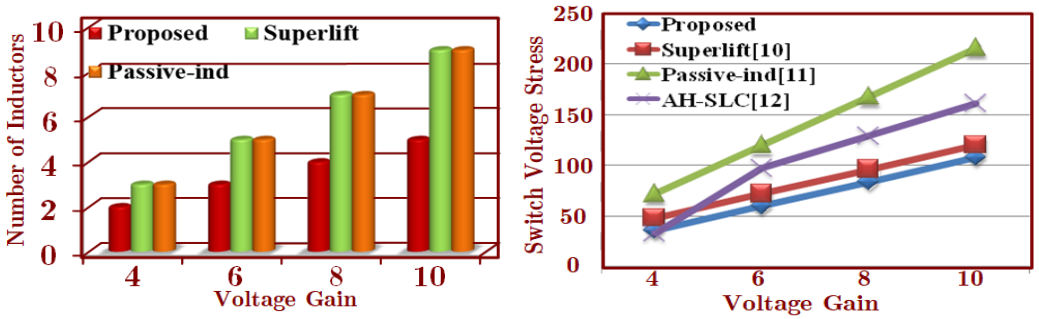


Figure 12. Comparative analysis: (**a**) Voltage gain vs. number of inductors. (**b**) Voltage gain vs. Voltage stress across the switch (S).

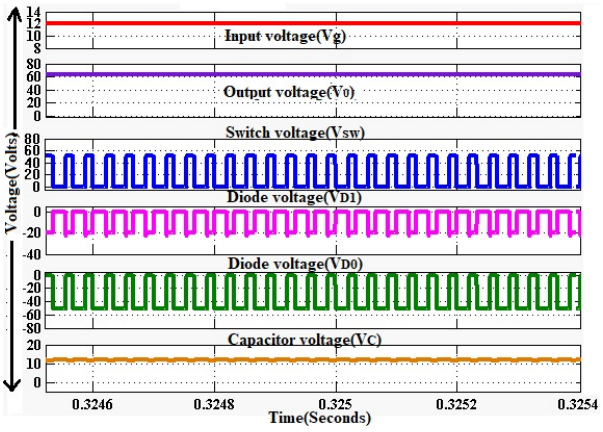
The switch voltage stress in the proposed converter is only 50% of the converter in [19] and 75% as the converter in [20], which is revealed in Figure 10b. Moreover, the proposed topology has a scope for voltage gain expansion, which is not possible in the converter provided in [20]. For voltage gain > 5, the HSIVL converter has a lower increase in the number of inductors compared to the converters [18,19] used for the comparison. The proposed converter is not compared with converter [20] for the number of inductors due to the fixed number of inductors in that converter [20]. Furthermore, the proposed converter is also compared with other performance metrics such as the voltage gain and switch voltage stress. Similarly, the HSIVL converter has lower voltage stress for higher voltage gain compared to other converters in the literature where the voltage stress is equal to the output voltage. Moreover, the firm features of the HSIVL converter are highlighted by further comparing with the converters presented in [21–23]. All the topologies considered for comparison have component counts more or less similar to the proposed topology. The gain is observed to be similar to the converters considered [21–23] for study.

Several topologies are derived with extendable form either in increasing the turns ratio of the coupled inductor in the converter [35] and adding N number of voltage multiplier cells [36]. In [36], the voltage gain of the converter is (N + 1)D/(1 − D) with the component count of 11, whereas the proposed topology presents the voltage gain of (1 + 2ND)/(1 − D).

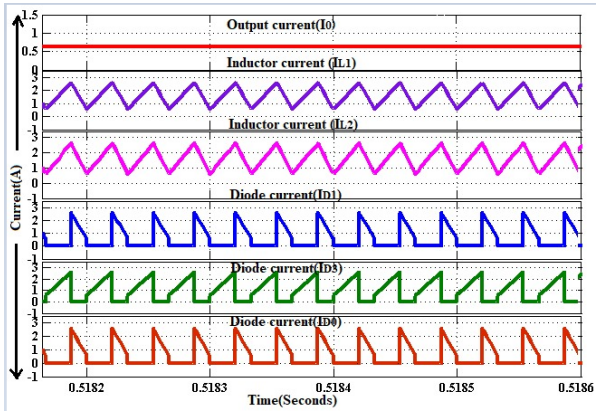
From this comparison, it is observed for N = 1 and D = 0.5 that the proposed HSIVL topology provides the gain twice that of the converter in [36] with a lower component count.

9. Simulation and Experimental Results

This section discusses the simulation results followed by hardware results. The derived topology is simulated in MATLAB-Simulink software and the results are presented in Figure 13a,b. Figure 13a depicts the output voltage, switch voltage, diode voltage, and capacitor voltage waveforms of the HSIVL converter. The current through the components of the converter is illustrated in Figure 13b. The proposed converter specifications for simulation are chosen as: Vg = 12 V, V_O = 66 V, D = 0.5, f_S = 50 kHz, L_1 = L_2 = 50 µH, R_O = 87 Ω, C = 100 µF, and C_O = 100 µF. The illustrated simulated waveform shows an output voltage of 65.5 V for an input voltage of 12 V. Finally, it is validated by testing the prototype in the laboratory. The switch voltage waveform shows that the switch stress is less than the output voltage. The switch and capacitor current with a high value of ESR to reduce the impulse is presented in Figure 13c. The suitability of the converter for higher voltage is depicted in Figure 13d with 48 V input voltage, 832 V output voltage, D = 0.7, and the number of expander cells N = 3. Finally, the transient response of the converter is observed by performing step changes in the input port and the results are depicted in Figure 13e.



(**a**)



(**b**)

Figure 13. *Cont.*

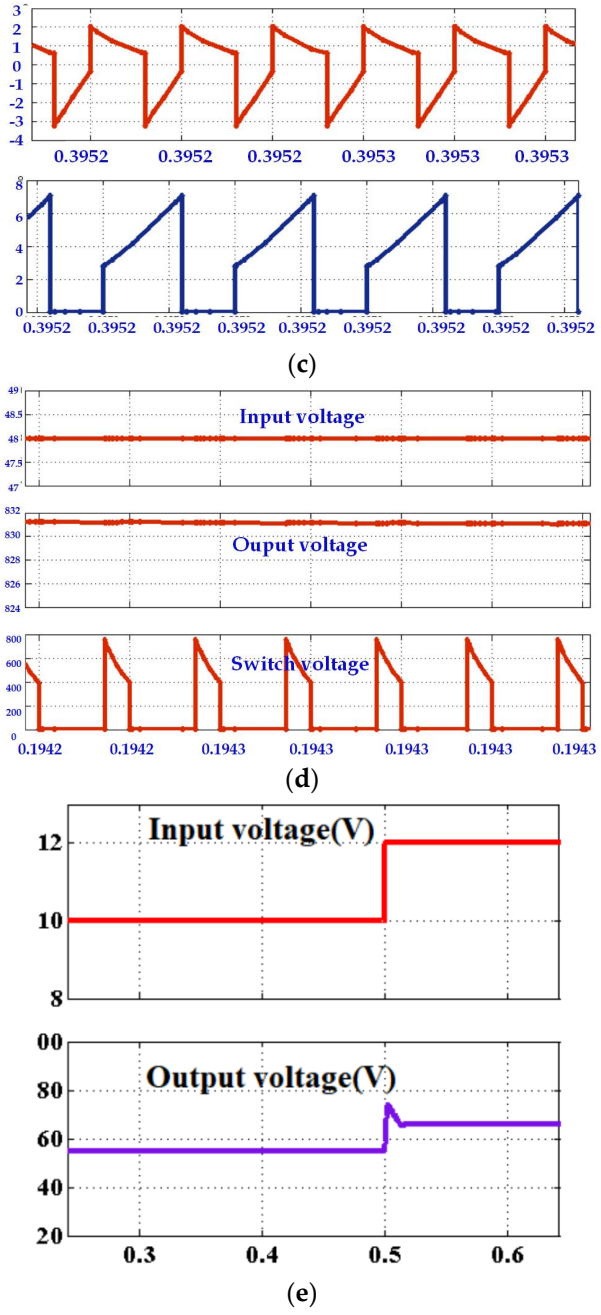


Figure 13. Comparative analysis. Key simulation results of HSIVL converter at 50 Watts. (**a**) Simulated voltage waveform, (**b**) Simulated inductor and diode current waveform, (**c**) Capacitor and switch current waveform, (**d**) Input, output, and switch voltage with N = 3 and D = 0.7 for higher voltage application. (**e**) Input and Output voltage with step change.

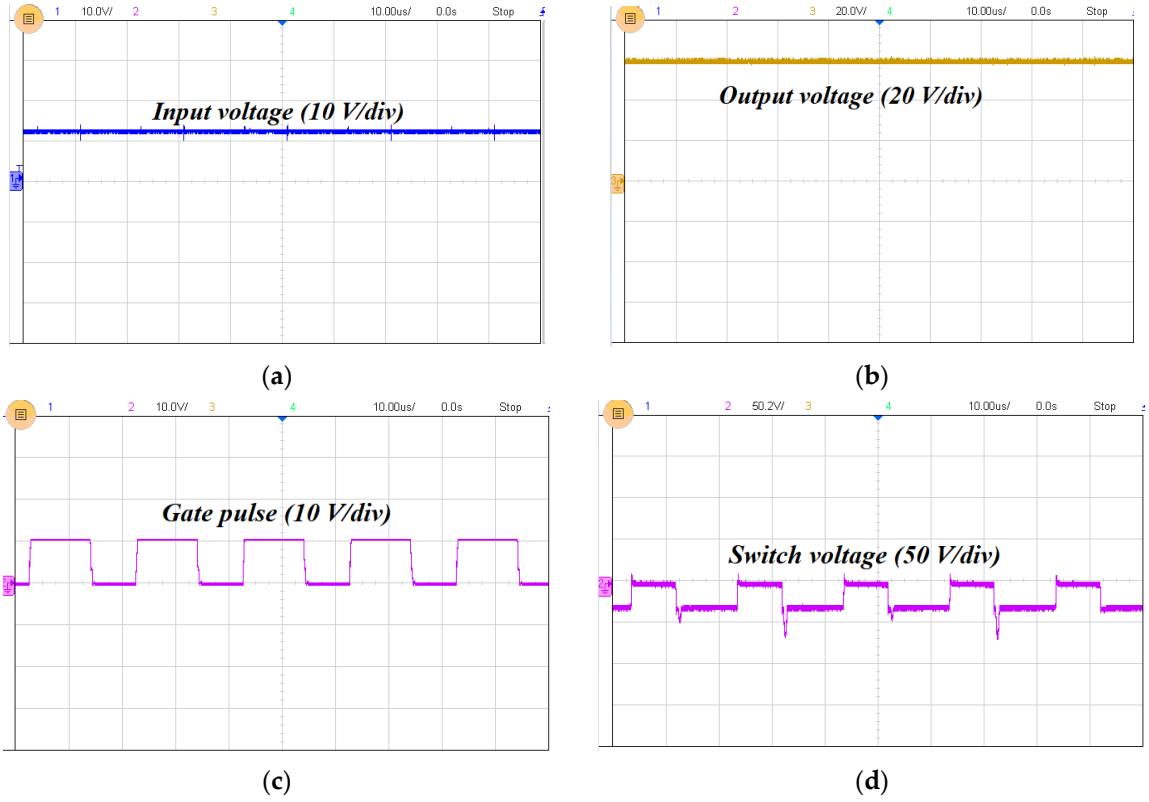
A 50 W prototype circuit with the specifications mentioned in Table 5 is implemented to validate the theoretical analysis of the derived converter and it is presented in Figure 14a–h. Figure 14a,b show the input and output voltage for a duty cycle of 0.6. Figure 14c,d depict the gate pulse and switch voltage of the HSIVL converter. It is observed that the maximum switch voltage is $(2V_O + Vg)/3$.

It is also noted that the voltages of diodes (D_1–D_4) and capacitor (C) are equal to the input voltage. This depicts that the stress on the diodes is much lower and it is independent of the boosted output voltage; these are illustrated in Figure 14e,g. The output diode voltage is presented in Figure 14f, which is equal to the difference of output and input voltage. The inductor voltage is presented in Figure 14h. The photograph of the tested

hardware is shown in Figure 14i. Finally, the whole setup implemented for validating the theoretical analysis is presented in Figure 14j.

Table 5. Specification and components for experimental setup.

Components	Specifications
Vg (input voltage)	12 V
V_O (output voltage)	66 V
P_O (power rating)	50 W
Duty cycle, D	0.6
f_S (switching frequency)	50 kHz
Inductors (L_1 and L_2)	100 uH, Torroidal core
Capacitors (C and C_O)	100 µF/200 µF, Electrolytic
MOSFET	IRF460P
Diode	VS-30PT100
Microprocessor	dsPIC 30F2010
Driver Circuit	TLP250



(**a**) (**b**)

(**c**) (**d**)

Figure 14. *Cont.*

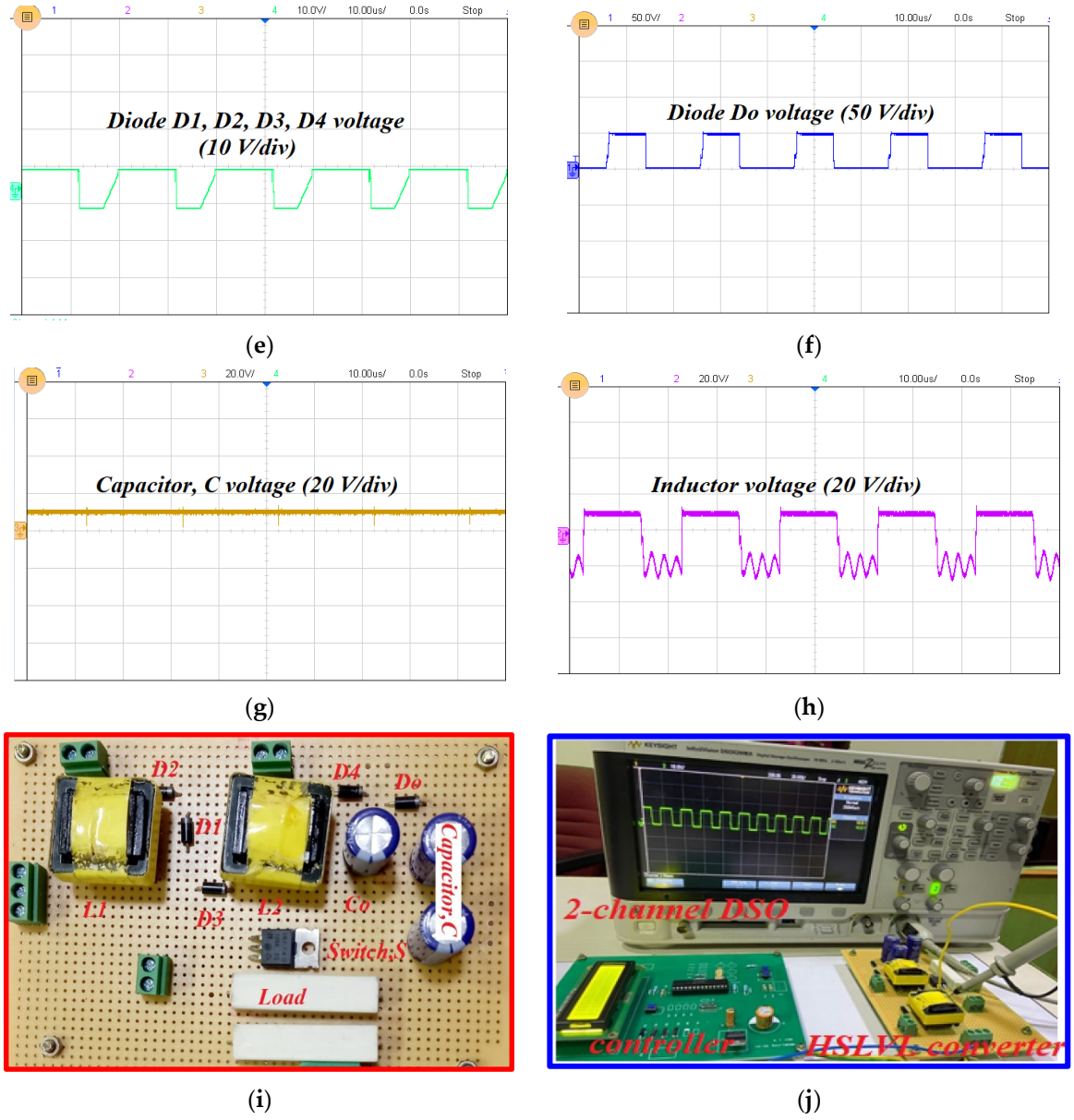


Figure 14. Test results. (**a**) Input voltage, (**b**) Output voltage, (**c**) Gate pulse, (**d**) Switch voltage stress, (**e**) Diode (D_1–D_4) voltage, (**f**) Output diode Do voltage, (**g**) Capacitor C voltage, (**h**) Inductor voltage (100 µs/div), (**i**) Photograph of the HSIVL converter tested, and (**j**) Entire setup implemented for validation.

The maximum voltage across the diodes (D_1, D_2, and D_3) is equal to the supply voltage, Vg, which is illustrated in Figure 14c. The voltage across the output diode is similar to the switch voltage, which is depicted in Figure 9d. It is seen that the inductor currents (I_{L1}, I_{L2}) are continuous, which are presented in Figure 14e. Table 6 validates the HSIVL converter. It is observed from Figure 15 that the efficiency of the converter starts to droop when the output power of the converter increases. Since the component count is less and the switch voltage stress is Vo–Vg, the efficiency of the converter is observed to be theoretically high. Figure 15 provides the efficiency curve for various loads that are calculated theoretically. The efficiency at the rated load is 95.8%, which can be observed from Figure 15. On average, the HSIVL converter shows 95% efficiency for various output powers.

Table 6. Comparison between theoretical, simulation, and experimental results.

Parameters	Theoretical (V)	Simulated Values (V)	Experimental Values (V)
P_O = 50 W, Vg = 12 V, D = 0.6, fs = 50 kHz			
Output voltage, V_O	66	65.5	65
Switch voltage stress, V_{SW}	48	47.5	46
Diode voltage stress, V_{D1}	12	12	11.5
Diode voltage stress, V_{DO}	54	53.5	52
Efficiency	96.2%	96.0%	95.0%

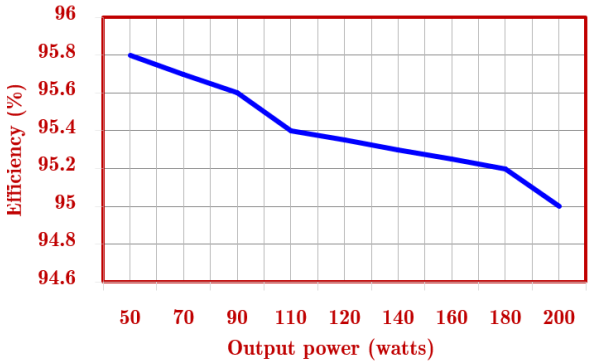


Figure 15. Efficiency versus output power.

10. Conclusions

A novel hybrid power converter structure with a switched inductor and voltage-lift cell was derived and analyzed. The proposed topology uses lower voltage stress on the switches and diodes, which further minimizes the cost of the converter confirmed by the analysis and experimental results. The voltage stress across the output diode in most of the high gain dc–dc converter is equal to the output voltage. In the derived topology, the stress across the output diode of the derived topology is the difference of output and input voltage, which reduces the cost and increases the reliability of the component. According to the military handbook for reliability prediction, the failure rate of the diode depends on the voltage stress ratio. Hence, the reduction in maximum voltage stress increases the maximum time to failure of the component. The switching and conduction losses are analyzed and it shows that the proposed topology offers low losses due to lower number of power components. The significant factors affecting the lifetime of the converter are identified and analyzed. The reliability study helps us to find the optimum value of the duty cycle with respect to the failure rate of the passive and active components. To demonstrate the theoretical results, a 50 W prototype has been assembled in the laboratory. The experimental results have validated and proved that the proposed converter is suitable for high voltage gain applications such as photovoltaic systems, fuel cell, etc.

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Nomenclature

MPPT	Maximum power point tracking
PV	Photovoltaic
N	Number of expander cells
D	Duty cycle
Gv	Voltage gain
S	Stress ratio
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
λ_{SW}	Failure rate of the switch
λ_D	Failure rate of the diode
λ_L	Failure rate of the inductor
λ_C	Failure rate of the capacitor
π_T	Temperature factor
π_E	Environmental factor
π_S	Stress factor
π_Q	Quality factor
π_A	Application factor

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