60-GHz RF System Performance Optimization

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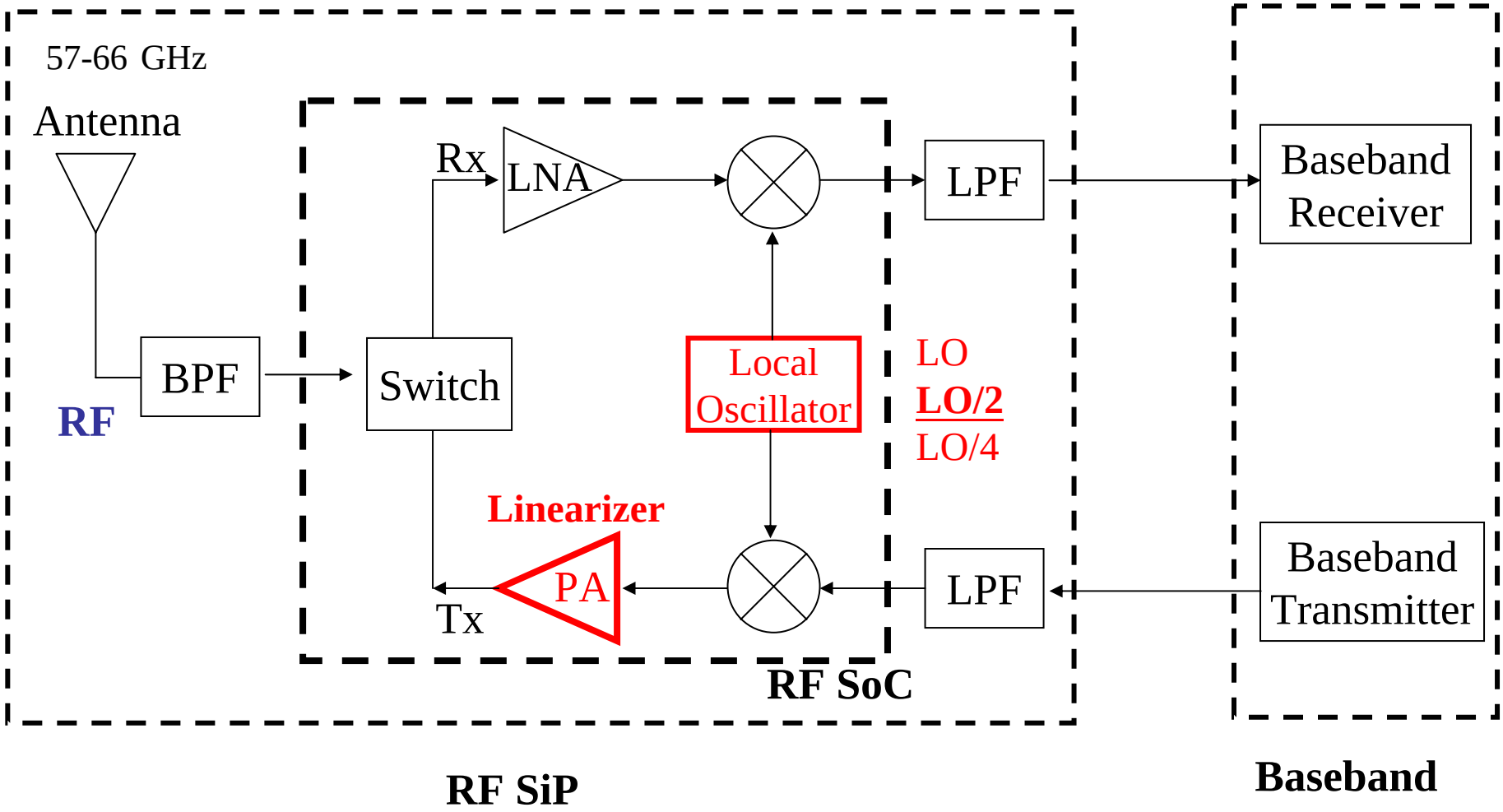
Abstract

- This presentation proposes two techniques to minimize the impact of RF impairments on the performance of 60-GHz multi-gigabit system.
- An example of 60-GHz 65-nm CMOS power amplifier pre-distortion linearizer is proposed for the optimization of multi-gigabit RF system linearity.
- A 60-GHz sub-harmonic local oscillator topology is also proposed for the 65-nm CMOS phase noise optimization.

Outline

- Introduction
- 65-nm CMOS PA linearity optimization
- 65-nm CMOS phase noise optimization
- Conclusions
- References

Introduction



Modified Rapp PA Modeling [1]

- **Input signal *x(t)* to an amplifier produces output signal *y(t)*:**

$$G(A) = g\frac{A}{\left(1+\left(\frac{gA}{A_{sat}}\right)^{2s}\right)^{\frac{1}{2s}}}$$

where

g is the small gain signal

s is the smoothness factor

A_{sat} is the saturation level

$$x(t) = A(t)\cos(2\pi f_c t + \theta(t))$$

$$y(t) = G[A(t)]\cos[2\pi f_c t + \theta(t) + \Psi(A(t))]$$

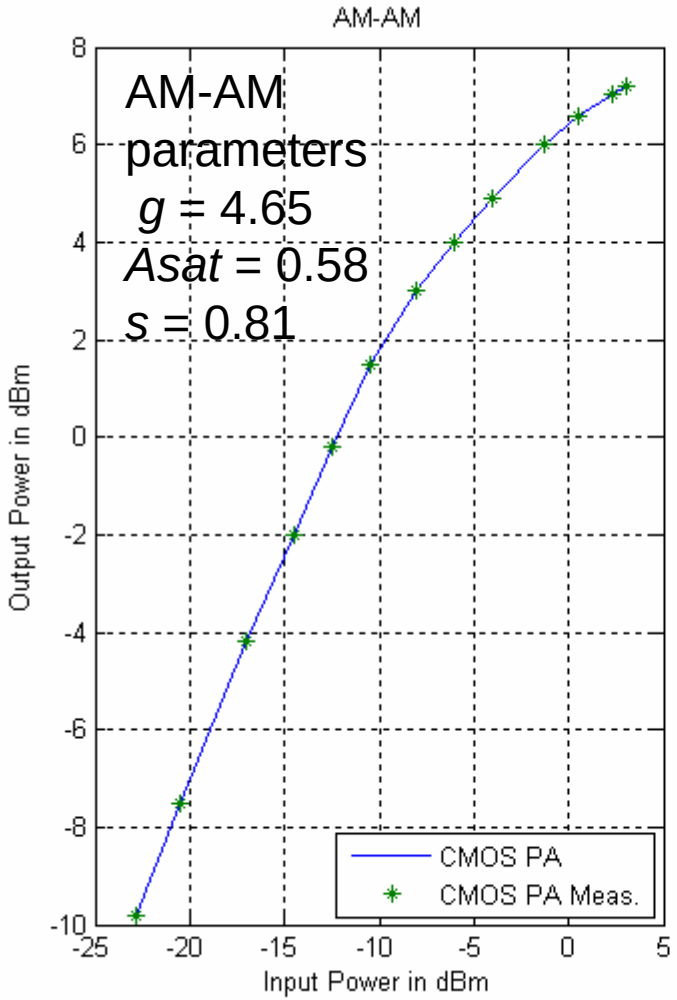
where

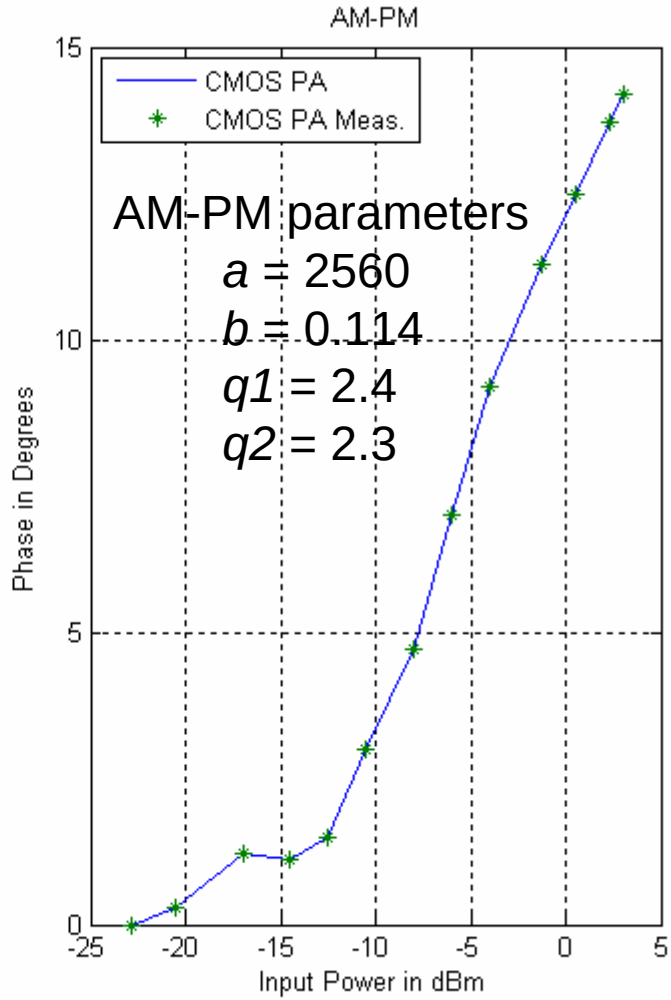
$G[A(t)]$ is the amplitude (gain) distortion (AM - AM)

$\Psi(A(t))$ is the phase distortion (AM - PM)

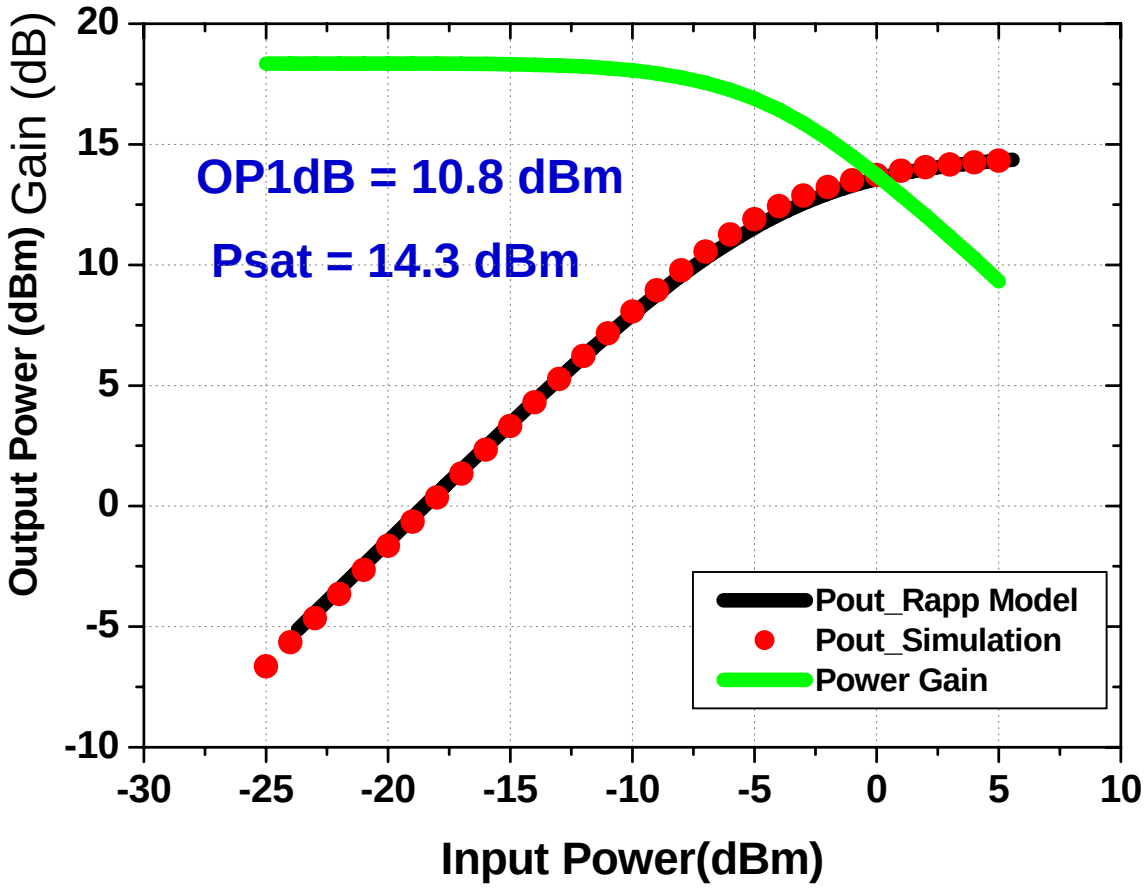
$$\Psi(A) = \frac{\alpha A^{q_1}}{\left(1+\left(\frac{A}{\beta}\right)^{q_2}\right)}$$

65nm CMOS Standard PA [1]





65nm CMOS NTU PA AM-AM VDD 1V



$$G(A) = g\frac{A}{\left(1+\left(\frac{gA}{A_{sat}}\right)^{2s}\right)^{\frac{1}{2s}}}$$

g is the small signal gain

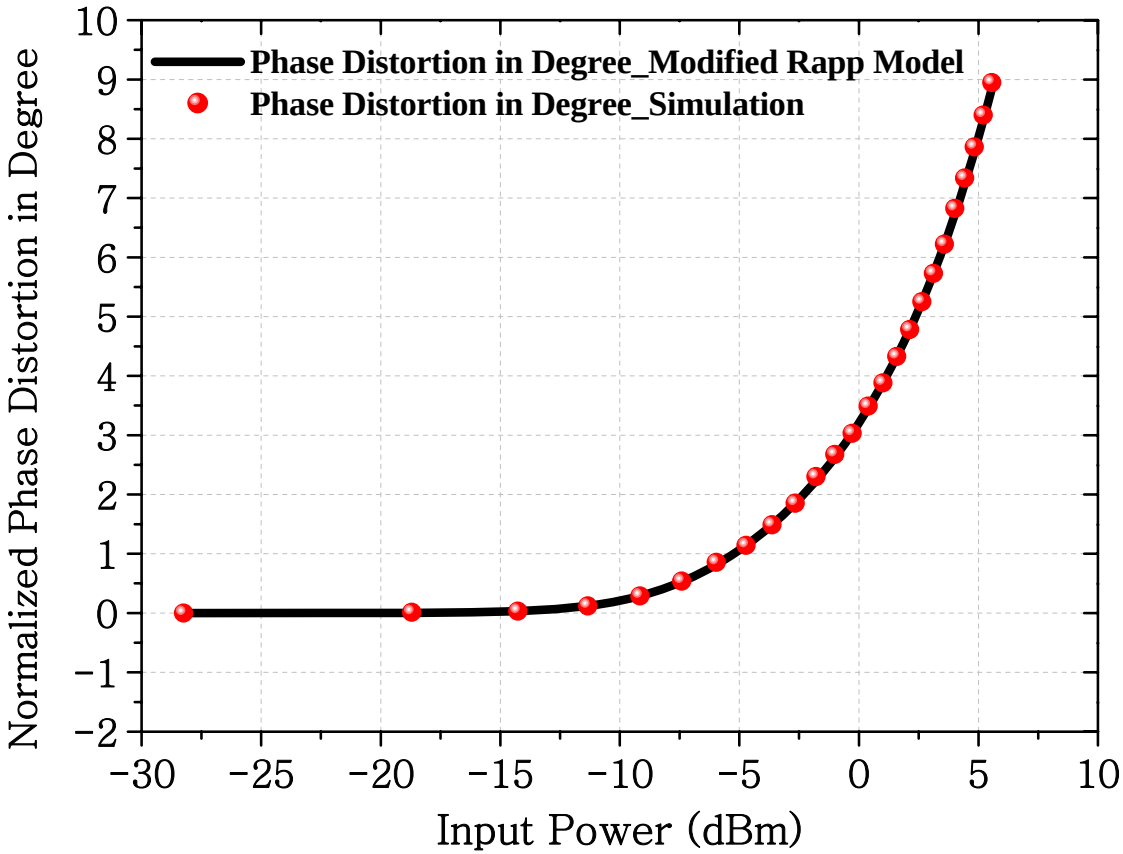
s is the smoothness factor

A_{sat} is the saturation level

g=8.5, s=1.2 ,Asat=1.7

PA simulation is using ADS and CMOS foundry model

65nm CMOS NTU PA AM-PM
VDD 1V



$$\Psi(A) = \frac{\alpha A^{q1}}{\left(1 + \left(\frac{A}{\beta}\right)^{q2}\right)}$$

q1=4.4 ,

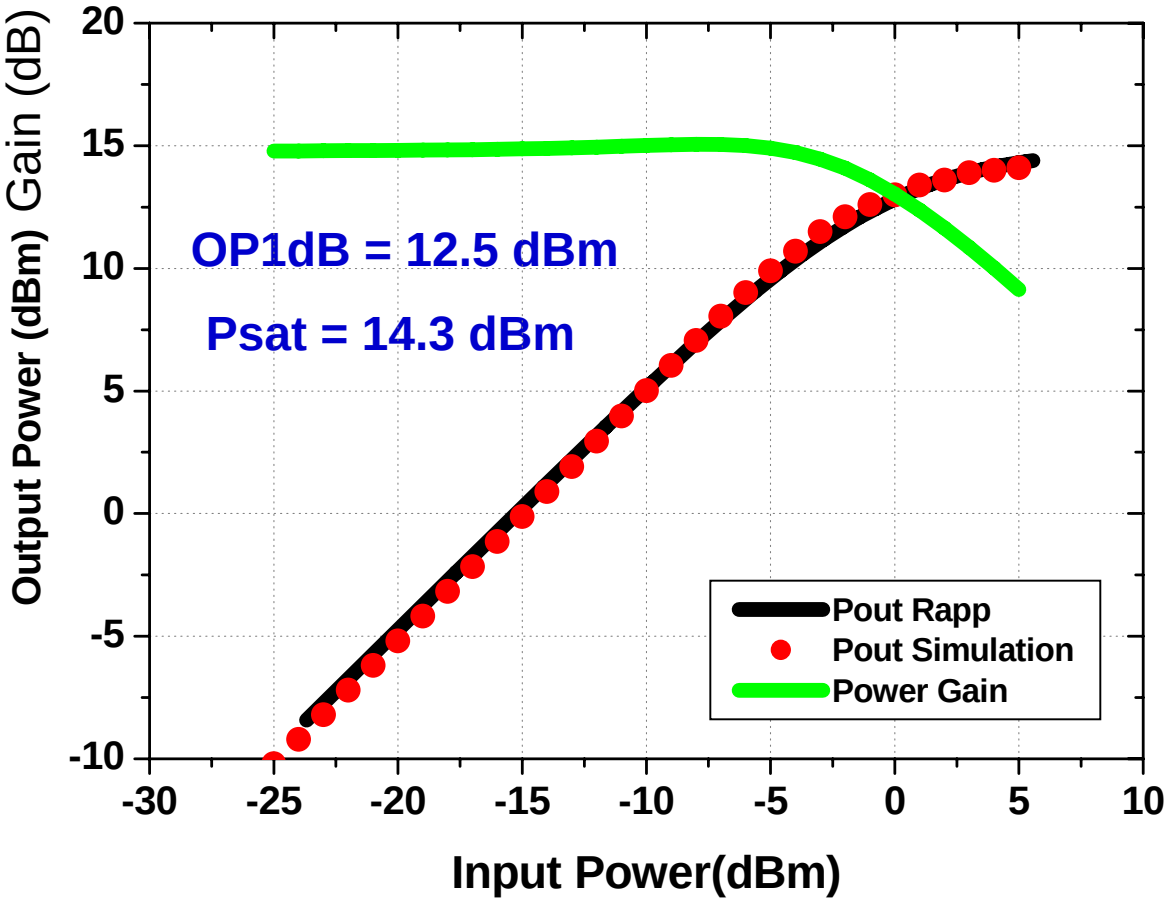
q2=3.0 ,

a=8000 ,

B=0.125

PA simulation is using ADS and CMOS foundry model

65nm CMOS NTU PA with Linearizer AM-AM VDD 1V



$$G(A) = g\frac{A}{\left(1+\left(\frac{gA}{A_{sat}}\right)^{2s}\right)^{\frac{1}{2s}}}$$

g is the small signal gain

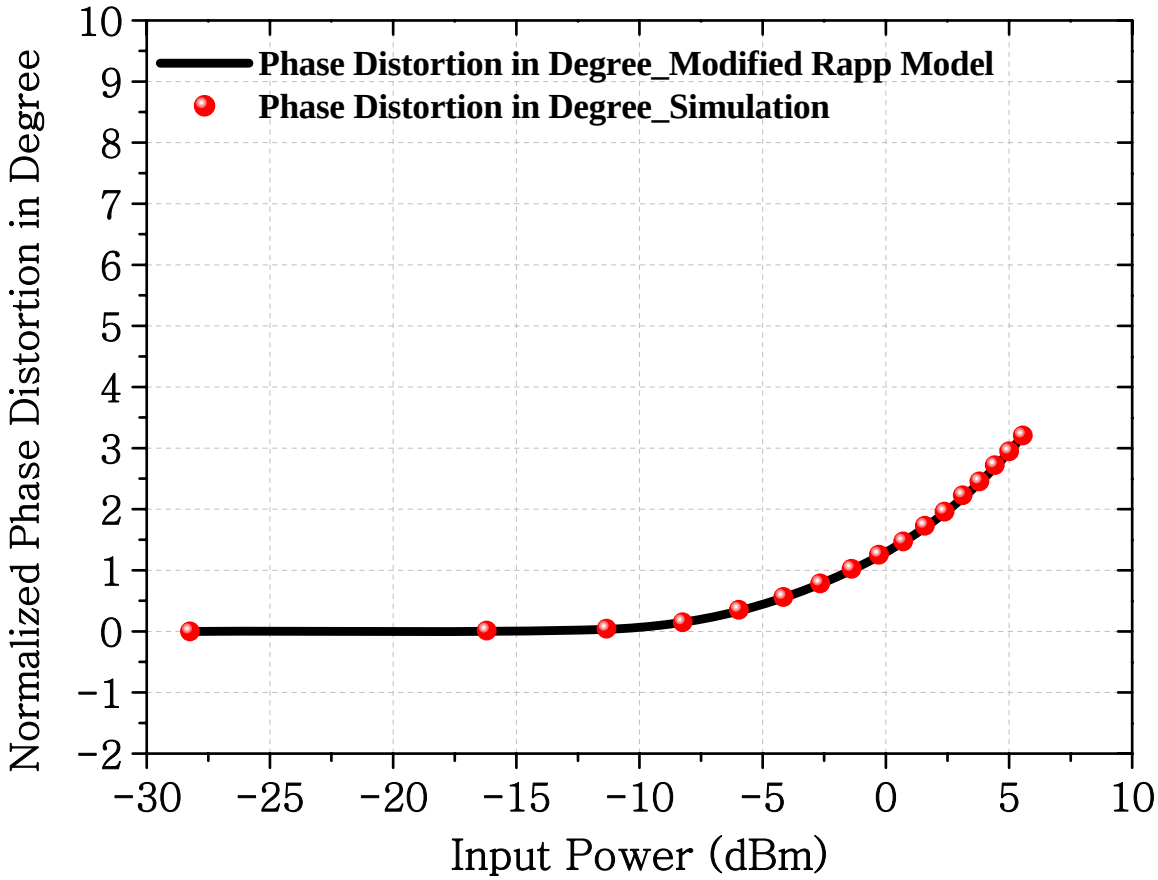
s is the smoothness factor

A_{sat} is the saturation level

g=5.8, s=1.35 ,Asat=1.75

PA simulation is using ADS and CMOS foundry model

65nm CMOS NTU PA With Linearizer AM-PM VDD 1V



$$\Psi(A) = \frac{\alpha A^{q1}}{\left(1 + \left(\frac{A}{\beta}\right)^{q2}\right)}$$

q1=4.5 ,

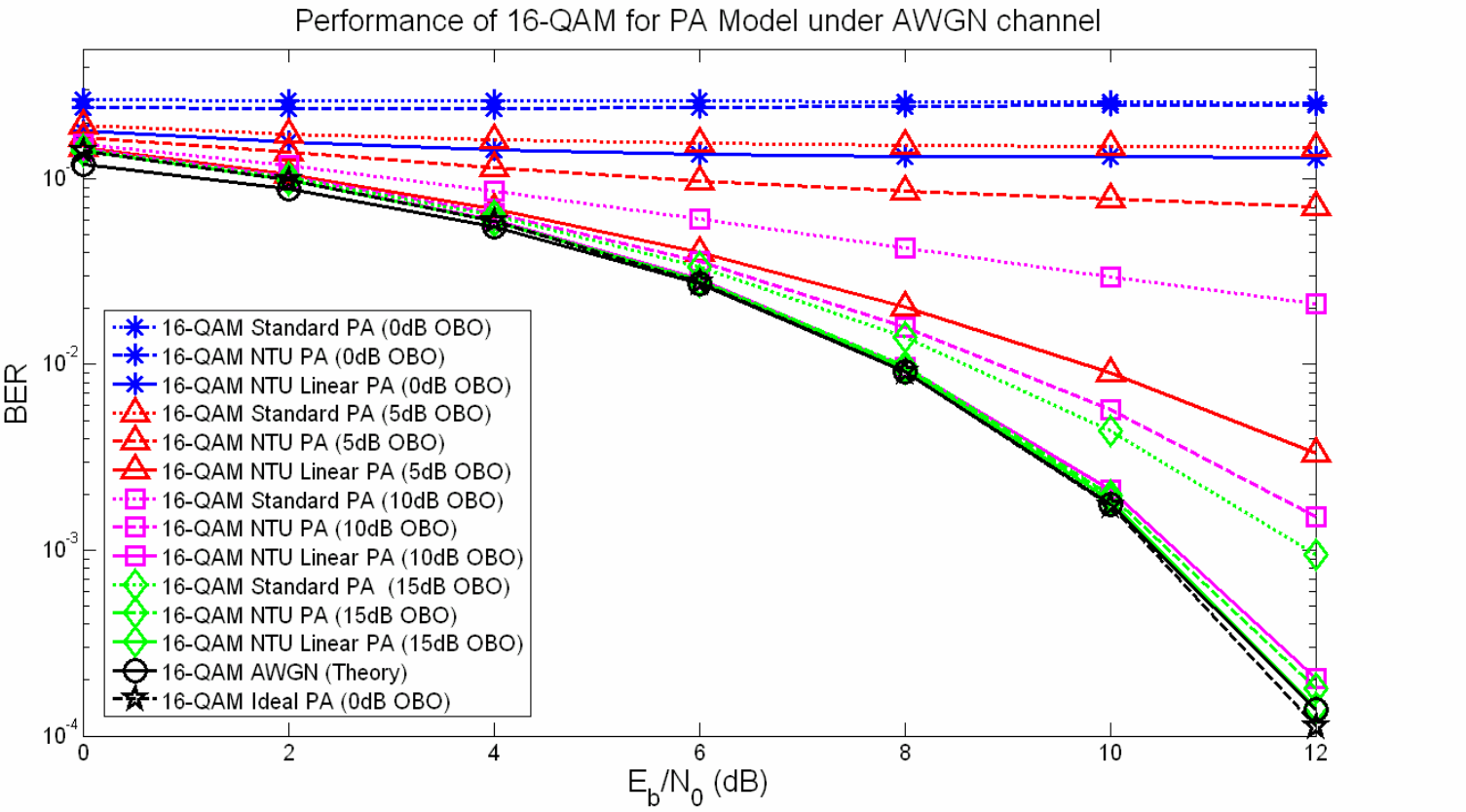
q2=3.2 ,

a=5000 ,

B=0.125

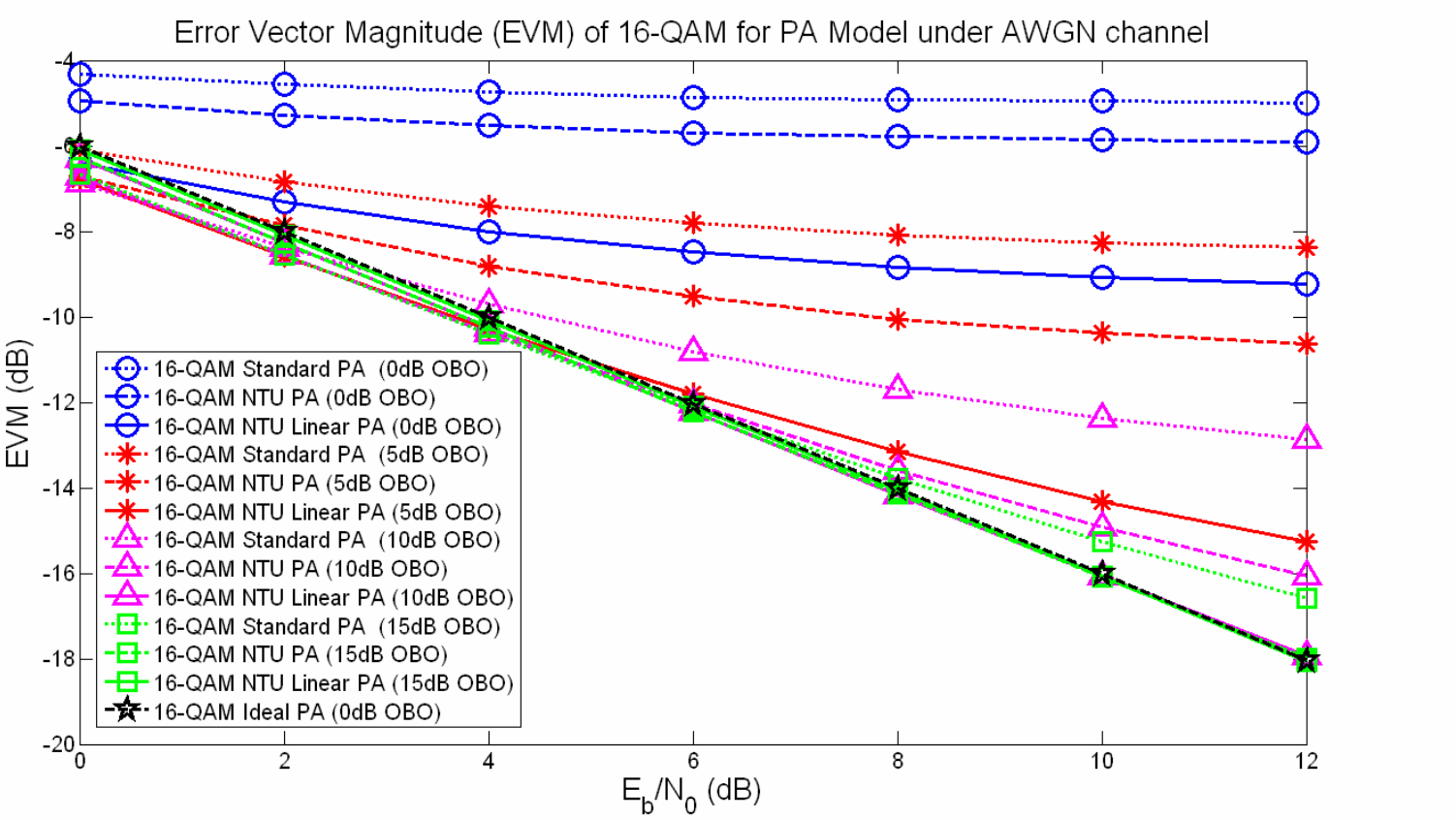
PA simulation is using ADS and CMOS foundry model

BER Peformance



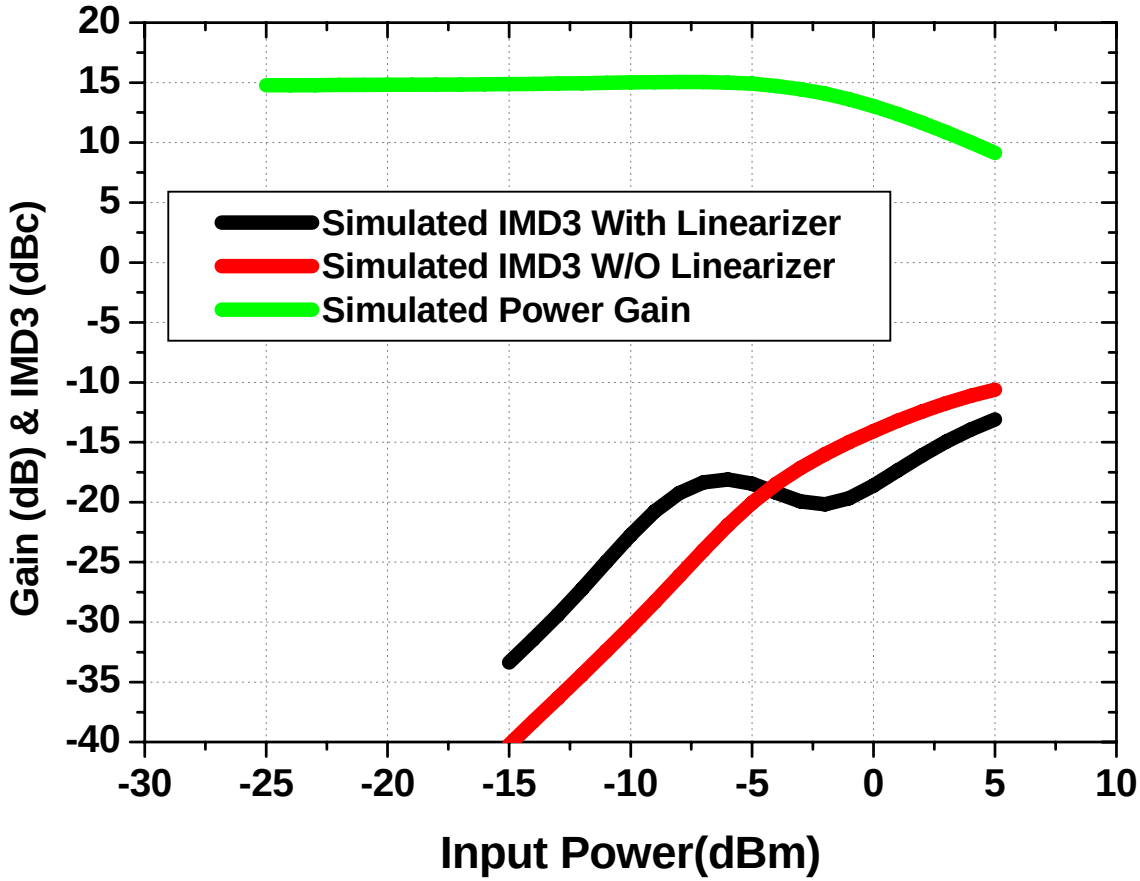
SC 16-QAM, 3Gbps

EVM Performance



SC 16-QAM, 3Gbps

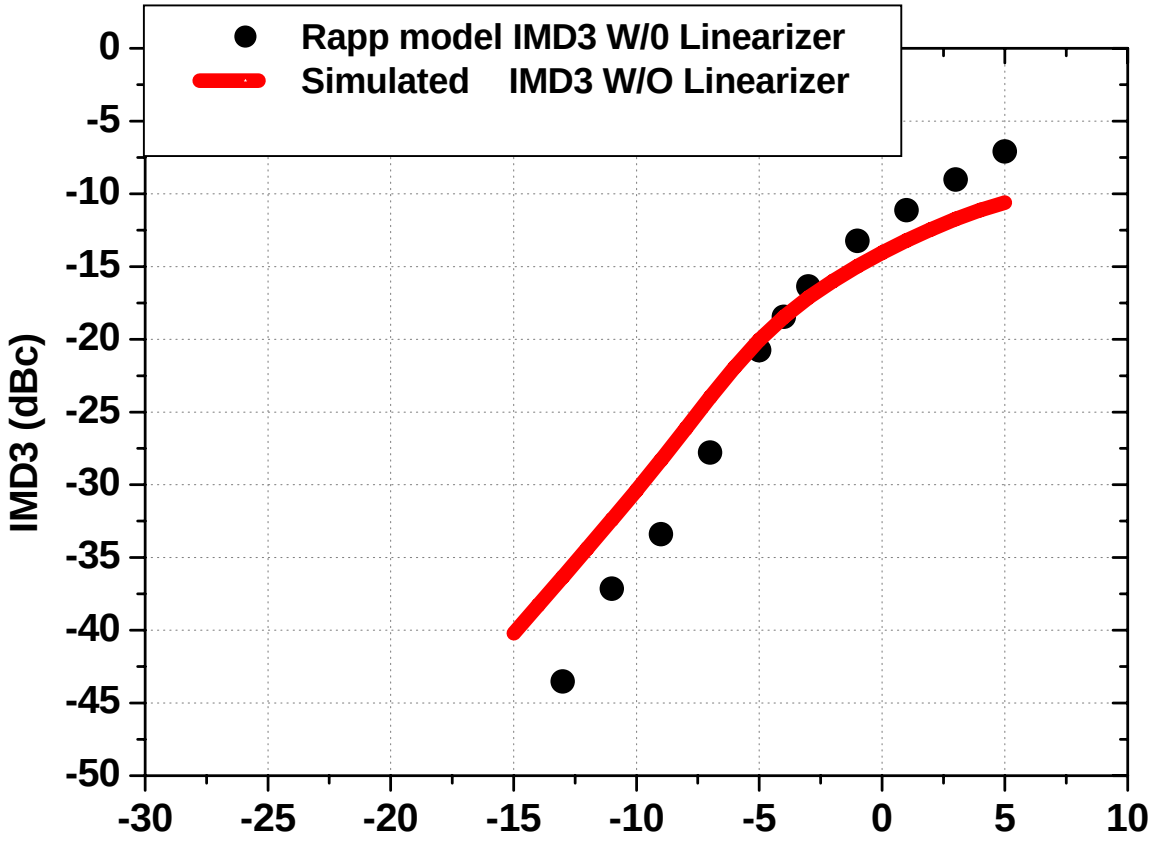
65nm CMOS NTU PA IMD3



Two tone frequency : 60GHz , 60.5GHz

PA simulation is using ADS and CMOS foundry model

Comparison of IMD3 for 65nm CMOS NTU PA Without Linearizer



Two tone frequency : 60GHz , 60.5GHz

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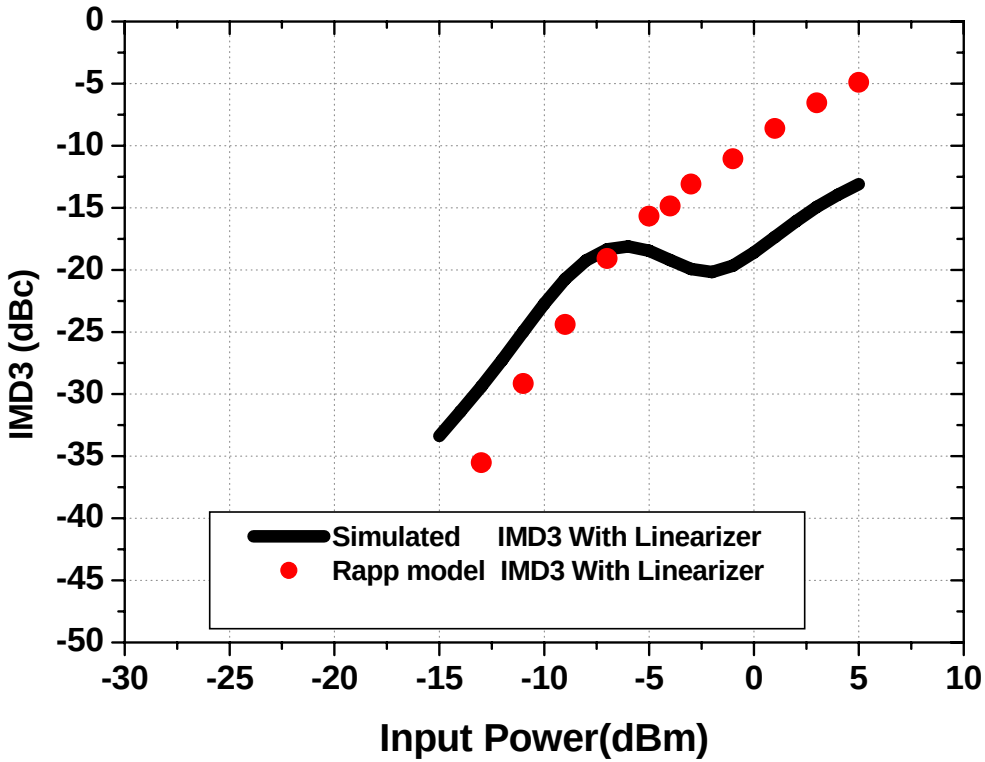
Comparison of IMD3 for 65nm CMOS NTU PA With Linearizer



$$v_{out} = \frac{v_{in}}{\left(1 + \left(\frac{v_{in}}{v_{sat}}\right)^{k}\right)^{\frac{1}{k}}}, \quad [3]$$

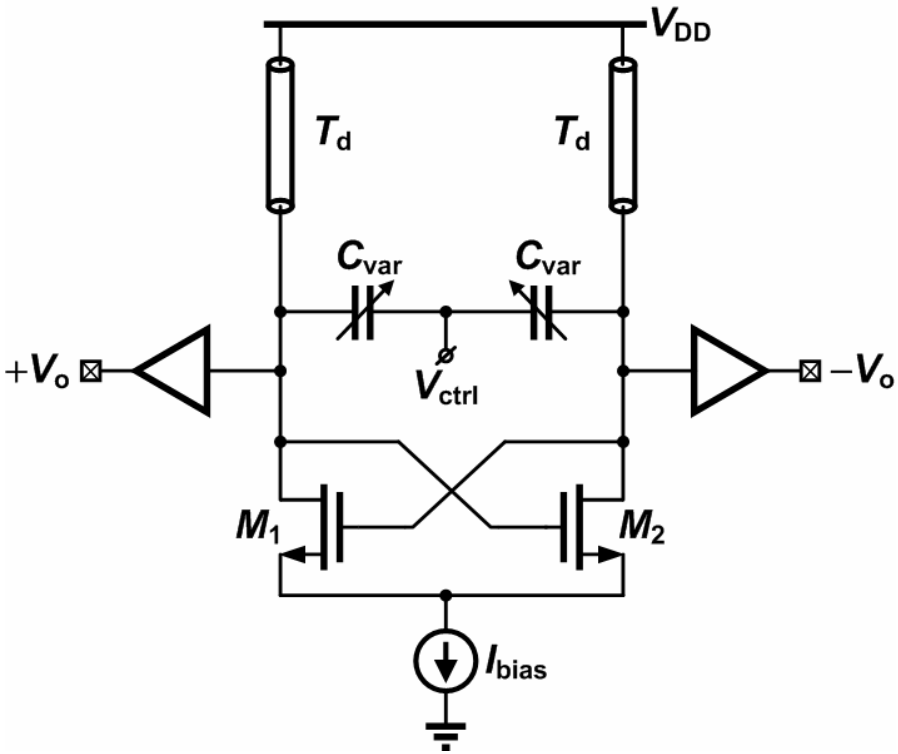
$$V_{out} = v_{in}\left\{1 - \frac{1}{k}\left(\frac{v_{in}}{v_{sat}}\right)^{k} + \left(\frac{1}{2}\right)\left(\frac{1}{k}\right)\left(\frac{1}{k}-1\right)\left(\frac{v_{in}}{v_{sat}}\right)^{2k} + \left(\frac{1}{6}\right)\left(\frac{1}{k}\right)\left(\frac{1}{k}-1\right)\left(\frac{1}{k}-2\right) \times \left(\frac{v_{in}}{v_{sat}}\right)^{3k} + \ldots\ldots\right\}.$$

Two tone frequency : 60GHz , 60.5GHz

PA simulation is using ADS and CMOS foundry model

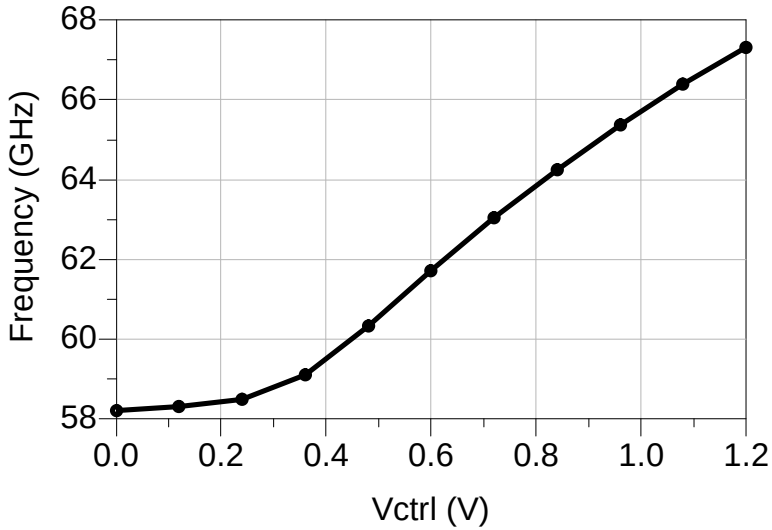
VCO Performances for LO (1/2)

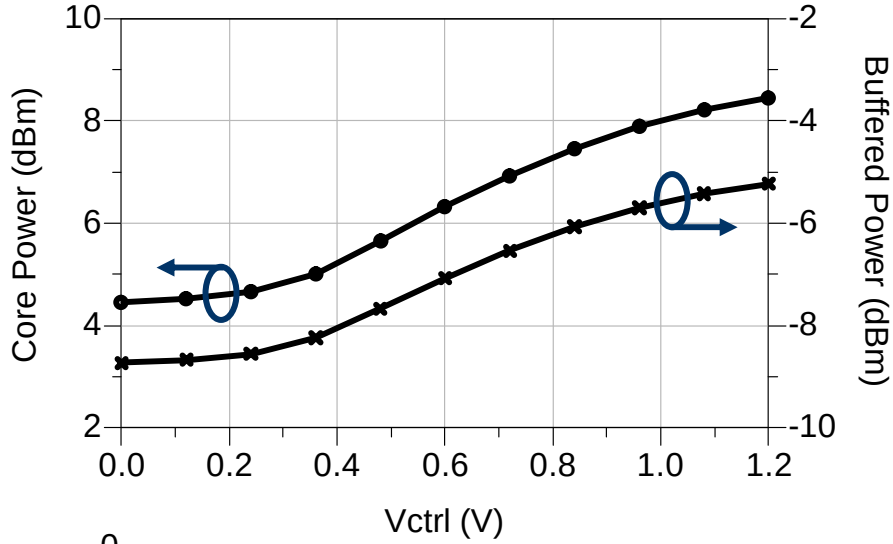
- Circuit Schematic & Design Parameters
  - **Based-on tuning requirement (6~8-GHz @60 GHz)**
  - **Design without band-switching for comparison**
  - **T_d: CPW with shielded ground**

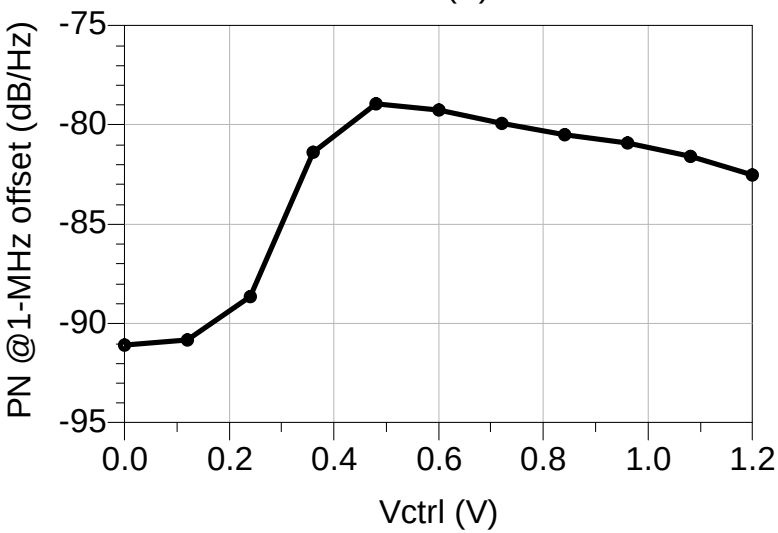


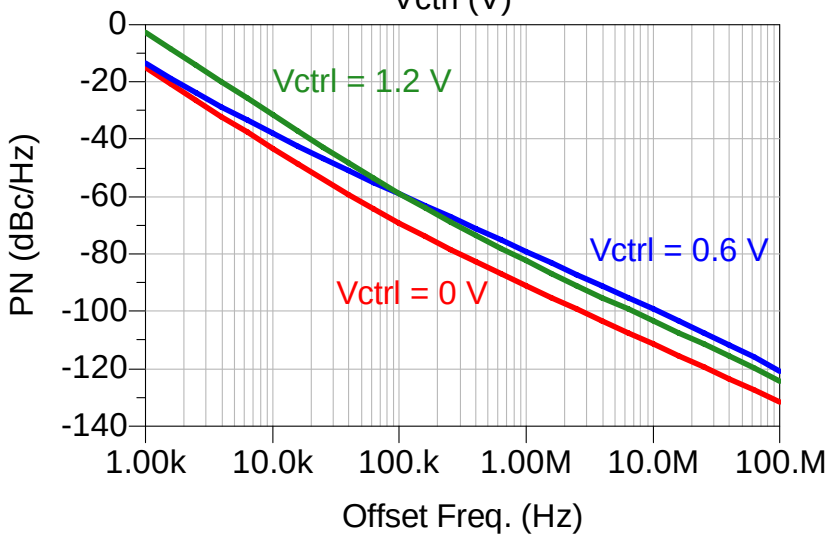
Device	Design Value	
M_1, M_2	1×8 μm / 0.06 μm	
I_{bias}	7.5 mA	
T_d	width	4 μm
	length	220 μm
	spacing	10 μm
	Z_0	57.7 Ω
C_{var}	21 ~ 46 fF	

VCO Performances for LO (2/2)



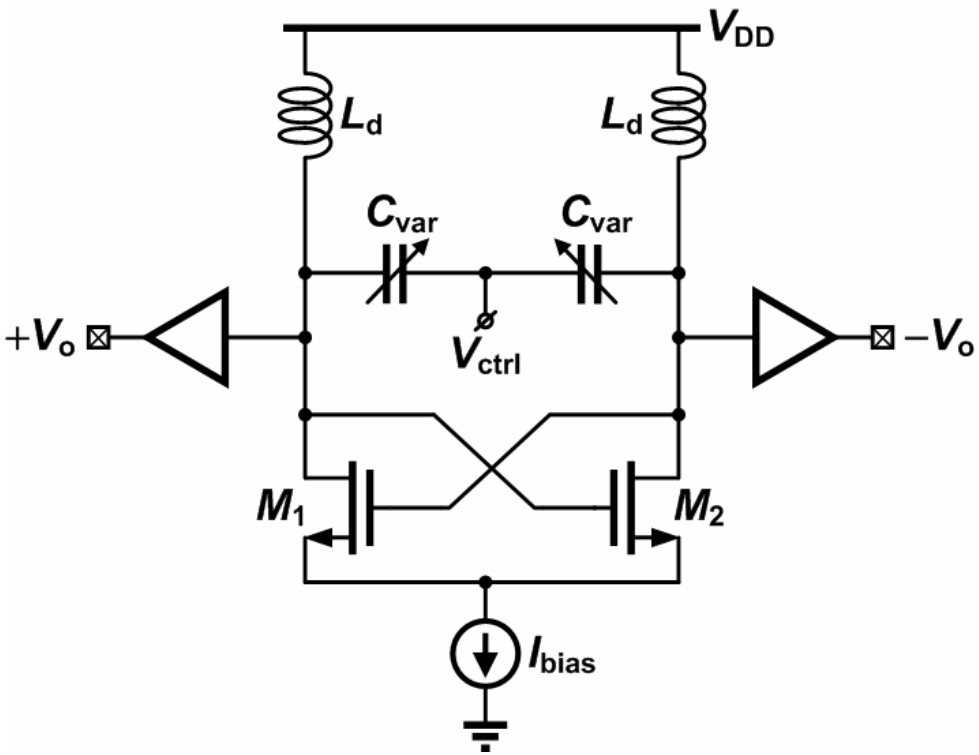






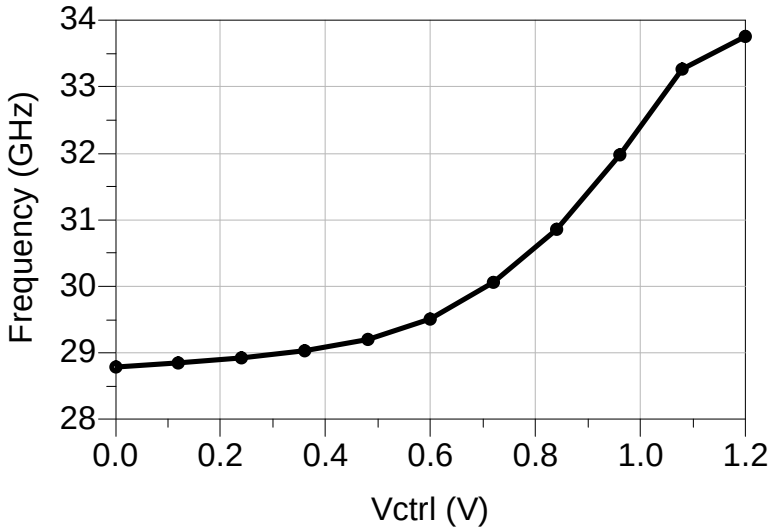
VCO Performances for LO/2 (1/2)

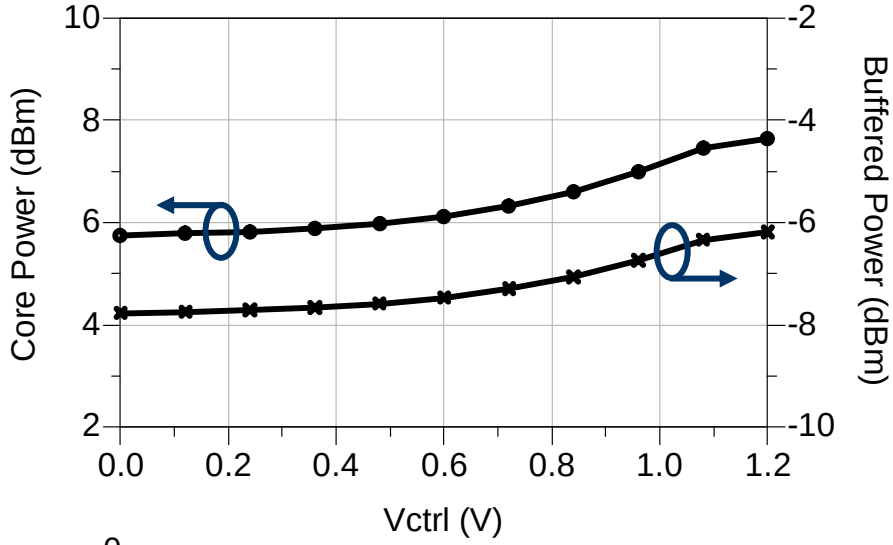
- Circuit Schematic & Design Parameters
  - **Based-on tuning requirement (3~4-GHz @30 GHz)**
  - **Design without band-switching for comparison**

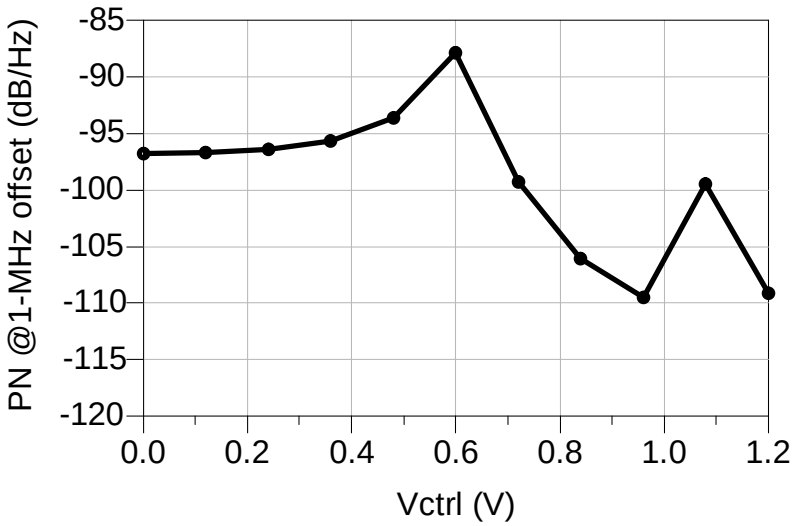


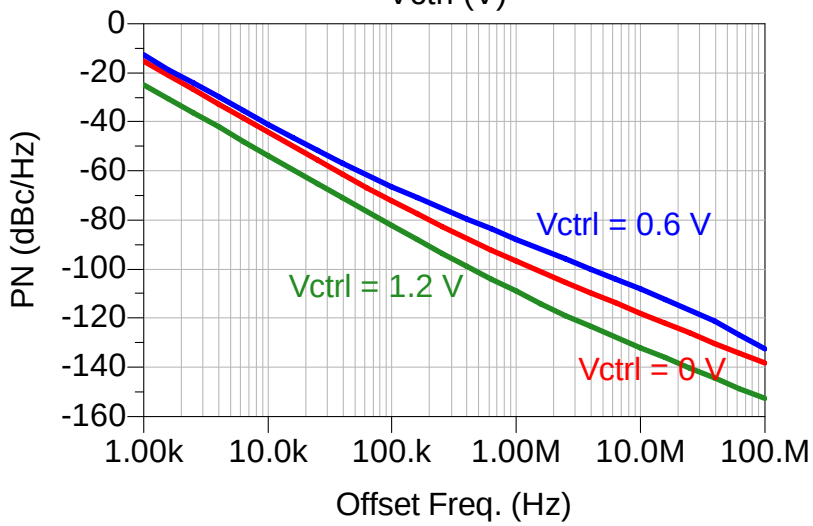
Device	Design Value	
M_1, M_2	1 × 12 μm / 0.06 μm	
I_{bias}	5.4 mA	
L_d	L	0.21 nH
	Q	32
C_{var}	62 ~ 100 fF	

VCO Performances for LO/2 (2/2)



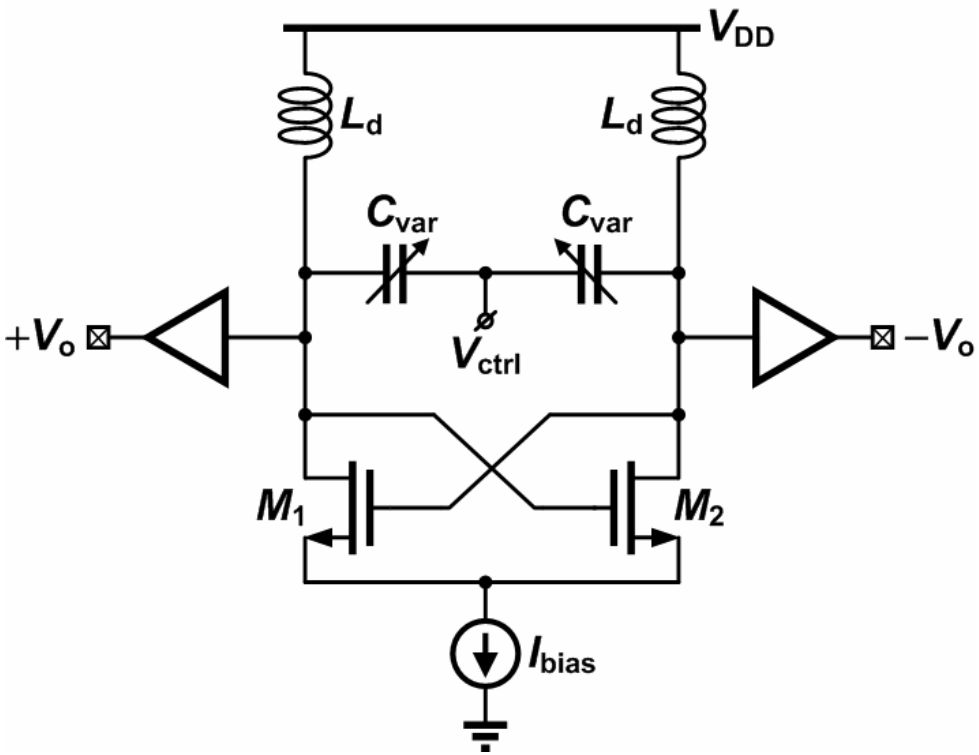






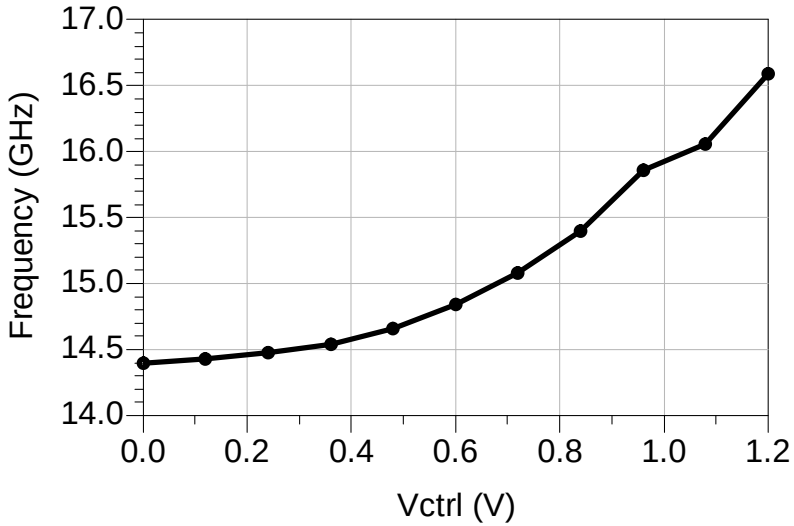
VCO Performances for LO/4 (1/2)

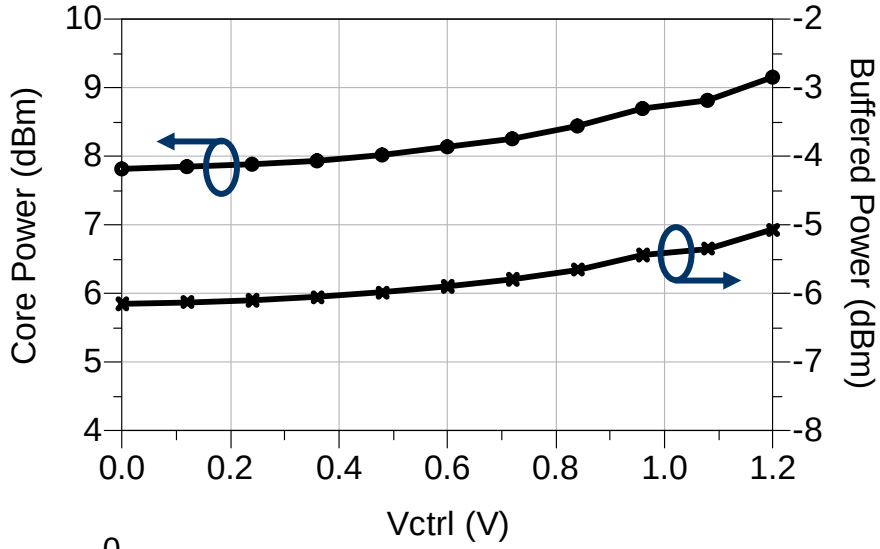
- Circuit Schematic & Design Parameters
  - **Based-on tuning requirement (1.5~2-GHz @15 GHz)**
  - **Design without band-switching for comparison**

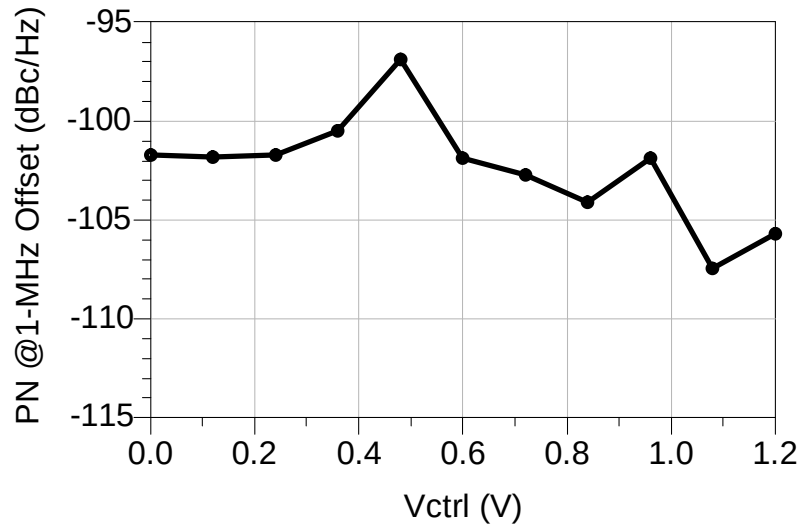


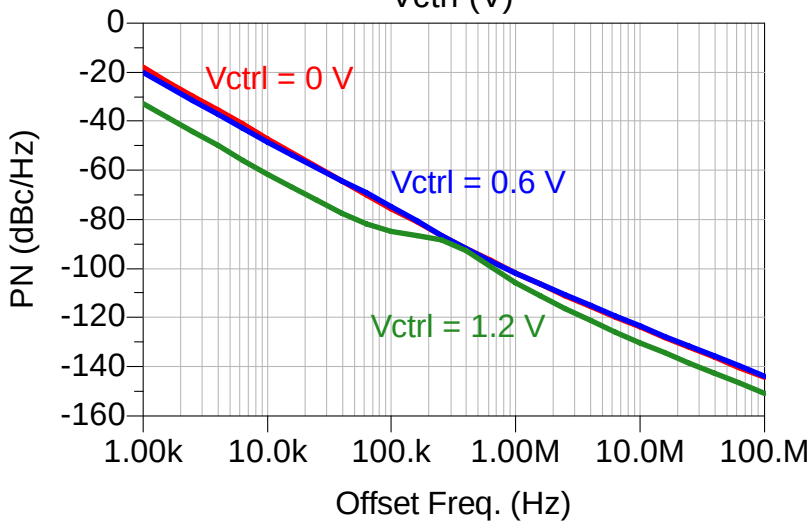
Device	Design Value	
M_1, M_2	$1 \times 9\ \mu m / 0.06\ \mu m$	
I_{bias}	2.9 mA	
L_d	L	0.88 nH
	Q	17.5
C_{var}	60 ~ 100 fF	

VCO Performances for LO/4 (2/2)









Comparison

- Performance Comparison among LO, LO/2, LO/4
  - **Phase-noise degradation: 6-dB/octave**
  - **Phase-noise performances can be further improved via band-switching design to cover the wide tuning range**

Mode	LO	LO/2	LO/4
Technology	65-nm 1P6M CMOS		
Frequency	60 GHz	30 GHz	15 GHz
Tuning Range	9 GHz	5 GHz	2 GHz
FTR	15 %	20 %	13.3 %
PN @1 MHz	-79 ~ -91 dBc/Hz	-88 ~ -109 dBc/Hz	-97 ~ -108 dBc/Hz
PN degradation	0 dB	6 dB	12 dB
Core Power	4.5 ~ 8.5 dBm	5.8 ~ 7.6 dBm	7.8 ~ 9.2 dBm
DC Power	9 mW	6.48 mW	3.48 mW

FOM Calculations

- FOM Comparison among LO, LO/2, LO/4 (VCO only)
  - **FOM = PN–20log(f_o/Δf)-20log(FTR/10)+10log(P_{DC}/1mW)-1.5log$_2$(f_o/LO)**
  - **PN degradations are included.**
  - **1.5 dB conversion loss is assumed for each multiplication by 2.**
  - **Based on simple *LC*-tank VCO, the one with LO/2 case yields the highest FOM.**
  - **The LO case with wide tuning ranges → PN degradations**
  - **Low inductor *Q* for LO/4 case → Colpitts structure or other available high-*Q* inductors**

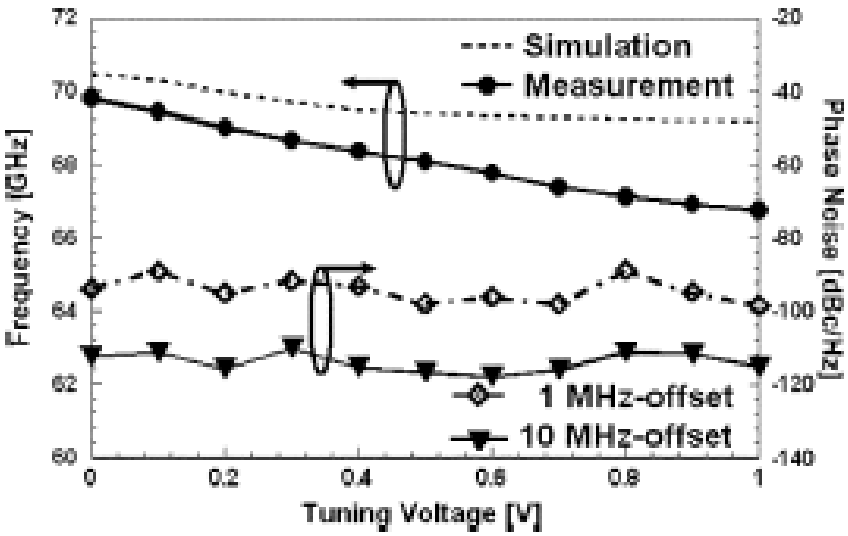
Mode	LO	LO/2	LO/4
FOM	-174.56 dBc/Hz	-184.42 dBc/Hz	-180.59 dBc/Hz

Recent Published VCO Phase Noise

IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, VOL. 18, NO. 7, JULY 2008 467

A 0.6 V, 4.32 mW, 68 GHz Low Phase-Noise VCO With Intrinsic-Tuned Technique in 0.13 μm CMOS

Hsien-Ku Chen, Hsien-Jui Chen, Da-Chiang Chang, Ying-Zong Juang, and Shey-Shi Lu, *Senior Member, IEEE*



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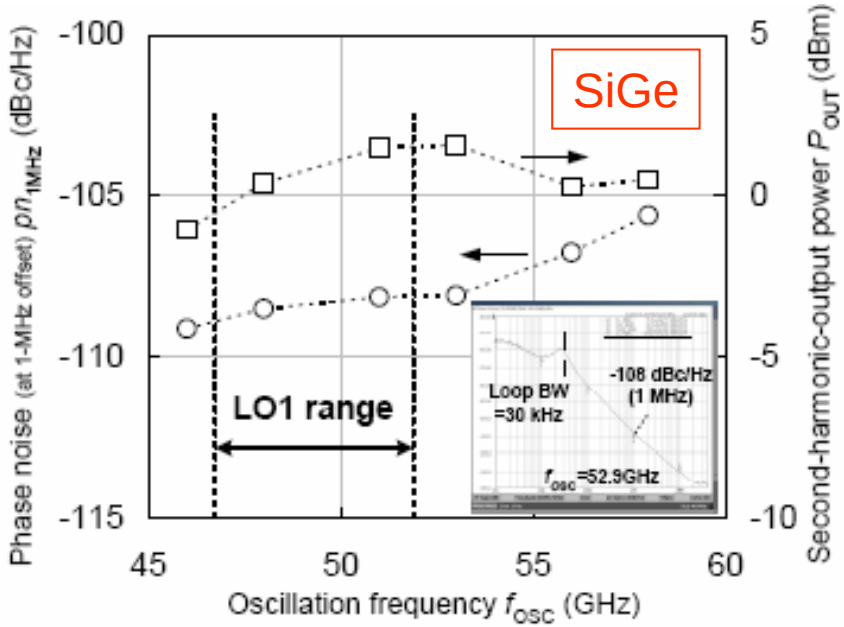
29.7 A 59GHz Push-Push VCO with 13.9GHz Tuning Range Using Loop-Ground Transmission Line for a Full-Band 60GHz Transceiver



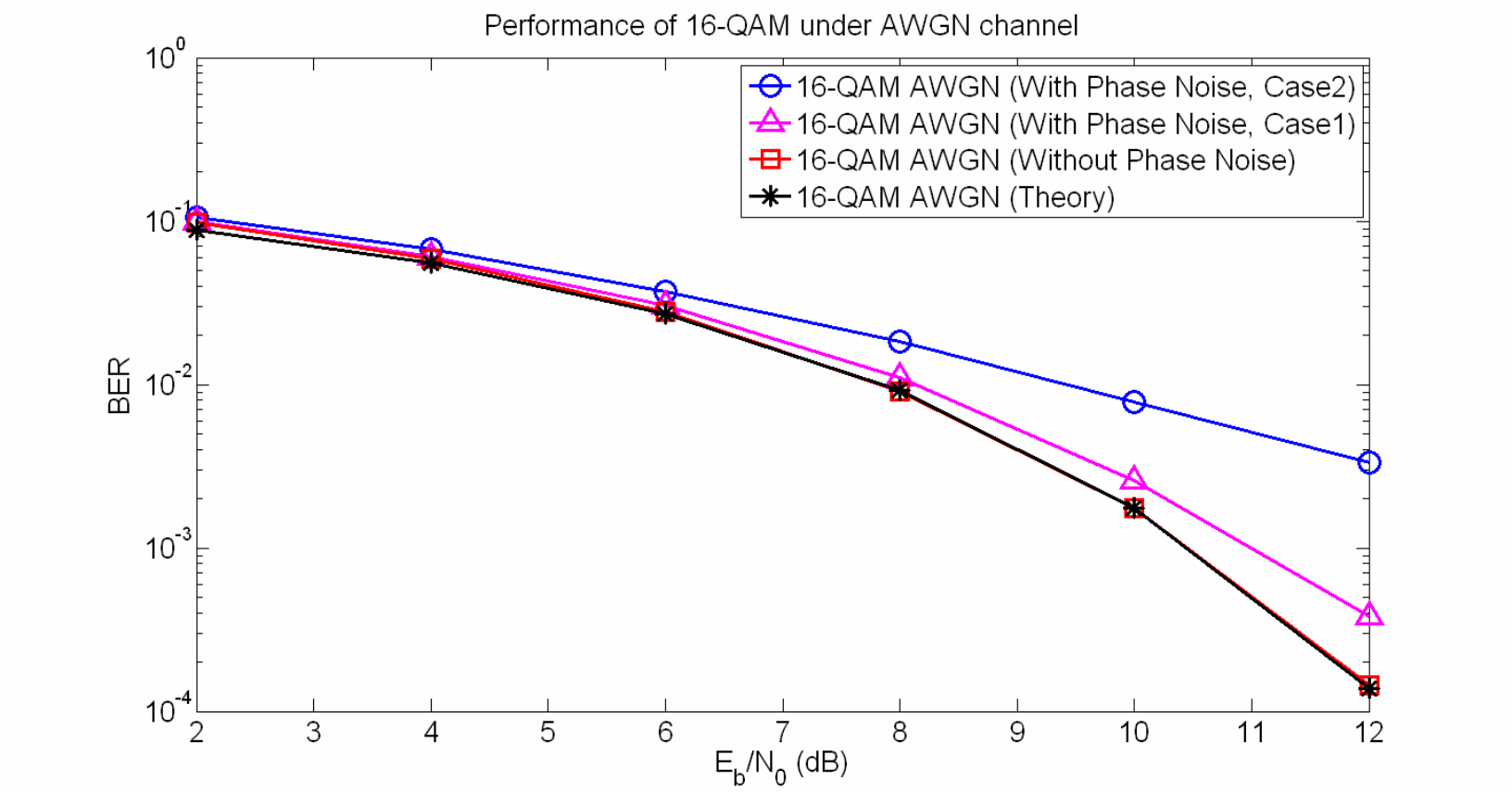
Phase Noise Model [1]

- **Phase noise may be reasonably modeled by a two pole – one zero model**

$$PSD(f) = PSD(0)\left[\frac{1+(f/f_z)^2}{1+(f/f_p)^2)}\right]$$

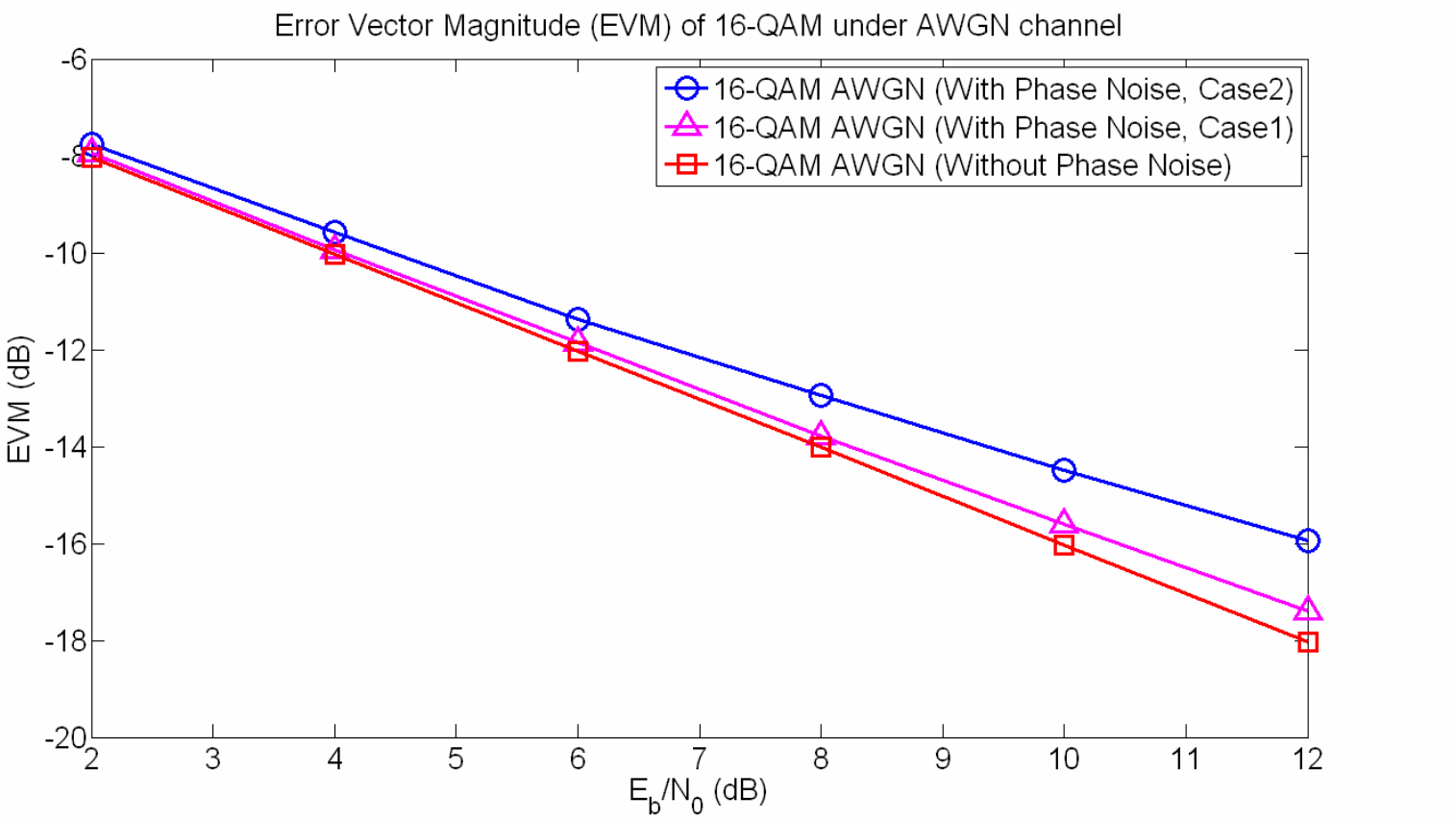
- **Case 1:**
  - PSD(0) = -92 dBc/Hz
  - Pole frequency f_p = 1 MHz
  - Zero frequency f_z = 100 MHz
  - PSD(infinity) = -130 dBc/Hz
- **Case 2:**
  - PSD(0) = -85 dBc/Hz
  - Pole frequency f_p = 1 MHz
  - Zero frequency f_z = 100 MHz
  - PSD(infinity) = -130 dBc/Hz

BER Peformance



SC 16-QAM, 3Gbps

EVM Performance



SC 16-QAM, 3Gbps

Conclusions

- 65nm CMOS PA linearizer can boost 60-GHz linear power 2-3dB under the same linearity requirement and DC power consumption.
- The modified Rapp PA model has a difficulty to model the corresponding IM3 plot with 3:1 asymptotic behavior.
- The divided-by-2 local oscillator frequency in 65nm CMOS 60-GHz RF system has better phase noise performance than the fundamental local oscillator frequency.

References

- [1] 11-09-1213-01-00ad-60ghz-impairments-modeling.ppt
- [2] Jeng-Han Tsai, Hong-Yeh Chang, Pei-Si Wu, Yi-Lin Lee, Tian-Wei Huang, and Huei Wang, " Design and Analysis of a 44-GHz MMIC Low-loss Built-in Linearizer for High-Linearity Medium Power Amplifiers," IEEE Trans. Microwave Theory Tech. Vol. 54, No. 6, pp. 2478-2496, June 2006
- [3] S. Cripps, “The Intercept Point Deception,” IEEE Microwave Magazine, pp. 44-50, Feb. 2007