United States Patent [19]

Baker et al.

[45] Feb. 18, 1975

[54]	ELECTRI	C POWER CONVERTER
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[22]	Filed:	Jan. 14, 1974
[21]	Appl. No.	: 432,939
[52] [51] [58]	Int. Cl	307/151, 321/5, 307/117
[56]	UNI	References Cited TED STATES PATENTS

7/1973

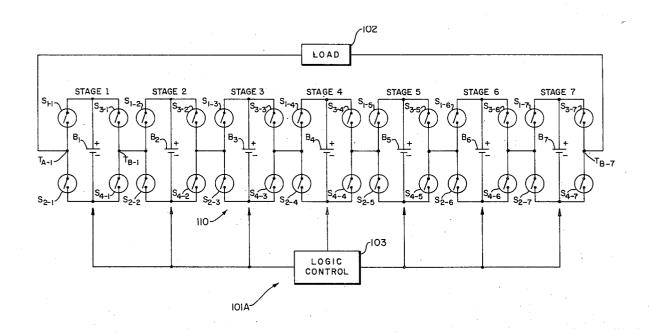
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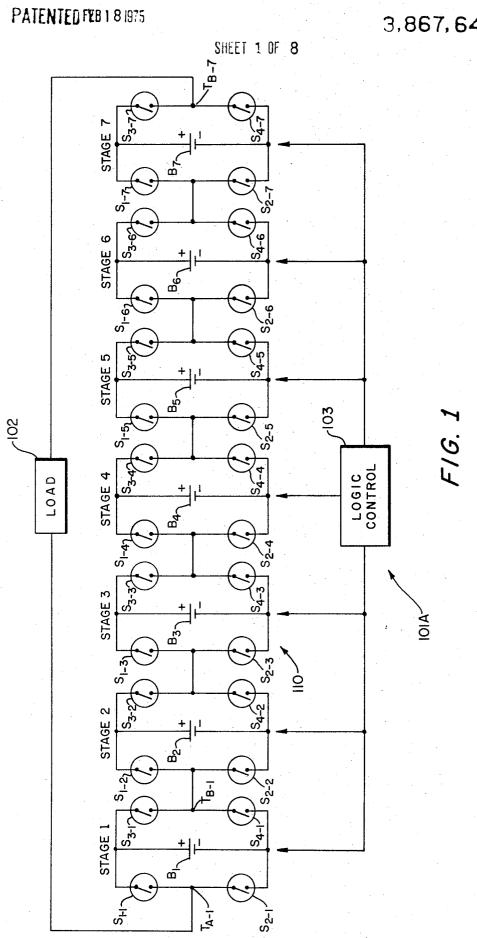
Primary Examiner—Robert K. Schaeffer Assistant Examiner—M. Ginsburg Attorney, Agent, or Firm—Arthur A. Smith, Jr.; Robert Shaw; Martin M. Santa

[57] ABSTRACT

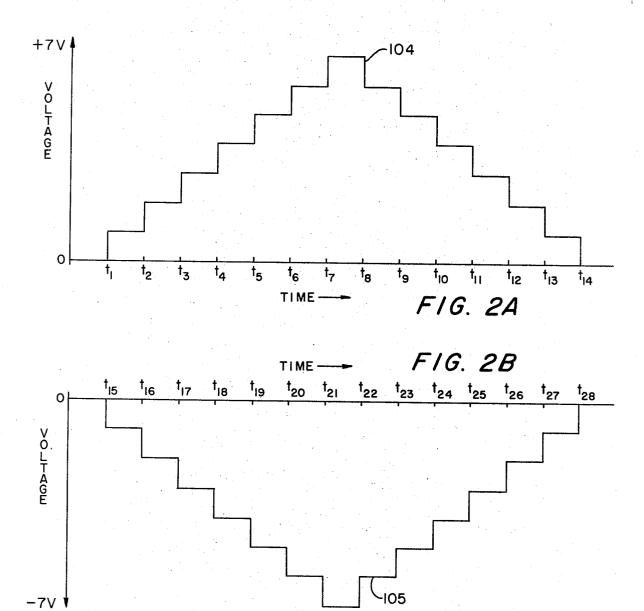
A programmed switching system for converting direct current into alternating current or some other variable current, or for converting alternating current of one frequency into alternating current of another frequency. The system employs a number of stages connected in cascade. Each stage includes an electrical energy source or an electrical energy storage unit and switch means adapted to bypass the energy source or storage unit, to interconnect the source or storage unit with other electrical energy source or storage units across a load in a programmed fashion, and to reverse the direction of current flow in the load to apply, for example, a quasi-sinusoidal voltage across the load.

27 Claims, 11 Drawing Figures





SHEET 2 OF 8



SHEET 3 OF 8

	t ₁	t ₂	t ₃	¹ C 4	t ₅	t ₆	t ₇	t ₈	t ₉	^t 10	t ₁₁	^t 12	^t 13	t ₁₄	t ₁₅
s_{1-1}	0*	0	0	0	0	0	0	0	0	0	0	0	0	0	С
S ₂₋₁	C*	C ,	C	C	C,	C	С	C	C	C .	C ,	C	C	С	0
s ₃₋₁	С	С	С	C	C	C	С	·C	C	C	С	C	С	0	0
s ₄₋₁	0	0	0	0	0	·O	0 .	0	0	0	0	0	0	С	С
S ₁₋₂	0	0	0	0	0	0	0	0	0	0	0	0	Ó	0	0
s ₂₋₂	С	С	С	С	C ·	С	С	C	C	С	С	C	c .	С	С
s ₃₋₂	0	С	С	С	С	С	С	С	C	С	С	С	0	0	0
S ₄₋₂	С	0	0	0	0	О.	0	0	0	0	0	0	С	С	С
												.*			
s ₁₋₃	0	0	0	0	0	0	0	О	0	0	0	0	0	0	0
s ₂₋₃	С	С	C	C	С	C	C	C	C	С	С	С	C .	С	С
s ₃₋₃	0	O -	С	С	C	С	С	C	С	C	С	0	О	0 .	0
s ₄₋₃	С	С	0	0	0	0	0	0	0.	0	0	С	c	Ċ	С
s ₁₋₄	0	0	0	0	0	0	0	0	0	0	0	0	0 .	0 -	0
S ₂₋₄	С	С	C -	С	C	С	C	С	C	С	С	C.	С	C	С
S ₃₋₄	0	0	0	C	С	C	C	С	С	С	0	0	0	0	0
S ₄₋₄	С	C	С	0	0	0	0	0	0	0	C	С	С	C ·	C
						1.									
s ₁₋₅	О	0 .	0	0	0	0	0	O	0	0	0	0	0	0	0
S ₂₋₅	С	Ċ	С	C	C	C	С	C ·	C	С	С	·C	С	С	С
S ₃₋₅	0	0	0	0	С	C ·	С	C	С	0	0	Ó	0	Ö	0
s ₄₋₅	C	С	С	С	0	0	0	0	0	C.	С	C .	С	С	С
s ₁₋₆	0	0	0	0	0	0	0	0	o .	0	0	0	0	0	0
S ₂₋₆	С	C	C	C	C	C	C	C	C	c	C	C	С	C	c
S ₃₋₆	0	0	0	0	0	C .	C	C	0	0	0	0	0	0	0
S ₄₋₆	C	C	C.	C ·	C	0 -	0	0	c ·	С	С	c	С	c	C
4-6	-	_	_		-	-	•		•			_	_		_
G.	0	0	0	0	0	0	. ^	^ -	•	^	•		•	^	•
S 1-7	C	c	C	c	c	C	C	0 ;	O C	0	0 C	0 C	0	0	0
S ₂₋₇				0	0					C			C	С	С
S ₃₋₇	0 C	0 C	. 0			0	C	0	0 .	0	0	0	0	0	0 .
s 4-7	C ·	C	С	C	C ,	C	0	С	С	C ·	C .	C	С	С	С

FIG.3A

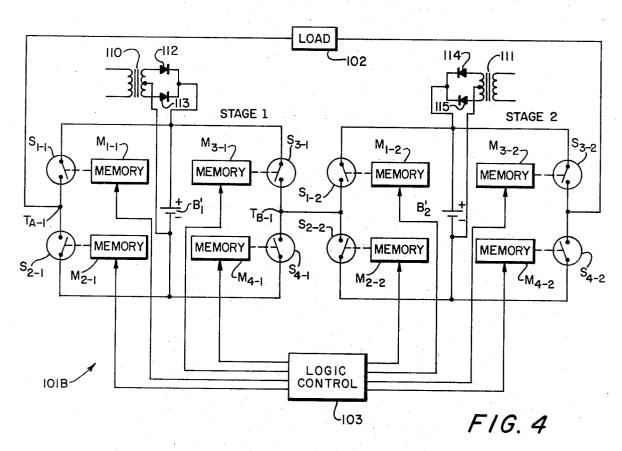
*O = open switch (non-conducting)
C = closed switch (conducting)

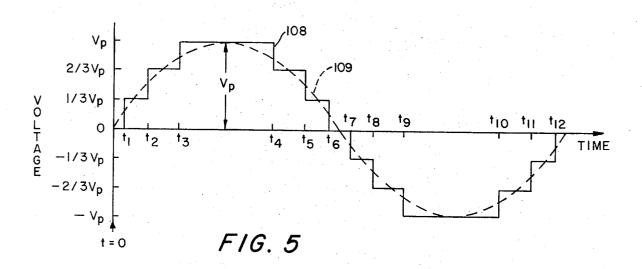
SHEET 4 OF 8

			_												
		^t 16	^t 17	^t 18	t ₁₉	t ₂₀	t ₂₁	^t 22	t ₂₃	t ₂₄	^t 25	^t 26	t ₂₇	t ₂₈	^t 29
s ₁₋₁	C*.	С	C .	С	С	C	C	С	C	С	C	C	С	0	0
s ₂₋₁	0*	0	0	0	0	0	0	0 .	0	0	0	0	0	С	С
s 3-1	0	0	0	0	0	0	0	0	0	0	0 .	0	0 -	0	С
s ₄₋₁	С	C	C .	С	C	С	С	C	C	C	C	С	С	c	o ·
									Ť						
s ₁₋₂	0	С	C	C	С	c	С	С	С	С	С	c ·	0	0	0
s ₂₋₂	C ,	0	0	0	0	0	0	0	0	0	0	0	C	C	C
S ₃₋₂	0	0 -	0	0	0	0	0	0	0	0	0	0	0	0	0
S ₄₋₂	C	C	С	C	c	С	c	С	C	С	С	C	C	c	C
												-	•		•
s ₁₋₃	0	0	С	C	С	С	C	C	C	С	С	0 .	0	0	0
S ₂₋₃	С	С	0	0	0	0	0	0	0	0	0	С	C	c	C
S ₃₋₃	0	0	0	0	Ó	0	0	0	0 -	. 0	0 .	0	0	0	0 -
S ₄₋₃	С	С	С	C	С	С	С	C.	С	С	С	С	С	С	С
6															
S ₁₋₄	0	0	0	C	С	C	C :	C ···	С	С	0	0	0 .	0	0
s ₂₋₄	С	С	C .	0	0	0	0	0	0	0	C .	Ċ	c ·	C	C
S ₃₋₄	Ο,	0	0	0	0	0	0 ' '	0	0	0	0	Ο,	0	0	0
S ₄₋₄	C	С	С	С	C	С	С	C	С	С	С	C	С	С	C
9										· ·					
s ₁₋₅	0	0	0	0	C	С	C	C	С	0	0	0	0	0	0
^S 2-5	С	C .	C	С	0	0	0	0	0	С	C	С	Ç	С	С
s ₃₋₅ s ₄₋₅	0	0	0	0	0	0	0	0,	0	0	0	0	0	0	0
-4- 5	C ·	С	С	C .	C	C	С	C	С	C	С	C	С	C	С
s ₁₋₆	_	_	_	_	2		•								
S ₂₋₆	0	0	0.	0	0	С	C	С	0	0	0	0	0	0	0
S ₃₋₆	C	C	C	C	C ·	0	0	0	С	C	C	С	С	C	C
S ₄₋₆	0	0	0	0	0	0	0	0	0	0	0	0	0		0
4-6	C ,	С	C	C	C ;	С	С	С	C	С	C .	С	С	C	С
s ₁₋₇	0	0	0	^	•		_		_	_	_				
s ₂₋₇	c	C	c	O C	0	0 ·	C	0	0	0	0	0	0		0
s ₃₋₇	0	0	0	0	0	0	0	С	C	C	C	C	C		С
s ₄₋₇	С	C .	c	C	C	C	0 C	0	0	0	0	0	0		0
- I					C	C		С	C	C,	С	С	Ċ	С	C .

^{*0 =} open switch (non-conducting) C = closed switch (conducting)

SHEET 5 OF 8



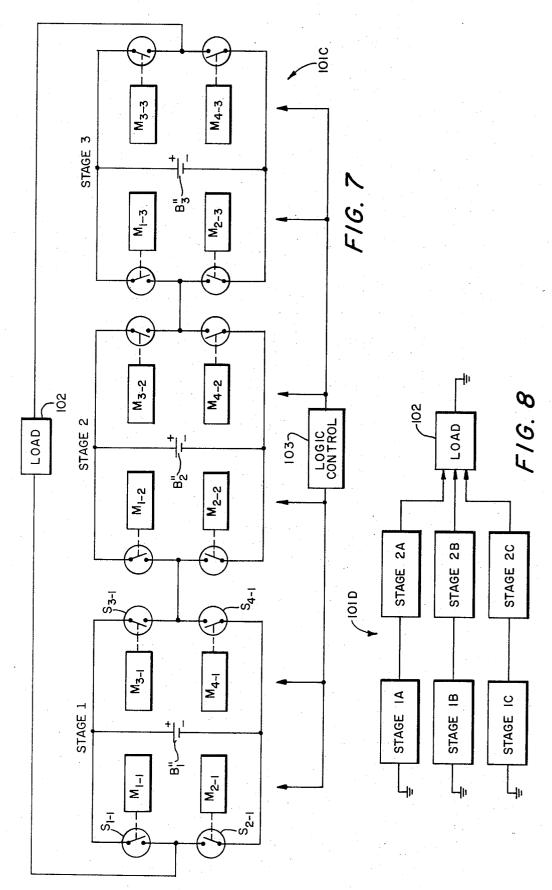


SHEET 6 OF 8

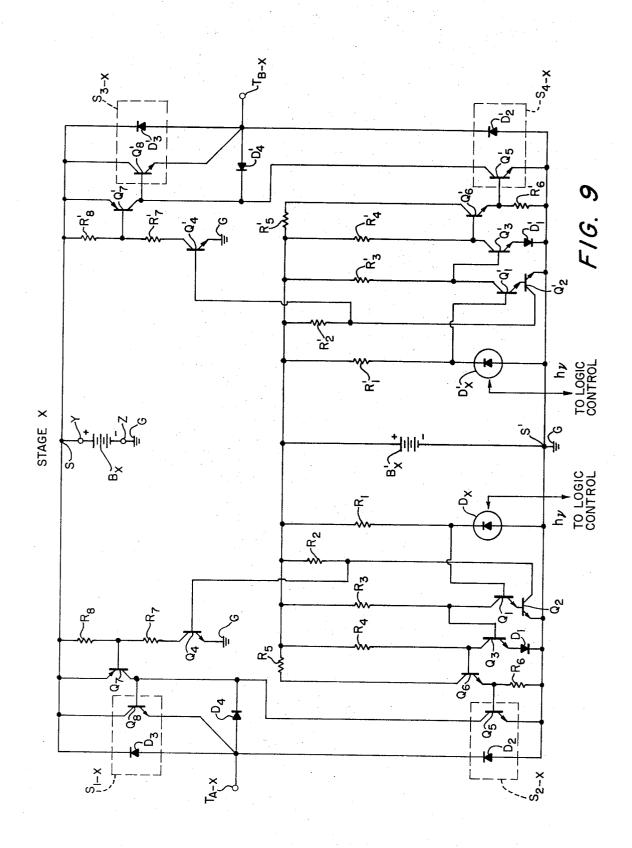
	t ₀	t_1	t ₂	t ₃	t,	ts	te	t.,	t,	t.	t	+.	+
s ₁₋₁	0	.0	0	0.	0	o	o	c′	C	c	$c^{t_{10}}$	c ¹¹	012
S ₂₋₁			C	C	C	С	С	0	0		0		
S ₃₋₁	0	0	C	C	С	0	0	C	0	0	0 %	С	O
s ₄₋₁											C		
s ₁₋₂	0	0	0	0	0	0	0	С	C	C	С	С	0
s ₂₋₂	C	, C	C	С	С	C	C	0	0	0	0	0	, C
S ₃₋₂	0	C	0	С	0	С	0	0	С	0	0	О	0
S ₄₋₂	, G	0	С	0	C	0	С	С	0	C	C	С	C

FIG. 6

SHEET 7 OF 8



SHEET 8 OF 8



ELECTRIC POWER CONVERTER

The invention described herein was made in the course of a grant from the Agency for International Development, an agency of the United States Govern- 5 ment.

The present invention relates to electric energy converters wherein a number of electric energy sources or electric energy storage elements are interconnected in a programmed fashion to cause an alternating current, to flow in a load.

tained in an electric power system that comprises a plurality of stages connected in cascade. Each stage includes in combination supply voltage means, first bilateral solid-state switch means connected between the supply voltage means and one terminal of the stage,

There has been a great deal of interest recently in fuel cells, solar cells, thermo-electric devices, and the like which convert chemical, radiation, and thermal energy to electrical energy. A number of problems have 15 arisen in connection with the use of such electrical energy generating devices. For example, individual generating units typically furnish electrical power of a few watts or less whereas many of the large uses contemplated require power in the kilowatt or megawatt 20 range. Also, most such devices provide a direct current output whereas most of the uses contemplated require alternating current and, particularly, quasi-sinusoidal voltage and current waveforms with small harmonic distortion. Also, most such devices have very poor reg- 25 ulation in that the voltage output differs markedly as a function of the current output. It is apparent, therefore, that any power system using such devices must be able to combine many of the individual electric generating devices efficiently, and must be able to convert direct 30 current into alternating current; and, further, the converter must yield a low impedance, quasi-sinusoidal output with small harmonic distortion.

Accordingly, it is an object of the present invention to provide a novel inverter that converts direct current ³⁵ into alternating current.

A further object is to provide a converter wherein a number of electric generators or storage elements, each providing a quasi-constant voltage, are combined to furnish a time varying output voltage.

A further object is to provide a converter wherein a number of quasi-constant voltage sources are combined to furnish an alternating voltage output.

A further object is to provide a converter wherein a number of quasi-constant voltage sources are combined to cause an alternating current to flow in a load.

A further object is to provide a very efficient inverter.

A further object is to provide an inverter furnishing a quasi-sinusoidal output whose harmonic content is controllable.

A further object is to provide an electrical energy converter having a low impedance output.

A further object is to provide an arbitrarily large voltage by combining a number of low voltage electric generators or storage elements.

A further object is to provide a converter having a large power output capability by combining a number of low power electric generators.

A further object is to provide a converter wherein alternating current of one frequency is converted to alternating current of another frequency.

A further object is to provide a voltage converter system that can be assembled from a multiplicity of similar modules.

A further object is to provide an electrical power converter wherein great flexibility is permitted in the 2

combination of individual devices and the manner in which these devices are combined to provide an output.

These, and further objects, are discussed hereinafter and are particularly delineated in the appended claims.

By way of summary, the foregoing objects are attained in an electric power system that comprises a plurality of stages connected in cascade. Each stage includes in combination supply voltage means, first bilatsupply voltage means and one terminal of the stage, and second bilateral solid-state switch means connected between the supply voltage means and another terminal of the stage. One terminal acts as input to the stage at one state of operation of the stage and the other terminal operates as output during said one state; the roles of the two terminals are reversed at another state of operation of the stage. The first switch means and the second switch means act in combination to connect one side or the other of the supply voltage means to either terminal as alternate conditions of stage operation or to bypass the supply voltage means.

The invention is hereinafter discussed with reference to the accompanying drawing in which:

FIG. 1 is a schematic circuit diagram partly in block diagram form, showing a seven-stage system which is adapted to combine the seven batteries shown, one per stage, in a way that will connect across the load shown an alternating voltage;

FIGS. 2A and 2B combined show an alternating single-phase voltage that may be provided across a load by the system of FIG. 1, FIG. 2A showing the positive-going voltage as a series of voltage steps, first increasing and then decreasing and FIG. 2B showing a negative-going voltage as a series of voltage steps, first decreasing and then increasing;

FIGS. 3A and 3B show a logical sequence in which switch elements in FIG. 1 may be actuated to furnish the waveforms shown in FIGS. 2A and 2B, respectively;

FIG. 4 is a schematic circuit diagram partly in block diagram form, showing a two-stage system somewhat similar in arrangement and purpose to that shown in FIG. 1;

FIG. 5 is a voltage waveform that can be provided by the system of FIG. 4;

FIG. 6 shows a logical sequence in which switch elements in FIG. 4 may be actuated to furnish the waveform shown in FIG. 5;

FIG. 7 is a schematic circuit diagram partly in block diagram form of a three-stage system somewhat similar in arrangement and purpose to that shown in FIG. 1;

FIG. 8 is a schematic circuit diagram in block diagram form showing a six-stage system which is adapted to combine six batteries, one per stage, in three parallel strings of two stages each in a way that will connect across a load an alternating voltage; and

FIG. 9 is a schematic circuit diagram of one practical realization of a single stage of the system of FIG. 1.

It is believed easiest to make this explanation with reference to a system that employs a number of batteries as individual electrical energy storage elements even though, as will be discussed later, other electrical energy storage means or electrical energy generating means are contemplated to be of great interest in a system employing the present concepts.

There follows now a description with reference to FIGS. 1, 2A, 2B and 3A, 3B of a direct current to alter-

nating current inverter using the concepts of the present invention.

In FIG. 1 a direct current to alternating current inverter system 101A includes a set of seven stages designated 110 that function under the control of a logic 5 control 103 to cause an alternating current flow in a load 102. It should be noted that the choice of seven stages for this illustration and description is somewhat arbitrary; as will be discussed later, a smaller of larger number of stages may be used in particular apparatus. 10

Continuing, then, the system 101A has seven stages, stage 1 through stage 7, each stage including a battery and first and second switch means, one such switch means at one terminal of the stage and the other such switch means at the other terminal of the stage. Each 15 stage has two terminals but, as will become apparent in the discussion to follow, neither can be called an input terminal nor an output terminal because the roles change (or can change) in the course of each cycle of the system operation. For present purposes, the first 20 switch means comprises the left hand switching units in each stage and the second switch means comprises the right hand switching units in each stage. Thus, the first switch means in each stage comprises switches S_{1-1} , $S_{2-1} \dots S_{1-7}$, S_{2-7} and the second switch means in each 25 stage comprises switches S_{3-1} , S_{4-1} ... S_{3-7} , S_{4-7} .

With reference to the first stage of the system 101A, the first switch means in stage 1 comprises a set of two semiconductor switches, the switches S_{1-1} and S_{2-1} , and the second switch means in stage 1 comprises a further set of two semiconductor switches S_{3-1} and S_{4-1} . One switch in each set is connected to carry electric current from the positive terminal of a battery B₁ to one or the other of the stage terminals designated T_{A-1} and T_{B-1} ; and the other switch in each set is connected to carry electric current from the negative terminal of the battery B_1 to one or the other of the two terminals T_{4-1} and T_{B-1} . Thus, the positive terminal of the battery B_1 may be connected to either of the stage terminals T_{A-1} or T_{B-1} and at the same time the negative terminal of the battery B₁ may be connected to the other stage terminal T_{B-1} or T_{A-1} , respectively. Also, the battery B_1 can be bypassed altogether by making switches S_{1-1} and S_{3-1} conduct simultaneously while switches S_{2-1} and S_{4-1} are nonconducting or by making switches S_{2-1} and S_{4-1} conduct simultaneously while switches S_{1-1} and S_{3-1} are nonconducting.

Note that the other stages of the system 101A are similar to stage 1 and have like numbered parts and that these other stages can be operated in a fashion similar to that described above in connection with stage 1.

As a specific example of the operation of the system 101A, it is supposed that the following switches only are conducting: S_{2-1} , S_{3-1} , S_{2-2} , S_{3-2} , S_{2-3} , S_{3-3} , S_{1-4} , S_{4-4} , S_{2-5} , S_{3-5} , S_{1-6} , S_{4-6} , S_{2-7} , S_{3-7} , then the potential difference between the terminal T_{A-1} and the terminal labeled T_{B-7} will be:

$$V_1 + V_2 + V_3 - V_4 + V_5 - V_6 + V_7$$

where V_1 , V_2 ... V_7 are the voltages provided by the batteries shown at B_1 , B_2 ... B_7 , respectively. Other combinations of conducting switches will yield other potentials between the terminal T_{A-1} and the terminal T_{B-7} up to, and including, the peak values:

$$V_1 + V_2 + V_3 + V_4 + V_5 + V_6 + V_7$$

$$-V_1-V_2-V_3-V_4-V_5-V_6-V_7$$

Operating as a direct current to alternating current inverter, the system 101A supplies a quasi-sinusoidal voltage wave that includes the two half cycles shown in FIGS. 2A and 2B, respectively, under the control of the logic control 103. The logical control to give the voltage waves numbered 104 and 105 can be provided in the switching sequences shown in FIGS. 3A and 3B.

The particular switching sequences illustrated in FIGS. 3A and 3B are chosen primarily to simplify an explanation of the operation of system 101A. A close study of the tabulations of FIGS. 3A and 3B will show that, in many cases, it will be better to use a different sequence to achieve the same end result. For example, the logical sequence shown is one in which the battery B₁ carries the heaviest burden of supplying the load 102 because it is in series with the load most of the time whereas the battery B₇ carries the lightest burden because it is in series with the load for only two units of time and is bypassed for the other 26 units of time in the 28 unit cycle shown in FIGS. 2A and 2B. The logical sequencing shown in FIGS. 3A and 3B would not ordinarly be followed, therefore, because it will usually be advantageous to divide the burden more evenly among the various energy sources. In addition, with the sequences shown in FIGS. 3A and 3B, switches S₂₋₇ and S_{4-7} are ON most of the time whereas switches S_{1-7} and S_{3-7} are OFF most of the time. Because the switches are, in fact, semiconductor switches which always dissipate some power in the form of waste heat, it will usually be advantageous to choose a switching sequence that makes the duty cycle for all switches approximately equal and so divides the burden of waste heat disposal more evenly among the various switches.

A study of the waveforms shown in FIGS. 2A and 2B and the switching sequences shown in FIGS. 3A and 3B will show that the switches S_{2-7} and S_{4-7} pass current in one direction during one part of the operating cycle and pass current in the other direction in the other part of the operating cycle. These switches, therefore, must have bilateral current carrying capability. But, further, to make it possible to divide the load evenly, both as to the energy storage or generating elements and as to the switching elements, it is necessary, in fact, that all the switches shown in FIG. 1 have bilateral current carrying capability. In this connection, the term bilateral is discussed in great detail in U.S. Pat. No. 3,748,492 granted to Baker, and there are shown in that patent various schemes for making semiconductor switches bilateral. Further schemes are shown in application for Letters Patent, Ser. No. 360,501, filed May 16, 1973 by Baker and in an application for Letters Patent, Ser. No. 426,269, filed Dec. 19, 1973 by Bannister and Baker.

In FIG. 1 and in the descriptive material heretofore, the electric power source in each stage of the system 101A has been shown and referred to, respectively, as a battery. This element, in fact, can be any one of the well known types of primary or secondary electric batteries. But, in many uses contemplated for the present invention, it will be advantageous to use some other form of electric energy source or storage element.

In particular, it is contemplated that in many systems the elements designated $B_1, B_2, \ldots B_7$ in FIG. 1 will be fuel cells, solar cells, or thermoelectric devices which convert chemical, radiation, or thermal energy into electrical energy, the system 101A being used to com-

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bine many of these devices in an arrangement furnishing high power alternating current to a load even though the individual electric sources provide only low power direct current.

Another adaptation is described now with reference 5 to FIG. 4 wherein a system 101B includes two stages. stage 1 and stage 2, that function under the control of logic control 103 to furnish an alternating current to load 102. If the system 101B is used to furnish substantial power to a load, for example, if it is used to drive 10 an electric motor to provide variable speed by virtue of varying the frequency of the alternating current supplied to the load, the batteries will discharge and therefore will require recharging. This can be accomplished by the arrangement shown in FIG. 4 wherein the bat- 15 tery B'₁ is charged by a transformer 110 through diodes 112 and 113 and the battery B'2 is charged by a transformer 111 through diodes 114 and 115. With this arrangement, electric power is derived from an alternating current supply connected to the primary of the 20 transformers 110 and 111; this can be any convenient source; for example, it can be the conventional 60 Hertz power distribution system. But the frequency of the alternating current supplied to the load is independently controlled by the logic control 103; so in this ar- 25 rangement the system 101B serves as a frequency converter to convert alternating current of one frequency into alternating current of another frequency.

In a configuration including a recharge capability like that shown in FIG. 4, it will be advantageous in some systems to replace the elements designated B'_1 and B'_2 by capacitors. For example, if the power to be supplied to the load is small, then small capacitors can be used as the electrical energy storage elements with a concomitant reduction in the physical size of the system 35 101B.

Individual control of the switches S_{1-1} , S_{1-2} , etc., can be effected through respective memories M_{1-1} , M_{1-2} , etc., under appropriate programming from the logic control 103. In this regard, the memories M_{1-1} , M_{1-2} , etc., can be, for example, the bistable circuits shown in said U.S. Pat. No. 3,748,492 but they can be monostable or tristable as well. The signals from logic circuit 103 can be light signals or can be signals fed through appropriate diodes as shown, for example, in said application Ser. No. 426,265, or some other appropriate coupling can be employed.

The logic control 103 in this as well as the other embodiments herein can be a register or a digital control. See FIG. 1, U.S. Pat. No. 3,705,391 which shows, among other things, a system for converting analog signals to digital signals and vice versa; the input to systems like 101A and 101B can be the binary type signal shown in that patent. It will be appreciated that the frequency of the waveform 108 later discussed, can be modified by changing the rate of sequencing and, in a digitally controlled system, this can be done by changing the frequency of a control clock.

A two stage system like that shown at 101B in FIG. 4 can be used to furnish to the load 102 a seven-step quasi-sinusoidal wave like that shown at 108 in FIG. 5. The sequencing to provide the wave 108 can be that given in the table of FIG. 6. In order to minimize harmonic distortion in the simulated sine wave numbered 109, the constant voltage provided by an electrical energy source or storage element B'_1 should be about 2Vp/3 and the voltage provided by element B'_2 should

be about Vp/3, where V_p is the peak voltage of the sine wave 109 in FIG. 5. It will be appreciated that an identical waveform can be furnished if the voltage of the element B'_1 is about Vp/3 and the voltage of the element B'_2 is about 2Vp/3 and if the switching sequence is modified appropriately.

Further, it has been found that the time difference between the instants at which the various switches are operated, times t_1 , t_2 ... t_{12} in FIG. 5, can be arranged in an optimal fashion, again to minimize total harmonic distortion or to minimize the distortion due to particular harmonics in the quasi-sinusoidal output waveform. In fact, in a system employing the techniques heretofore discussed, an output wave 108 has been provided with a total harmonic content of less than 10 percent and a third harmonic content of less than 2 percent.

The electric power system shown at 101C in FIG. 7 functions similarly to the systems 101A and 101B and, in particular, to the system 101B in that the electric energy source of storage elements designated $B_1^{\prime\prime}$, $B_2^{\prime\prime}$, and $B_3^{\prime\prime}$ in FIG. 7 have terminal voltages, respectively, of about Vp/2, Vp/3, and Vp/6. The three-stage system 101C can be used in circumstances where harmonic distortion requirements are more stringent than those for which the system 101B may be used.

It will be appreciated on the basis of the discussions heretofore that stages like those shown as parts of 101A, 101B, and 101C can be part of a system that includes multiple parallel stages like those shown as parts of system 101D in FIG. 8. And it will be appreciated that these multiple parallel stages can be sequenced in a manner which permits the energy source or storage elements to rest or be recharged between intervals of use. And it will be appreciated, further, that this permits the combination of many individual source or storage elements so that substantial power can be furnished to a load even though the individual source or storage element can provide only low power. It will be further appreciated that the stages in FIG. 8 can be sequenced, for example, in a three-phase manner to furnish a three-phase power supply to a load which might be, for example, a three-phase motor.

A detailed schematic of one practical implementation of a single stage is shown as FIG. 9. Stages like that shown in FIG. 9 have been used to implement systems like those shown at 101A, 101B, and 101C. Again, the electric energy source or storage means shown in FIG. 9 is a battery and, in fact, batteries have been used in the systems that have been build, tested, and analyzed because, among other things, the use of batteries facilitates the construction of the experimental apparatus. Single stage X in FIG. 9 shows in detail one stage of an actual system like the seven-stage system 101A employed to provide a voltage waveform like that shown in FIGS. 2A and 2B. In FIG. 9, the portion of the stage to the left of points S and S' is a mirror image of the portion to the right of points S and S'. The labeling used is consistent with that fact in that the elements of the right-hand part of stage X are merely the primed counterpart of the elements of the left-hand part. The bilateral semiconductor switches between terminals T_{A-X} and T_{B-X} and labeled S_{1-X} , S_{2-X} , S_{3-X} and S_{4-X} perform the functoin of the switches $S_{1-1},\,S_{2-1},\,S_{3-1}$ and $S_{4-1},\,$ respectively. The bilateral current carrying capacity of the switch S_{1-X} , for example, is the result of the combination of a transistor Q₈ and a diode D₃ whose operation is discussed in detail in said U.S. Pat. No.

3,748,492. The further circuit elements act to control the switches S_{1-X} , etc. In the stage X, transistors Q_1 , Q_2 , Q₃, and Q₄ and their primed counterparts are lowpower transistors, transistors Q₅, Q₆, Q₇ and Q₈ and their primed counterparts are high-power transistors, 5 diodes D2 and D3 and their primed counterports are high-power diodes and D₄ is a high-current diode. D₁ and D_1' are low-power diodes. The diodes labeled D_X and D_{X}' are light sensitive diodes which act to control or switch the stage X from one state to the other of its 10 various states in response to a logic control. In the actual system, the signal input to diodes D_X and $D_{X'}$ is light the source of which is light emitting diodes, under the control of an external control. There now follows a brief explanation of the electrical operation of stage 15

In FIG. 9 the supply voltage means of the stage is the battery shown at B_x ; a battery $B_{x'}$ acts to bias the various transistors in the stage. The battery B_X has terminals Y and Z, the terminal Z being connected to ground 20 G which in this situation is merely a common connection. In an operating system, a circuit can be made from the terminal T_{A-X} , the transistor Q_5 to the terminal Z thence from the terminal Y through Q8' to the terminal T_{B-X} . Reversal of the current in stage X can be from the 25 terminal T_{B-X} through the transistor Q_5' to the terminal Z, thence from the terminal Y through the transistor Q₈ to the terminal T_{A-X} . Bypassing the battery B_X can be accomplished by having both switches S_{1-X} and S_{3-X} ON with switches S_{2-X} and S_{4-X} OFF or vice versa. It is important to note that the switches S_{1-X} and S_{2-X} operate as a pair; that is, the switch S_{1-x} is ON when the switch S_{2-X} is OFF and vice versa; similarly, the switches S_{3-X} and S_{4-X} operate as a pair. But the switch-pair $S_{1-X} - S_{2-X}$ is independent of the switch-pair S_{3-x} and S_{4-x} , ON^{-35} OFF switching of the former being effected by the diode D_X and of the latter by the diode D_X' . As used herein, a switch is ON when the transistor therein is conducting and OFF when the transistor is nonconducting. It should be apparent, however, that current may in fact pass through the diode of the switches when the transistor is non-conducting, as above ex-

The control section for the switches S_{1-X} , S_{2-X} consists of the battery B_X (for power to run the control circuits) and the electronic components R_1 , D_X , R_2 , Q_1 , Q_2 , R_3 , D₁, R₄, Q₆, R₅, R₆ Q₄, R₇, R₈, Q₇ and D₄. The circuitry operates in the manner now explained. If it is supposed that the light sensitive diode D_x had no light shining on it, then it represents a high impedance (i.e., an open circuit) and current will flow through the resistor R₁ from the positive terminal of $B'_{x}(+12v)$ into the base of the NPN transistor Q₁ causing it to conduct. When the transistor Q₁ conducts, the transistor Q₂ also conducts and therefore the collector of the transistor Q₂ (bottom of resistor R₂) is at ground and therefore the transistor Q4 is rendered non-conducting. When the transistor Q₄ is OFF (non-conducting) then the transistors Q_7 and Q_8 are OFF and switch S_{1-X} is used to be OFF, that is, it represents a high impedance or openswitch condition. When the transistor Q₁ is ON, the transistor Q3 is OFF and cannot accept current at its collector terminal; the therefore the current flowing down through the resistor R₄ goes into the base terminal of the transistor Q6 which causes both the transistors Q₆ and Q₅ to be ON (conducting). When the transistor Q_5 conducts the switch S_{2-X} is ON.

When the light sensitive diode D_X has light shining on it, it acts as a low-impedance (in fact it is a small area solar cell) and its cathode is negative with respect to its anode. A negative potential at the base of the transistor Q_1 causes both the transistors Q_1 and Q_2 to be OFF. When the transistor Q2 is OFF, it will not accept current and therefore the current flowing through the resistor R₂ will flow into the base of the transistor Q₄ causing it to conduct. When the transistor Q₄ conducts the PNP transistor Q₇ conducts which causes the transistor Q_8 to conduct; the switch S_{1-x} is ON. When the transistor Q₁ is OFF, the current flowing through the resistor R₃ will cause the transistor Q₃ to conduct and the current flowing through the resistor R₄ is conducted to ground through the transistor Q_3 and the diode D_1 causing the transistor Q₆ and Q₅ to be non-conducting; therefore the switch S_{2-X} is OFF.

The presence or absence of light shining on the diode D_{X}' causes the control circuits of the right hand side, that is, the elements Q'_1 , Q'_2 etc., to control the switches S_{3-X} and S_{4-X} in the same manner as described above for the left side. The battery B'x is used in common with both the left and the right control sections. The diodes D₄ and D₄' are used as bias elements for the transistors Q₈ and Q₈'. For example, when the transistor Q₅ is conducting, its collector current must flow through the diode D₄ which causes the NPN transitor Q₈ to be back biased, that is, held in the OFF state.

Modifications of the invention herein discussed will occur to persons skilled in the art and all such modifications are deemed to be within the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. An electric power system comprising a plurality of stages connected in cascade, each stage including, in combination: supply voltage means; first bilateral solidstate switch means connected between the supply voltage means and one terminal of the stage; and second bilateral solid-state switch means connected between the supply voltage means and another terminal of the stage, one terminal acting as input to the stage at one state of operation of the stage and the other terminal operating as output during said one state, the roles of the two terminals being reversed at another state of operation of the stage, the first switch means and the second switch means acting in combination to connect one side or the other of the supply voltage means to either terminal as alternate conditions of stage operation or to bypass the supply voltage means.

2. An electric power system as claimed in claim 1 in which the supply voltage means is a d-c source of electric energy in each stage, the first switch means and the second switch means acting, in combination, to connect the positive side of the d-c source to one terminal or the other of the stage as alternate conditions of stage operations while simultaneously connecting the negative side of the d-c source respectively to said other terminal and said one terminal, or said switch means acting to bypass the d-c source.

3. An electric power system as claimed in claim 2 that further includes logic control means to establish logical sequencing of the first switch means and the second switch means to provide an a-c output from the system, said a-c output being effected by combining the d-c sources in a determined sequence.

4. An electric power system as claimed in claim 3 in which the first switch means in each stage comprises a

set of two semiconductor switches and the second switch means in each stage comprises a set of two semiconductor switches, one switch in each set acting to connect the positive side of the d-c source to one or the other of the two terminals of the stage and the other 5 switch of each set acting to connect the negative side of the d-c source to one or the other of the two terminals of the stage.

5. An electric system as claimed in claim 4 in which the set of two semiconductor switches forming the first 10 switch means act in pairs in that one switch of the set turns ON when the other switch of the set turns OFF and vice versa, and in which the set of two semiconductor switches forming the second switch means act in pairs in that one switch of the set turns ON when the 15 other switch of the set turns OFF and vice versa.

6. An electric system as claimed in claim 5 in which the logic control means switches each of the four switches in a stage individually, thereby connecting the positive side of the d-c source or the negative side of 20 the d-c source in each stage to either terminal or effecting a bypass of the d-c source in a stage to provide an a-c system output.

7. An electric system as claimed in claim 5 in which the a-c output is a close approximation of a sine wave. 25

8. An electric system as claimed in claim 7 in which the logic control means acts to vary the sequencing rate of the switch means thereby to vary the fundamental frequency of the a-c output.

9. An electric system as claimed in claim 7 that con- 30 sists of two stages connected in cascade, in which the d-c voltage of the source in one stage is about 2Vp/3, where V_p is the peak voltage of the sine wave, and in which the d-c voltage of the source in the other stage is about Vp/3.

10. An electric power system as claimed in claim 9 in which the logic control means effects switching between one state of system operation and another state of system operation at predetermined time intervals which are determined to provide an acceptable level of 40 harmonics in the output sine-wave approximation.

11. An electric power system as claimed in claim 10 in which the sequencing pattern for one cycle is

stage is about Vp/6, where V_p is the peak voltage of the

13. An electric power system as claimed in claim 7 that comprises more than three stages connected in

14. An electric power system stage having an input and an output, said stage including: supply voltage means; first bilateral solid-state switch means; and second bilateral solid-state switch means, the first switch means and the second switch means acting in combination to connect the supply voltage means between the input and the output and to effect a bypass of the supply voltage means as well as to effect reversal of the polarity of the supply voltage means connection within the stage, thereby to effect a change of roles of the input and the output of the system as alternate conditions of system operation.

15. An electric power system stage having an input and an output, said stage including: supply voltage means; first bilateral switch means; and second bilateral switch means, the first switch means and the second switch means acting in combination to connect the supply voltage means between the input and the output and to effect a bypass of the supply voltage means as well as to effect reversal of the polarity of the supply voltage means connection within the stage, thereby to effect a change of roles of the input and the output of the system as alternate conditions of system operation.

16. An electric system that comprises a plurality of stages connected in cascade, each stage of the plurality of stages having an input and an output and including supply voltage means, first bilateral switch means, and second bilateral switch means, the first bilateral switch means and the second bilateral switch means acting in combination such that the input and output are connected together and therefore at equal potential or that the supply voltage means is connected between the input and the output such that the output is positive with respect to the input or the output is negative with respect to the input as conditions of system operations.

17. An electric system as claimed in claim 16 in which the the supply voltage means in each stage com-

•	t_0	t ₁	t_2	t ₃	t4	t ₅	t ₆	t ₇	t ₈	t ₉	t ₁₀ .	t_{ij}	t ₁₂
S ₁₋₁	0	0	0	0	0			С	C	С	C	C	. 0
S ₂₋₁	C	C	C	C	C	C	C	0	0	О	0	0	С
S ₃₋₁	0	0	C	C	C	0	0	C	0	0	0	C	0
S ₄₋₁	C	C	О	0	0	C	C	0	C	.C	C	0	C
S ₁₋₂	О	0	O	0	0	0	О	C	C	C	C	С	.0
S ₂₋₂	С	С	C	C	C	С	C	0	0	0	0	О	, C
S_{3-2}	О	C	0	C	0	С	0	0	C	0	0	0 .	О
S ₄₋₂	Ċ	0	Ċ	0	Ċ	0	С	С	0	С	С	C	С

where t_0 , t_1 , etc., represent the time at which the stages are at a particular state, $S_{1\text{--}1}-S_{2\text{--}1}$ and $S_{3\text{--}1}-S_{4\text{--}1}$ are respectively the switches of the first switch means and the second switch means of the first stage and S_{1-2} — S_{2-2} and $S_{3-2} - S_{4-2}$ are respectively the switches of the first switch means and the second switch means of the second stage, C designates that the switch represented is closed and O designates that the switch represented is open.

12. An electric power system as claimed in claim 7 that consists of three stages connected in cascade, in which the d-c voltage of the source in one stage is about Vp/2, in another stage is about Vp/3 and in the other prises battery means and that further includes means for charging the battery means.

18. An electric system as claimed in claim 17 in which the means for charging comprises a source of alternating current connected to charge the battery

19. An electric system as claimed in claim 18 in which the source of alternating current is a source of variable frequency alternating current and that further includes control means that controls the first bilateral switch means and the second bilateral switch means to supply as system output an alternating current of another frequency.

- 20. An electric system as claimed in claim 19 in which the control means acts to vary the frequency of the output of the alternating current from the system.
- 21. An electric system as claimed in claim 20 in combination with like systems, interconnected to provide a variable-frequency output.
- 22. The combination as claimed in claim 21 in which the systems are connected in parallel to provide said variable-frequency output.
- 23. The combination as claimed in claim 21 in which the systems are connected in a polyphase connection to provide a variable-frequency polyphase output.
- 24. The combination as claimed in claim 23 that further includes a polyphase motor connected to receive the variable-frequency polyphase output and to operate at variable speed as a consequence of variation in the frequency.
 - 25. A system as claimed in claim 16 that further in-

cludes control means to control the first bilateral switch means and the second bilateral switch means to give a system output that is a-c.

26. A system as claimed in claim **25** in which the system output is variable in frequency.

27. Electrical apparatus that comprises a plurality of electrical systems connected in cascade, each said system comprising a plurality of stages connected in cascade, each of the plurality of stages having an input and an output and including supply voltage means, first switch means, and second switch means, means whereby the first switch means and the second switch means are operable to connect the supply voltage means between the input and the output of the stage such that the input and the output can be at equal potential or the output can be positive with respect to the input or the output can be negative with respect to the input.

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Disclaimer and Dedication

3,867,643.—Richard H. Baker, Bedford and Lawrence H. Bannister, Dedham,
Mass. ELECTRIC POWER CONVERTER. Patent dated Feb. 18,
1975. Disclaimer and Dedication filed July 29, 1980, by the assignee,
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Hereby disclaims and dedicates to the Public the entire term of said patent. [Official Gazette November 25, 1980.]

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