8.6 A 15mW 3.6GS/s CT-ΔΣ ADC with 36MHz Bandwidth and 83dB DR in 90nm CMOS

Pradeep Shettigar, Shanthi Pavan

Indian Institute of Technology, Madras, India

We propose design techniques that enable the realization of power-efficient single-bit CT-ΔΣ ADCs at multi-Gb/s speeds. An FIR DAC [1] is used to reduce sensitivity to clock jitter and relax loop filter linearity. A mostly analog path compensates the modulator for the delay introduced by the FIR DAC. The CTDSM samples at 3.6GS/s, has 83dB DR in 36MHz BW, and occupies 0.12mm^2 in 90nm CMOS. Dissipating 15mW from a 1.2V supply, it thereby achieves an FoM_{SNDR} of 72.8fJ/level, which is an improvement over the state of the art for converters with bandwidths greater than 20MHz.

The number of quantizer levels is a key design choice affecting the ADC architecture. Many prior-art DSMs [2] use a 4b quantizer to achieve wide bandwidths. Alternatively, a 1b quantizer can be used, but the sampling rate should be increased to achieve the desired DR. A 1b quantizer operating at 3.6GS/s consumes less power than a 4b quantizer working at half the speed. Further, DEM is not needed in a 1b design. However, the challenges must be overcome to obtain high resolution with such a design are: 1) increased clock-jitter sensitivity, 2) quantizer metastability, and 3) the loop-filter linearity. Our ADC employs several techniques that address these issues. Figure 8.6.1 shows the CTDSM architecture. The 4th-order loop filter is implemented using a combination of feedback and feedforward paths [2]. The fastest path around the quantizer is through I_1, while the linearity is determined by I_4. This allows independent optimization of these integrators. The cascade of I_3 and I_4 reduces the noise of the rest of the loop filter when referred to the ADC input. The 8-tap FIR feedback DAC [F(z)] attenuates the high-frequency content in the feedback sequence and reduces jitter sensitivity, resulting in jitter noise equivalent to that of a 4b modulator operating at half the sampling rate. The linearity required of the first integrator is also greatly relaxed, resulting in significant power savings. The FIR DAC is driven by the quantizer output delayed by one clock cycle. The additional latches used to obtain this delay reduce the effect of quantizer metastability. Thus, the use of an FIR DAC has the benefits of multibit operation without the need for DEM. DAC_0 is an RZ DAC driven by a half-cycle delayed version of the modulator output, while DACs 1 to 4 are of the NRZ variety. Excess loop delay is compensated by appropriate choice of gains for DAC_0 and DAC_1, similar to [2]. The zeroes of the NTF are spread optimally in the signal band through weak feedback (not shown in Fig. 8.6.1) around I_1-I_2 and I_3-I_4.

The FIR DAC introduces delay in the signal that is fed back to I_4, needing compensation to restore the NTF. Conventionally, this is done with another FIR DAC directly around the quantizer. This DAC's coefficients are large, resulting in low loop gain around the summing opamp. The amplifier has to be fast, wasting power. Gm-C techniques can be used [3], but these are sensitive to parasitics and difficult to reliably implement at our speeds. In our design, the loop is compensated using the filter shown in the grey box in Fig. 8.6.1. This is conceptually explained in Fig. 8.6.2, which shows the FIR DAC [F(z)] driving the first two integrators (I_4 and I_3). The DAC is excited by the quantizer output, comprising the input signal and shaped quantization noise. The DC gain of F(z) is 1 (so that STF(0)=1). The transfer function of the cascade F(z)-I_4-I_3 (signal path (1)) goes as 1/f^2 at low frequencies; more significantly, it attenuates high frequencies, as shown in Fig. 8.6.2(d). This deficit at high frequency is made up by using a compensation path consisting of I_{4r} and I_{3r} (replicas of I_4 and I_3), driven by an FIR DAC with transfer function [1 – F(z)] (Fig. 8.6.2(a), between p and q). The frequency response of the compensating path (2) is shown in grey in Fig. 8.6.2(d). Since the DC gain of F(z)=1, [1 – F(z)] has a zero at DC, and is combined with I_{4r}, resulting in an equivalent FIR filter E(z), driving I_{3r}, as shown in Fig. 8.6.2(b). The output of E(z) consists of the ADC input and shaped quantization noise. The input component (a low-frequency signal) would necessitate a large integrating capacitor in I_{3r}. To prevent this, V_{in} is subtracted from the DAC output, leaving I_{3r} to integrate only the shaped noise (Fig. 8.6.2(b)). The shape of the spectrum at the output of the compensating path follows the response NTF-E(z)-I_3 and is marked as (3) in Fig. 8.6.2(d). At low frequencies, the contribution of path (2) is much smaller than that of path (1), so I_{3r} is replaced by a filter $H_1(s)$ with low DC gain and a (1/s) roll-off at high frequencies (a bandpass shape) as shown in Fig. 8.6.2(c). This prevents offsets from saturating I_3. The output of $H_1(s)$, which has very little low-frequency content, feeds I_1 and I_2. The path to I_2 is further high-pass filtered (corner of ω_x in Fig. 8.6.1). This shapes the clock jitter noise injected into I_2 and prevents injection of DC offset of $H_1(s)$ into I_2.

A single-ended circuit diagram of the modulator is shown in Fig. 8.6.3. Active-RC integrators are used for better linearity and wide swing. The fast path around the quantizer is through I_1 (and to a lesser extent, I_2). The parasitic poles of these integrators need to be at very high frequencies, and would need power-hungry opamps. Power reduction is achieved in our design by implementing I_1 and I_2 using the assisted-opamp technique [4], where a replica of the integrator input current is injected into the output of the opamp. This reduces the opamp's burden and enhances speed for a given power. In our design, current-steering DACs (DAC_{a0} and DAC_{a2}) are used to assist integrators I_1 and I_2 respectively. Assistance is only used for the "fast input currents" of I_1 and I_2. The compensating filter $H_1(s)$, with a DC gain of about 2, is implemented as shown in the grey box. The response peaks at mid-frequency, and asymptotically rolls off as 1/s. The output of $H_1(s)$ feeds into I_2 through an RC-series branch that acts like a high pass filter. The FIR DACs are implemented using semi-digital techniques (Fig. 8.6.3).

The first opamp (Fig. 8.6.4(a)) consists of the cascade of g_{m1} and g_{m2}, which is feedforward-compensated with g_{mff}. Conventional opamps with feedforward compensation have limited output swing. Our design avoids this by AC-coupling g_{mff} to the input through c_b. The signal path is marked in black in the transistor level schematic. The 2nd-stage current is reused for the feedforward path.

The quantizer is shown in Fig. 8.6.4(b). The latch is similar to a CML design, but without current limiting in the regeneration phase. Apart from enhancing speed, the outputs can be interfaced with CMOS logic without level shifters. All DACs (other than DAC_{a0} and DAC_{a2}) are resistive; this results in less DAC noise and distortion when compared to current-steering designs. The entire loop filter consumes 5.5mA, while the digital section draws 5.1mA. The FIR DACs draw a total of 1.9mA.

The 90nm CMOS ADC occupies 0.12mm^2. The total power consumption is 15mW (with references) from a 1.2V supply. Fig. 8.6.5(a) shows the SN(D)R (for a 36MHz BW) as a function of input amplitude. The DR achieved is 83dB. Fig. 8.6.5(b) shows the PSD of the captured bit stream for a -4dBFS input. The THD is dominated by the second harmonic (believed to be from the test setup). The peak DR/SNR/SNDR are 83dB/76.4dB/70.9dB. The FoM_{DR}/FoM_{SNR}/FoM_{SNDR} are 17.9/38.8/72.8fJ/level. Fig. 8.6.6 compares the performance of this design with state-of-the-art ADCs [2,5,6,7].

Acknowledgments:
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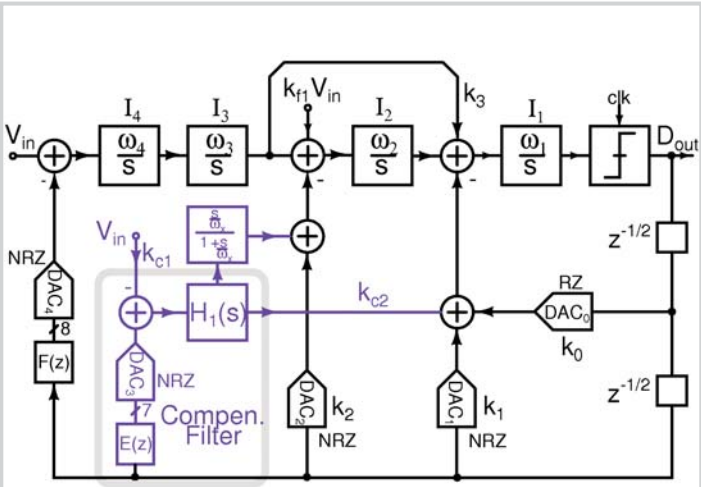

Figure 8.6.1: Modulator architecture, with the compensation path shown in blue.

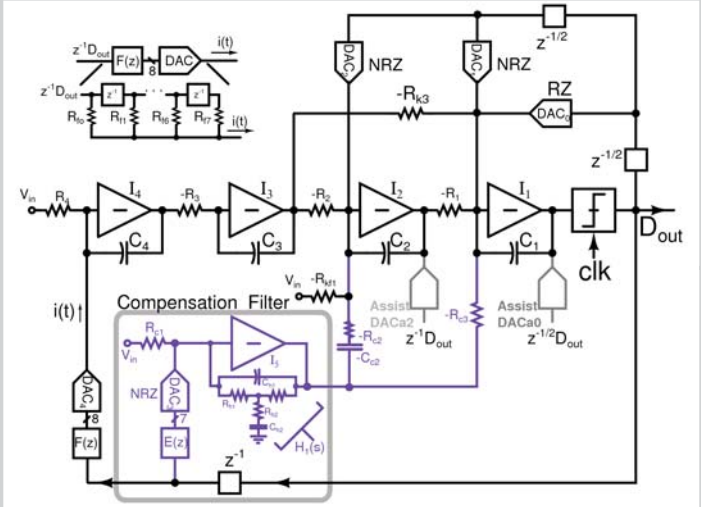

Figure 8.6.3: Single-ended schematic of the CTDSM. The compensation path is shown in blue. I_1 and I_2 are implemented using the assisted opamp technique, and the FIR DAC is a semi-digital structure (top left).

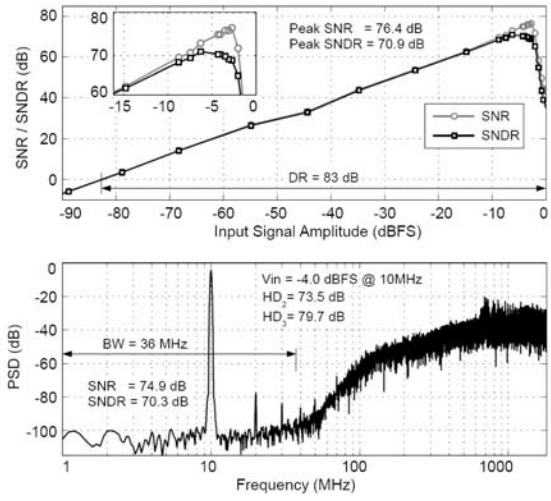

Figure 8.6.5: (a) Measured SNR and SNDR at 3.6GS/s in a 36MHz bandwidth. (b) PSD for a -4dBFS input tone at 10MHz.

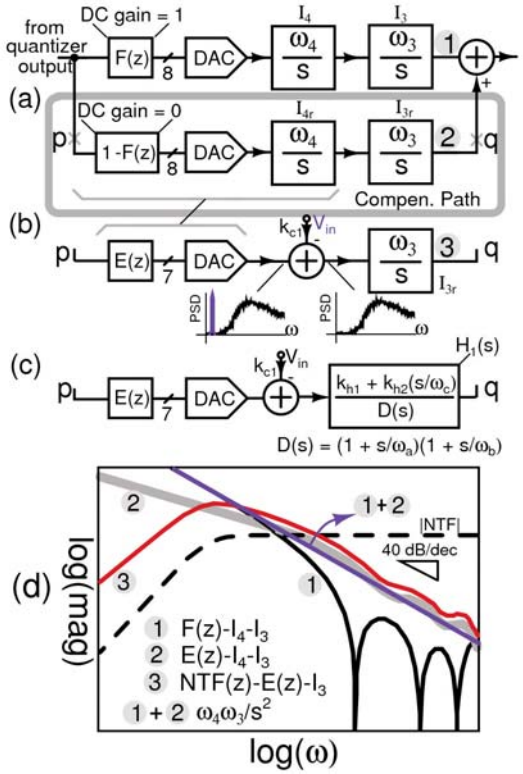

Figure 8.6.2: (a) Conceptual compensation technique (b) Combining [1-F(z)] with I_{4r} and subtracting V_{in} (c) Replacing I_{3r} with H_1 (s) (d) Responses of various paths.

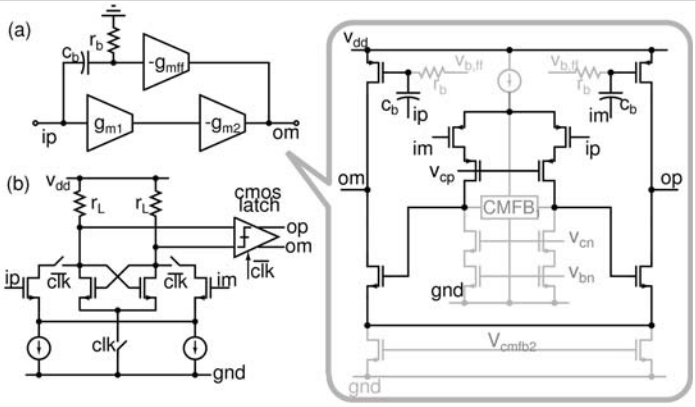

Figure 8.6.4: (a) Macromodel and schematic of the AC-coupled feedforward compensated 2-stage opamp and (b) schematic of the quantizer.

	This work	[2]	[5]	[6]	[7]
CMOS Feature Size	**90nm**	130nm	90nm	65nm	45nm
Active area	**0.12mm²**	1.2mm²	0.15mm²	0.15mm²	0.90mm²
Supply voltage	**1.2V**	1.2V	1.2V	1.2/1.3V	1.1V
Sampling rate	**3.6GHz**	640MHz	500MHz	250MHz	4GHz
P_d	**15mW**	20mW	8.5mW	10.5mW	256mW
BW	**36MHz**	20MHz	25MHz	20MHz	125MHz
DR	**83dB**	80dB	70dB	68dB	70dB
SNRmax	**76.4dB**	76dB	64dB	62dB	65.5dB
SNDRmax	**70.9dB**	74dB	63.5dB	60dB	65dB
$P_d/2BW\cdot2^{(DR-1.76)/6.02}$	**18fJ**	61fJ	66fJ	128fJ	396fJ
$P_d/2BW\cdot2^{(SNRmax-1.76)/6.02}$	**38.6fJ**	96fJ	131fJ	255fJ	665fJ
$P_d/2BW\cdot2^{(SNDRmax-1.76)/6.02}$	**72.8fJ**	122fJ	139fJ	321fJ	705fJ
$DR+10\log_{10}(BW/P_d)$	**176.8dB**	170dB	164.7dB	160.8dB	156.8dB

Figure 8.6.6: Performance summary and comparison with state-of-the-art CTDSMs with bandwidths in excess of 20MHz.

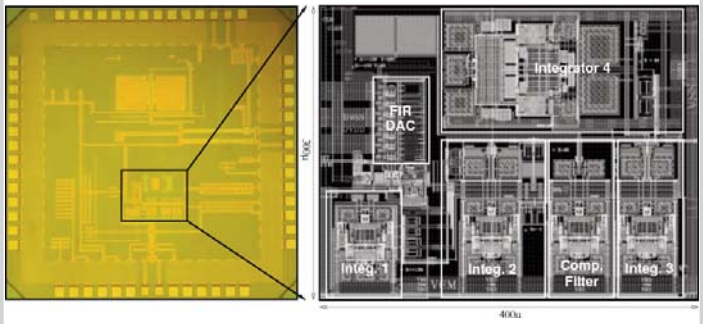

Figure 8.6.7: Die photograph (left) and zoomed in version of the CTDSM layout (right).

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