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## Comparative Analysis of High Voltage Gain DC-DC Converter Topologies for Photovoltaic Systems

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# Comparative Analysis of High Voltage Gain DC-DC Converter Topologies for Photovoltaic Systems

Asim Amir <sup>a</sup>, Aamir Amir <sup>a</sup>, Hang Seng Che <sup>a</sup>, Ahmad El Khateb <sup>b</sup>, N.A. Rahim <sup>a,c,\*</sup>

<sup>a</sup> *UM Power Energy Dedicated Advanced Centre (UMPEDAC), Level 4, Wisma R&D, University of Malaya, Jalan Pantai Baharu, 59990 Kuala Lumpur, Malaysia*

<sup>b</sup> *School of Electronics, Electrical Engineering and Computer Science, Queen's University Belfast, Belfast BT9 5AH, UK*

<sup>c</sup> *Renewable Energy Research Group, King Abdulaziz University, Jeddah 21589, Saudi Arabia*

\*Corresponding author: [nasrudin@um.edu.my](mailto:nasrudin@um.edu.my)

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## ABSTRACT

In this paper, a comparative analysis has been presented on various topologies of isolated and non-isolated DC-DC converters. Here, the major focus remains on transformer-less (TL) DC-DC converters, based on the conventional basic boost converter. In addition, to attain high voltage gain, a classification of non-isolated converters based on extendable and non-extendable design has been presented. For comparative and theoretical analysis, the parameters chosen are the number of components utilized by each converter topology, high voltage gain offered, voltage stresses on each component involved and the efficiency of the high gain topologies. For the converters under discussion, operation under ideal and non-ideal conditions has also been highlighted. Based on this study, authors present a guide for the reader to identify various high voltage gain topologies for photovoltaic (PV) systems.

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### 1. Introduction

In photovoltaic (PV) systems, high gain voltage is favorable. As in uninterruptible power supplies (UPS) and micro PV inverter [1-8]. For such applications, low input voltage from (PV) source need to be stepped-up. For example, in micro PV inverter, interfacing PV panel with a 230  $V_{RMS}$  grid requires the low PV voltage (typical around 30  $V_{DC}$ ) to be stepped up to around 375-400  $V_{DC}$  [5, 9-19]. For such applications, the voltage boosting required is too high to be achievable using conventional basic boost DC-DC converter topology, hence there remains a necessity for modified topologies offering high voltage gain. DC-DC converters commonly been divided into isolated and non-isolated topologies. For isolated DC-DC converters high voltage transformers (*HVT*) are utilized as presented in [4, 20-26]. Typically, for such converters high gain voltage boosting can be attained by *HVT* with high turn's ratio and by using voltage multipliers [16, 27-30]. Considering the case of full-bridge converters based on Phase-Shifted (PS) PWM, Zero-voltage (*ZVS*) and Zero-current (*ZCS*) switching can attained by utilizing leakage inductance of the *HVT*. The drawbacks of such a design include that the leakage inductance of *HVT* induces eddy current and excessive current on the primary of the transformer possibly decreasing the life span of PV panels. In addition, high current and voltage spikes on the secondary of the *HVT*, necessitates diodes with high breakdown voltage at output, as the voltage stress on the diodes remains greater than the output voltage [31-35]. Such shortcoming decrease the overall efficiency of the isolated converters.

In contrast, size and weight of the converter can be sizably reduced and higher efficiency offers a similar high voltage gain can be attained by employing TL DC-DC converters [35, 36]. Conventional boost and the buck-boost converters [34, 37-46]. For various applications Ćuk, SEPIC and Zeta topologies are preferred over conventional buck-boost converter for their better efficiency and continuous input current [47-52], albeit having higher component count [53]. Some attempts to create hybrid converters by crossover structures including the boost and the Ćuk topologies, but at expense of the extra components devoid of enhancing voltage gain characteristics [28, 50]. The boost converter usually has higher efficiency than the SEPIC [52]. In any case, boost converters output voltage is constantly higher than the input, which offers means of rigidity in power extraction [52, 54-59].

Despite many different topologies, the conventional boost converter still enjoys considerable amount of popularity due to the following advantages: few number of components which translate into system cost reduction; non-pulsating input current (if the converter operated in continuous-conduction mode (*CCM*)) and simple drive circuit.

By contrast, the major demerit of basic boost converter is the limited voltage gain. To further elaborate, in order to accomplish high voltage gain in basic boost converter, switch must conduct for 90-95 % of the total time, consequently; sharp current spikes for short time and high current stress harass the switch over the entire conduction time. On the other side, the diode conducts for 5-10 % of the total time, diode suffers severe reverse recovery problems. Additionally, the parasitic resistive elements inherited with the components in the circuit further constrain the voltage gain and the overall efficiency of the converter. The main losses of power occur due to; switching losses. Secondly, to construct a converter of this nature, a high voltage rating diode is required which causes severe diode reverse recovery problems. Thirdly, copper losses and core losses in the inductor [32, 35, 38, 46, 60-66].

In light of aforementioned issues, considerable amount of work has been dedicated to enhance voltage gain and the overall efficiency of boost converter, as seen in the available literature. So, to attain high voltage gain, various voltage multiplying techniques have been introduced, where they allow the modified boost converters to have extendable voltage gain. Many review articles have been published on DC-DC converter topologies [26, 67-80], however, none of the articles has presented a classification of the non-isolated DC-DC converters based on the design for extendable or non-extendable voltage gain. This paper brings most of the topologies together and categorizes them comparative and theoretical analysis. By classifying the topologies based on their theoretical achievable voltage gain, this paper attempts to give better insights to the performances and drawbacks of the converters, and hence help users or researchers in determining the most suitable converter topology based on their desired voltage gain range.

The objectives of the review are as follows:

1. Present a wide range of isolated and non-isolated DC-DC converters, which have been neglected by various review articles.
2. Classify the non-isolated DC-DC converters based on the design for extendable or non-extendable voltage gain.
3. A comparative review between different DC-DC converters, by theoretically analyzing each converter under discussion, particularly focusing the non-isolated design.
4. Guide for future work on DC-DC converter topologies, by displaying the pros and cons of the mentioned topologies.

The remaining of this paper is structured in the following manner: Section 2 Highlights the isolated DC-DC converter designs. Subsequently, Section 3 comparatively analyze the non-isolated DC-DC converters, focusing various modified topologies based on conventional boost converter with extendable and non-extendable voltage gain designs. Section 4 discusses the merits and demerits of all the converters under consideration. Finally, Section 5 provides the concluding remarks.

## **2. Isolated DC-DC Converter Topologies**

Fig. 1 presents only the chief isolated and non-isolated converters. In order to connect energy sources offering lower input voltages with a DC – Bus at higher voltage, galvanically isolated DC-DC converters are one of the most promising options available [4, 20-26]. For such converters, this isolation protects the source from high voltage variations at the load. Such converters offer effectual utilization of the energy source, wider load regulations and possess the capability to work with a broader variety of input voltages.

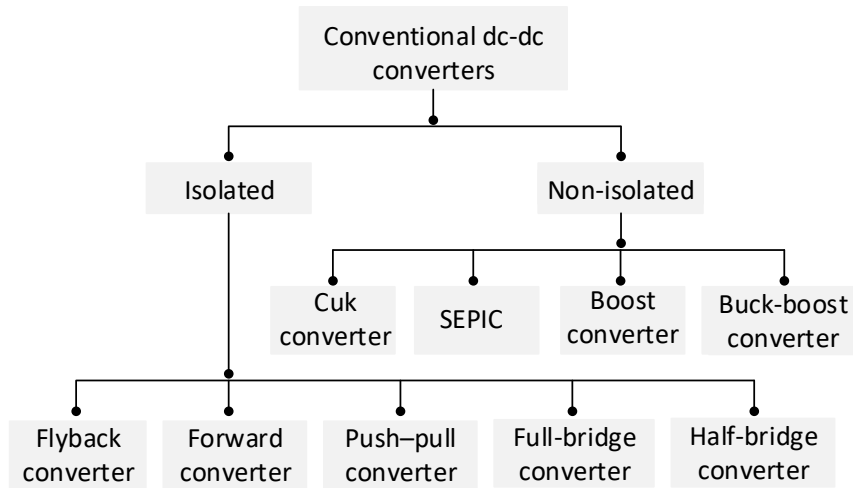
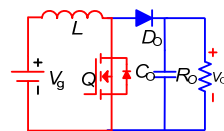


Fig. 1. Isolated and non-isolated DC–DC converts.

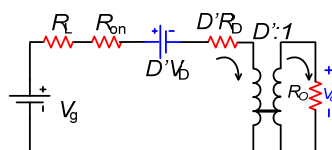
### 3. Non-isolated DC-DC Converter Topologies

#### 3.1. Analysis of parasitic elements in the non-isolated DC-DC converters

In this paper, the major focus remains of non-isolated DC-DC converter topologies. For the case of non-isolated converters by utilizing semiconductor and passive components ideally, there is a probability to attain high voltage gain against duty cycle. Section 3 presents various modified approaches for non-isolated high voltage gain DC-DC converters. Starting from the most fundamental topological design, Fig. 2(a) presents the schematic diagram of the basic boost converter and Fig. 2(b) the equivalent diagram of the conventional boost converter. In this paper, the power stage is highlighted in red color, rectifier stage in blue and the switched capacitor stages in black. Here, the parasitic elements have also been considered to evaluate the gain and efficiency of the converter.



(a)



(b)

**Fig. 2.** (a) Basic boost converter, (b) equivalent circuit of the boost converter.

Theoretically, by utilizing the volt-second balance, the analysis of the basic boost converter can be done. Here, current charge balance principles in continuous conduction mode (CCM) of operation have also been highlighted. As,

$$\langle V_L \rangle = D(V_g - IR_L - IR_{on}) + (1-D)(V_g - IR_L - V_D - IR_D - V_o) = 0 \quad (1)$$

$$\langle i_C \rangle = D(V / R_o) + (1-D)(I - V / R_o) = 0 \quad (2)$$

Where,

$D$  is the duty cycle,  $R_o$  remains the load resistance,  $V_g$  input voltage and  $V_o$  remains the output voltage. Non-ideal inherent resistive elements, have also been considered, corresponding to the diode resistance  $R_D$ , diode threshold voltage  $V_D$ , series inductor  $R_L$  and the switch  $R_{on}$

$$V_g - IR_L - IDR_{on} - (1-D) \cdot V_D - I(D-1)R_D - (1-D) \cdot V_o = 0 \quad (3)$$

$$I(1-D) - (V_o / R_o) = 0 \quad (4)$$

Furthermore, it remains simple enough to express voltage gain  $M = V_o / V_g$  to be given by [81]:

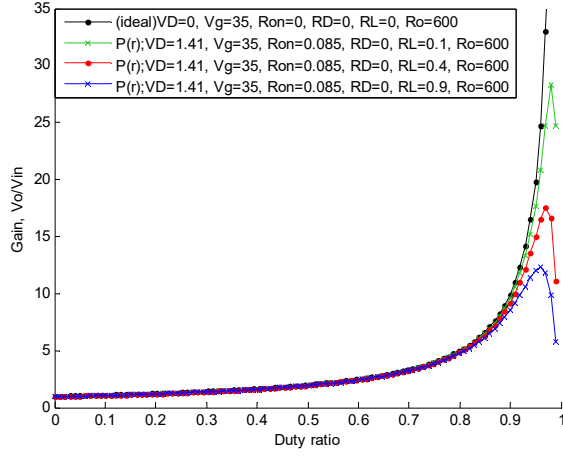
$$M = \frac{V_o}{V_g} = \frac{1}{(1-D)} \left( 1 - \frac{(1-D)V_D}{V_g} \right) \left( \frac{(1-D)^2 R_o}{(1-D)^2 R_o + R_L + DR_{on} + (1-D)R_D} \right) \quad (5)$$

Efficiency  $\eta$  of the conventional boost converter can be obtained as [81]:

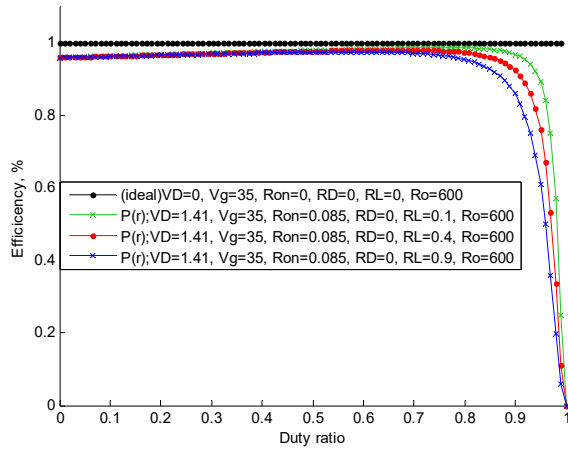
$$\eta = (1-D) \frac{V_o}{V_g} \quad (6)$$

$$\eta = \left( \frac{\left( 1 - \frac{(1-D)V_D}{V_g} \right)}{1 + \frac{R_L + DR_{on} + (1-D)R_D}{(1-D)^2 \cdot R_o}} \right) \quad (7)$$

Fig. 3(a) displays the plot for  $M$  versus  $D$  by equation (5) in MATLAB. Considering ideal conditions, if no parasitic resistive elements ( $R_L=0$ ,  $R_o=600$ ,  $R_{on}=0$ ,  $R_D=0$ ,  $V_D=0$ ) are considered, the basic boost converter offers a high voltage gain. By contrast, considering non-ideal situation where parasitic elements remain ( $R_o=600$ ,  $R_{on}=0.085 \Omega$ ,  $R_D=0$ ,  $V_D=1.41 V_{DC}$ ) where load resistance  $R_o$  is kept constant and the values of  $R_L$  are gradually increased;  $R_L=0.1$ ,  $R_L=0.4$ ,  $R_L=0.9$ . In addition, voltage gain for the conventional basic boost converter is observed to decrease as the values for  $R_L$  increase as shown in Fig. 3(a).



(a)

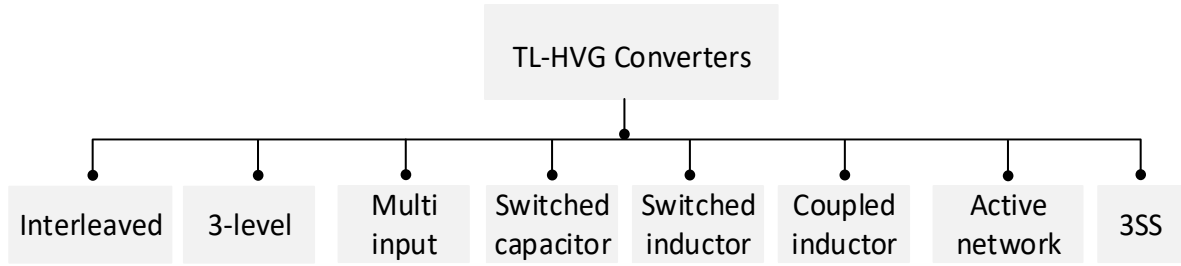


(b)

**Fig. 3.** (a) Plot for  $M$  versus  $D$ , and (b) plot for  $\eta$  versus  $D$  of the conventional boost converter.

Secondly, Fig. 3(b) displays the plot for  $\eta$  versus  $D$  curve by equation (7) in MATLAB. Considering ideal conditions, the basic boost converter can achieve an efficiency of 1 which is unrealistic. By contrast, considering non-ideal situation with parasitic elements remaining ( $R_o=600$ ,  $R_{on}=0.085 \Omega$ ,  $R_D=0$ ,  $V_D=1.41 V_{DC}$ ) where load resistance  $R_o$  is kept constant and the values of  $R_L$  are gradually increased;  $R_L=0.1$ ,  $R_L=0.4$ ,  $R_L=0.9$ . The efficiency of the basic boost converter theoretically decreases as the values for  $R_L$  increase as shown in Fig. 3(b).

To further improve efficiency and the voltage gain, different kinds of modified TL (Transformer-less) High Voltage Gain (HVG) boost converters have been proposed based on the conventional boost converter. These topologies can be categorized as 3-state switching-based boost converters, active network-based boost converters, 3-level-based boost converters, switched capacitor-based boost converters, coupled inductor-based boost converters, cascaded-based boost converters, switched inductor-based boost converters, multiport-based boost converters, and interleaved-based boost converters, as also given in Fig. 4. These converters are further categorized into Non-extendable voltage gain and Extendable voltage gain converters.

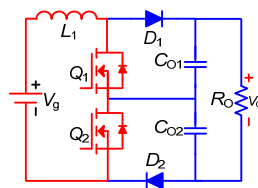


**Fig. 4.** Various Transformer-less High Voltage Gain Converter Topologies.

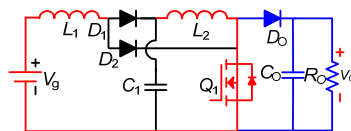
### 3.2. Non-isolated DC-DC Boost Converter with the Non-Extendable Voltage gain

#### 3.2.1. Conventional 3-level Boost Converters

The conventional 3-level boost converter has been presented in Fig. 5(a). It has double the voltage gain and one-half the voltage stress on power switches as compared with conventional basic boost converter. In addition, it remains appropriate for the various low input voltage and the high output voltage applications. Moreover, the low voltage rating power devices can be utilized and switching losses minimized. By contrast, power switch has a severe output diode reverse recovery problem when it operates under the hard switching condition [82-87]. Moreover, it has a balanced output voltage which is advantages to avoid damage to the power switches, adding to this, as the voltage is balanced between both the capacitors  $C_{O1}$  and  $C_{O2}$ , this feature permits the use of inverters that require capacitive divider, also this feature is advantageous in reducing common mode current circulation through the grid. On the contrary, switching frequency is low and the converter qualifies for low input voltage and high input current, therefore converter has a poor efficiency, hence it is recommended in low power applications. Single switch quadratic boost converter in Fig. 5(b) has a low efficiency, due to the effect of cascading. Quadratic 3-level boost converter in Fig. 5(c) has two stages. It has the advantages of both the topologies in Fig. 5(a) and (b). Voltage gain with high efficiency can be achieved. Therefore, it can be attractive for applications where high output power with high voltage ratio is required [88].

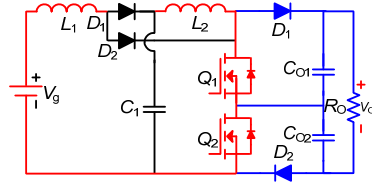


(a)



(b)



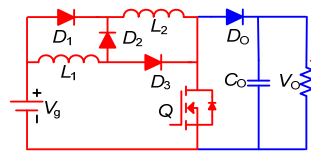


(c)

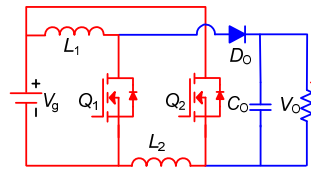
**Fig. 5** (a) Conventional 3-level boost converter [82-87], (b) Single switch quadratic boost converter [85, 86] (c) Quadratic 3-level boost converter [88]

### 3.2.2. Switched Inductor (SL) Based Boost Converter

Switched Inductor *SL*-cell based Boost Converters has been presented in Fig. 6 (a), which utilizes two inductors  $L_1$  and  $L_2$  of equivalent inductance and employs 3 diodes ( $D_1$ ,  $D_2$  and  $D_3$ ). Advantageously, both inductor windings can be accommodated into a single core [89]. Input current is small, which allows the use of smaller inductors. Moreover, the voltage gain is higher compared to the basic boost converter. On the contrary, the voltage stress on power switch and the output diode is almost equivalent to output voltage. Also, output diode encounters reverse recovery problems. Fig. 6 (b) utilizes the *SL*-cell based technique, in which two inductors with the same inductance are employed. Using this technique the high voltage gain can be attained without using unrealistic high duty cycle. Further, voltage stress on the output diode and power switch is less than the basic boost converter, as an advantage, both the switches with the rated low voltage and the low  $R_{DS(on)}$  could be utilized in order to reduce the cost of the system.



(a)



(b)

**Fig. 6.** (a) TL DC-DC high step-up converter [89], (b) High step up *SL*-based boost converter [90].

### 3.2.3. Ćuk Derived Boost Converter & Zeta Derived Boost Converters

The basic concept follows as, when the switch is *OFF*, the capacitors charged in parallel and as switch turns *ON*, the inductor is fully charged. Now, the capacitors form a series connection to offer high voltage at the output. Different boost or buck-boost topologies can be obtained by tapping out any two of the (*A-B-C-D*) points shown in Fig. 7. However, only two *SC*-cells can be utilized at a time. For example, if points *A* and *B* are tapped out topology Fig. 8 (b) can be realized. And, if points *C* and *D* are tapped out topology Fig. 8 (a) can be realized. Moreover, points *B* and *D* cannot be tapped out because the buck-boost capacitor  $C_{bb2}$  is directly

connected to the boost capacitor  $Cb2$ . As a result, the topologies in Fig. 8 are considered non-extendable. The voltage stress on the diodes and power switch is one-half the output voltage. Furthermore, turn-on current spike of the switch is controlled owing to the minor peak reverse-recovery currents. Here, the efficiency of the system can be improved if the capacitors with lower  $ESR$  are utilized.

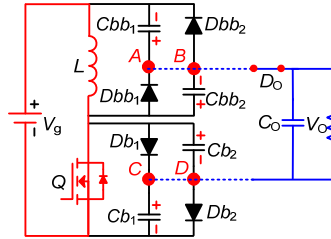


Fig. 7. Generic boost and buck-boost converters with SC-cell technique [8].

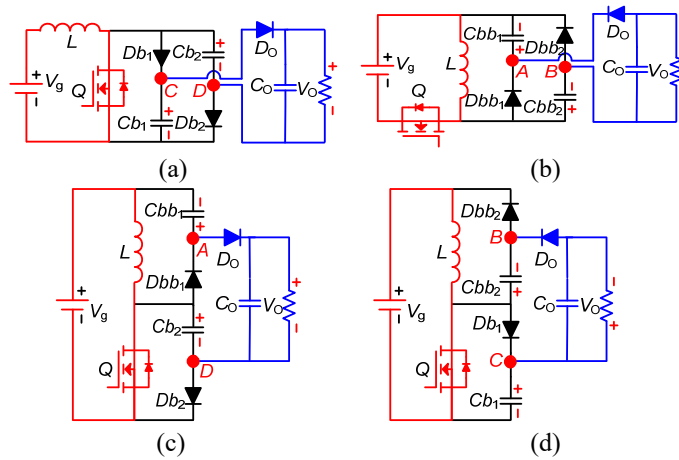


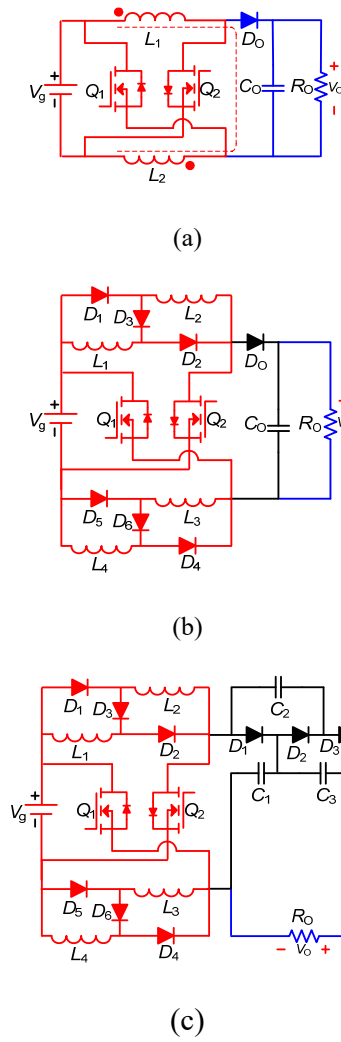
Fig. 8. (a) Cuk derived converter [91], (b) Zeta derived converter [91] (c) Type-1 boost-buck-boost-based [91]. (d) Type-2 boost-buck-boost-based [91].

### 3.2.4. Active Network Based Boost Converters

The active-network based DC-DC converter shown in Fig. 9(a) consists of two  $L_1$  and  $L_2$  inductors of equivalent inductance and  $Q_1$  and  $Q_2$  the two switches are provided with the same gate drive signal. In addition, inductors are charged up by input source connected in parallel as switch turns on. Now, inductors form a series connection as switch turns off and charges the output capacitor  $C_o$ , offering high voltage gain at the output.

Low current and voltage stresses are observed on the power switches. Moreover, inductor current is low which can be helpful to reduce the size of inductors integrated them into single magnetic core. Here, simplest topology of  $SL$  based  $ANC$  has been presented in Fig. 9(b).

The winding resistance of the inductors, conduction resistance, and diode forward voltage of power devices slightly affect the voltage gain of the topology presented in Fig. 9(c). The Converter shown in Fig. 9(c) can attain high gain with a small duty cycle. The basic boost converter cannot offer such merits. This offers high voltage gain with a low voltage and a low current stress for both the controlled and uncontrolled semiconductor devices. With the reduction in such stresses the number of  $SL$  and  $SC$  cells can be extended as per the required gain.



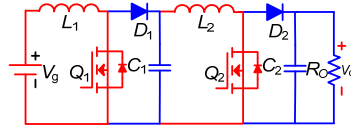
**Fig. 9.** (a) Active-network based DC-DC converter [90] (b) *SL* based *ANC* [92] (c) *SL* and *SC* based *ANC* [92].

### 3.3. Non-isolated DC-DC Boost Converter with Extendable Voltage gain

For certain applications, as micro inverter, high voltage gain is necessary in order to provide sufficient voltage. Such high gain is either beyond the capability of conventional boost converter and its modified topologies. In light of this, some researchers have proposed modified TL DC-DC converters which are extendable up to  $n$  stages, to have a higher voltage gain.

#### 3.3.1. Cascaded Boost Converter

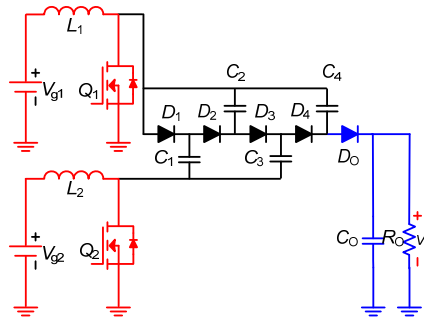
For high voltage gain, two (or more) boost DC-DC converters can be cascaded together as shown in Fig. 10. Nevertheless, this approach doubles the number of components as well as the losses when compared to conventional single stage boost converter. Higher DC-link voltage is supplied to the second stage and lower duty cycle can be used. This DC-link voltage is stepped up by the first stage by using higher duty cycle. Such a technique reduces current stress on power switch for second stage. Overall, the cascaded converters approach attains high voltage gain at the expense of higher component counts, higher cost, and degraded converter efficiency [93, 94].



**Fig. 10.** Conventional cascaded boost converter [93].

### 3.3.2. Multiport Based Boost Converter

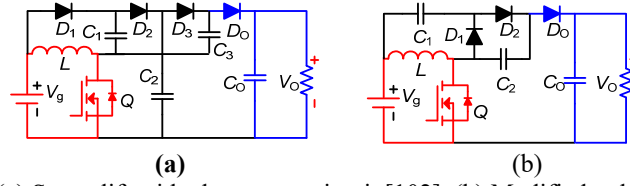
Two independent DC sources can be used to power multiport based boost converter as shown in Fig. 11 [95, 96]. High voltage gain is achieved by cascading several switched capacitor cells which confines the voltage stresses on the semiconductor and passive components. The list of advantages above, indicate that this converter can be in favorable and good solution if integrated with solar panels as DC micro-grid. Traditional approaches, suggest connecting several panels in series to achieve a voltage of 400-V on the DC bus, as the PV panel offers low output voltage. However, dependability of a system of this type always decline. Moreover, such a decline can be addressed by connecting individual PV panels to the converters with high voltage gain capability [97]. Further, multiport converter with an advancement of the interleaved boost input and Cockcroft Walton (CW) voltage multiplier also have been proposed in the literature in [98, 99]. It is observed that current fed converters are far better when compared with voltage fed equivalent as they offer minimal input current ripple [99]. However, for CW based converters with the increase of multiplying stages, output impedance increases rapidly [100]. This counts a major demerit of the topology. Here, output impedance is the determinant of efficiency of the converter.



**Fig. 11.** High voltage gain multiport converter [101]

### 3.3.3. Super Lift Voltage converter (SLVC) & Modified Voltage Lift Converter (MVLC)

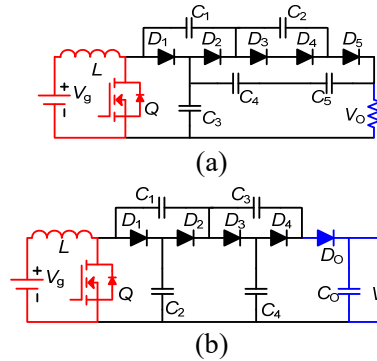
The SC cells can be extendable using super lift technique; output voltage can be increased stage-by-stage along the geometric progression. This technique is widely utilized so as to enhance high voltage gain and decline ripple voltage and current on the power components. However, input current in SVLC shown in Fig. 12(a), is not continuous. Additionally, output voltage will be affected by small load resistance by the capacitors; this may cause the currents in the circuit to increase. Secondly, the input current of the MVLC in Fig. 12(b) is continuous, which makes it most suitable for renewable energy application. The voltage gain can be further extend utilizing MVLC contrasted with conventional SVLC. In addition, when the converter operates in CCM, at such point voltage stresses are lower than conventional basic boost converter allowing the use of lower voltage rated diodes and switches to reduce the conduction loss.



**Fig. 12.** (a) Super-lift with elementary circuit [102], (b) Modified voltage lifter [103]

### 3.3.4. Cockcroft Walton Multiplier Based Boost Converter & Dickson Multiplier Based Boost Converter

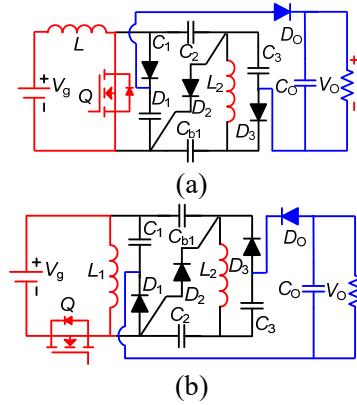
Two topologies based on switched capacitor integrating the basic boost converter and Cockcroft Walton voltage multiplier and Dickson voltage multiplier have been presented in Fig.13(a and b). These techniques can add up *SC* cells to *n* number. Moreover, are able to overcome the problem of pulsating input current, which is absorbed by the multiplier, these topologies provide high output voltage over smaller duty cycles.



**Fig. 13.** (a) Dickson Multiplier Based Boost Converter [104] (b) Cockcroft Walton Multiplier Based Boost Converter [104]

### 3.3.5. Boost derived MIESC SC-cell converter & buck–boost derived MIESC SC-cell converter

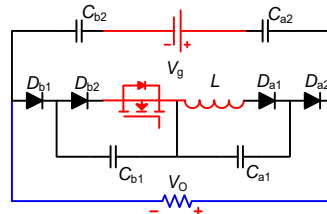
By connecting an additional *SC* cells in series to existing cells, the voltage gain can be further increased. For instance, converter shown in Fig. 8 (a), capacitor  $C_3$  is connected in series and one more inductor energy storage cell topology in Fig. 14 (a) can be seen. In contrast, converter shown in Fig. 8 (b), capacitor  $C_3$  is connected in series with an additional inductor energy storage cell; topology in Fig. 14 (b) can be seen. It can be suitable for applications demanding wide input voltage range i.e. 25–45  $V_{DC}$ . As the input voltage is low, the efficiency declines. As the input voltage decreases, the inductor current  $i_L$  surprisingly increases. On the contrary, circulating current through  $i_{D0}$  is independent of input voltage and considerably low. The circulating current is much smaller compared with the inductor current. Despite the fact that with minor increase in switch current, a considerable decrease in duty cycle can be attained by utilizing *SC* cells. Here, a small inductor is connected in series with output diode  $D_0$  in order to subside current peaks as the switch is turned on. In addition, the switch dominates power loss in these converters, and the second major is the entire power loss caused due to the three diodes. However, as the *ON* time of the switch is lesser, the switch off current and current ripple can be made smaller. This offers less switching and conduction losses, increasing the efficiency of the converter topology. However, cost for more components has to be paid to achieve a higher voltage gain. Here, only with a fewer component count high voltage gain can be attained.



**Fig. 14.** (a) boost derived MIESC SC-cell converter [91] (b) buck–boost derived MIESC SC-cell converter [91]

### 3.3.6. Hybrid Boosting Converter

Hybrid boosting converter (HBC) employing bipolar voltage multiplier (BVM) is shown in Fig. 15. Characteristics of interleaving are inherited to this converter which reduces the voltage on output filter capacitor and increases utilization rate of components as the voltage gain is higher at a lower duty cycle. Topologies in [105, 106] utilize interleaving technique for ripple decline and power increase; however, these topologies require more components. This converter realizes minor ripples while maintains high voltage gain with only single inductor and single switch. Higher gain was archived in topologies in [107-112], but they implement two inductors and two switches. The HBC topology has the advantages such as low cost design and potential to employee in high power applications. As a disadvantage to applications where common ground is required this topology has different ground for source and load. Moreover, due to this problem audible noise may be encountered, which may necessitate a fast control loop and an input filter.



**Fig. 15.** Hybrid Boosting Converter [113].

### 3.3.7. Boost Converters with Coupled Inductor

Coupled inductor-based boost converters can offer high voltage gain by aptly choosing the winding ratio, moreover extreme duty cycle operation of the switch(es) can be avoided [114, 115]. They offer reduced switch voltage stress, and low  $R_{DS(on)}$  switch and the reverse recovery for the diode at the output is improved [116-121] [84, 122]. It's simple structure is also favorable characteristic [123-125]. However, the leakage inductance might restrain the current induction in the secondary winding, causing considerable ac conduction loss, resulting in decline of the voltage gain dominantly when the converter operating under high frequency [114, 126]. As a solution, active clamp circuits are used in order to reprocess leakage energy to attain soft switching under the zero-voltage (ZVS) [127]. Moreover, additional clamp switch will increase topology complexity [128-130].

### 3.3.7.1. Coupled Inductors with Active Clamp Circuit-based Boost Converter

Both the switches  $S_2$  and  $S_1$  are assisted by the coupled inductors  $L_1$  and  $L_2$  and the leakage inductance of  $L_{k1}$  and  $L_{k2}$  in order to switch high with an operation under zero voltage condition (ZVS). Here, the switching low losses of switches are minimized by connecting parallel capacitors  $C_{r1}$  and  $C_{r2}$ . As a result, for high voltage applications, this converter topology remain a commendable choice. In addition, appropriate turns ratio  $n$  for coupled inductors must be selected with maximum duty ratio of  $D = D_{\max} < 0.5$ . Larger value of  $n$  has an effect of lower current stress on power switches thus, lower voltage stress mean switches with lower  $R_{DS(on)}$  and low voltage rated can be utilized. This converter not only has a less number of total components count also can achieve lower switching loss. Moreover, with a raise in for turns ratio  $n$ , as voltage stress for the diode at the output increases, thus high voltage operation may provoke high reverse-recovery losses. As a solution, an extra snubber circuit can be used to alleviate this issue [131].

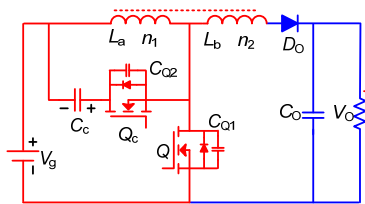


Fig. 16. Active clamp coupled-inductor-based converter [131].

### 3.3.7.2. Single Phase Coupled Inductor Boost-based Converter with Extended Voltage Doubler

The output diode voltage stress is reduced. In addition, a high voltage gain is attained by the extended SC. Moreover, during ON state of the switch, the coupled inductor, as a transformer, transfers energy. As the switch turns off, energy is conveyed in the form of a filter inductor as shown in Fig. 17, due to this feature complete utilization of the coupled inductor is possible. As a result, magnetic core of smaller size can be utilized.

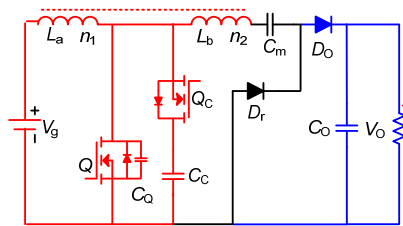
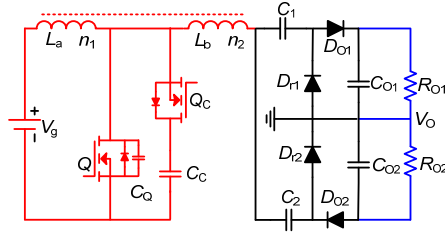


Fig. 17. Active clamp-coupled inductor-based converter [132]

### 3.3.7.3. Coupled Inductor Multiplier with Active Clamp Circuit Based Boost Converter

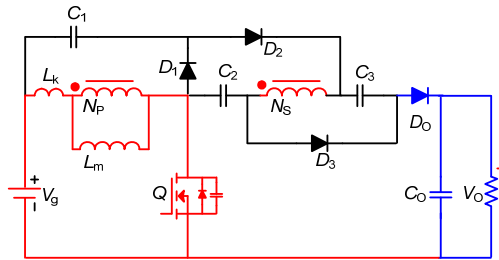
For this converter topology secondary winding of the coupled inductor is connected to a multiplier circuit. Moreover, 2 switched capacitors and 2 diodes are employed to construct the DC-DC converter as presented in Fig. 18. High voltage gain is achieved and voltage stress on the switches is reduced. Therefore, the efficiency is improved and the conduction losses are subsided. So the switches with lower  $R_{DS(on)}$  can be utilized. ZVS switching condition can be achieved, switching losses can be reduced; particularly in high-power and high-frequency applications.



**Fig. 18.** Single-phase high step-up converter with coupled inductor multiplier [109]

### 3.3.7.4. Coupled Inductor and Double Voltage Lift Capacitors-based Boost Converter.

An amalgamation of the SC and the coupled inductor into the voltage lift technique which is based on the conventional basic boost converter has presented by this converter topology in Fig. 19. Here, magnetizing inductor and leakage inductor in the coupled inductor are symbolized as  $L_m$  and  $L_k$ , respectively. Voltage across the switch  $Q$  can be clamped as the capacitors  $C_1$  and  $C_2$ , as the capacitors make use of the energy released by the coupled inductor as the leakage inductor energy. As,  $R_{DS(on)}$  resistance of switch  $Q$  and voltage stress is small, efficiency of the converter increases. Moreover, capacitor voltages across  $C_2$  and  $C_3$  are adjusted via the turns ratio of coupled inductor. High voltage gain can be achieved by reducing switch voltage stress across  $Q$ . Here, major operating technique is adopted from voltage-lift converts that when switch is under *ON* condition; induced voltage  $V_s$  on secondary side of the magnetic device, input voltage  $V_g$  and capacitor voltage  $V_{C1}$ , charge capacitor  $C_2$ . Simultaneously, capacitor  $C_3$  is charged by induced voltage. Thus, parallel charging of capacitors  $C_2$  and  $C_3$  takes place. As the switch turns off, energy from the magnetic device is released and induces voltage with an opposite-polarity to the secondary side. The induced voltage  $V_s$ , input voltage  $V_g$ , in order to charge the output capacitor  $C_0$  and  $R_0$ , capacitor voltages  $V_{C2}$  and  $V_{C3}$  are connected in series.

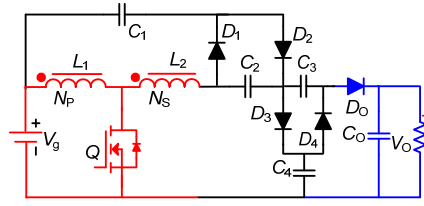


**Fig. 19.** Coupled inductor high voltage gain DC-DC converter [133].

### 3.3.7.5. Single Switch converter with high step-up gain

As presented in Fig. 20 a coupled inductor boost based DC-DC converter with only a single switch  $Q$  and SC network. This topology easily achieves high voltage gain through 2-boosting capacitors  $C_{b1}$  and  $C_{b2}$ , 2-switched capacitors  $C_{s1}$  and  $C_{s2}$ . Moreover, leakage energy is reprocessed at output, due to which the voltage spike on switch during *ON* time is alleviated. Here, voltage stress on power switches is  $V_o/3$  time less. On the plus side, power devices with lower; so that a voltage rated switch with a small  $R_{DS(on)}$  can be utilized.

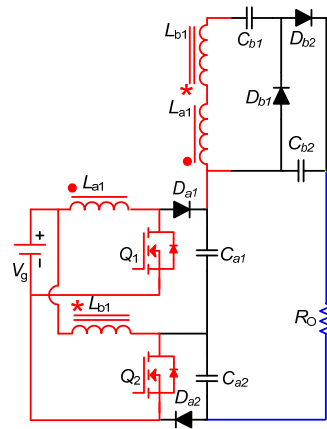




**Fig. 20.** Single-switch converter with high step-up gain [62]

### 3.3.7.6. Single Switch Converter with High Step-up Gain

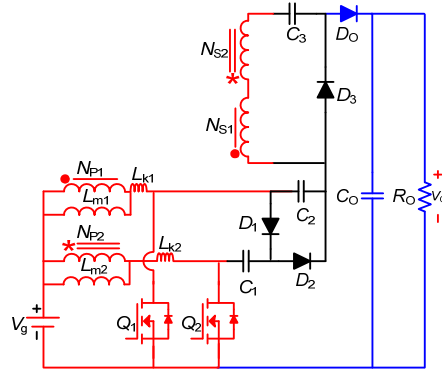
Fig. 21 presents a topology which is based on two parts. Part 1 is a modified version of an interleaved boost converter and part 2 is a capacitor diode based voltage doubler combined with coupled inductor. Main functions of part 2 are; Function.1: it is able to achieve 2 times voltage gain compared to conventional interleaved boost based converter. Function.2: interleaved series connected capacitors suppress the output voltage ripple. Function.3: voltage stress on the switches  $Q_1$  and  $Q_2$  becomes low. In order to attain a higher voltage gain, the secondary windings are connected in series with voltage multiplier [134].



**Fig. 21.** High gain input-parallel output-series DC-DC converter with dual coupled inductors [134]

### 3.3.8. 3-State Switching-based Boost Converter

Interleaved boost converter integrated with voltage multiplier and magnetic coupling technique carried with 3-state switching is utilized in topology shown in Fig.22. This topology is able to attain a high voltage gain without a high turns ratio and high duty cycles. Here, even with a lower turns ratio a voltage gain similar to the conventional boost converters with coupled inductor can be attained. Moreover, the input current is shared by the primary sides of the two coupled inductors, reducing the size of the magnetic core. Also, current ripples on the switches are less which decreases the conduction loss. Furthermore, diode capacitor provides lossless passive clamp performance, also gives a raise to the voltage gain. The switches  $Q_1$  and  $Q_2$  are exposed to minimum voltage spikes as the leakage energy of coupled inductors is reprocessed with recursive iterations in a loop. As the voltage stress are low, low voltage rating and low  $R_{DS(on)}$  switches can be chosen.



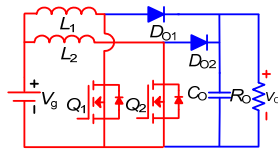
**Fig. 22.** Three-state switching boost converter mixed with magnetic coupling and voltage multiplier [135].

### 3.3.9. Interleaved Boost-based Converters

By increasing power level, reducing passive component size and by improving transient response the current ripple can be reduced. This topology is utilized in high power density and many large current applications.

#### 3.3.9.1. Conventional Interleaved Boost Converter

This topology has been presented in Fig. 23 [136]. It offers a gain similar to that of the basic boost converter, at higher duty cycles, which is not favor of applications that demand high voltage gain. The on time of the switch increases and offers a larger current ripple increasing the conduction losses. Here, off time decreases and severe reverse-recovery issues are confronted by the output diode.



**Fig. 23.** Conventional interleaved boost converter [136]

#### 3.3.9.2. Interleaved Boost Converter with Voltage Multiplier

Conventional interleaved boost is integrated with coupled inductors and SC-cells, as presented in Fig. 24. The coupled inductors the SC offer high voltage gain. Furthermore, conduction and diode reverse recovery losses are subsided by energy stored in the magnetizing inductor when one switches turns off, will transfer via three respective paths. Consequently, the current decreases during distribution, moreover, current through a few diodes even decrease to zero before they turn off. High-power applications can utilize this converter as it offers low conduction losses and low input current ripple increases the life span of renewable energy sources the inductors leakage current recycles to the output. Hence, large current spikes across the power switches are decreased, besides, lower voltage stresses. As a result, high efficiency with reduced cost converter is attained.

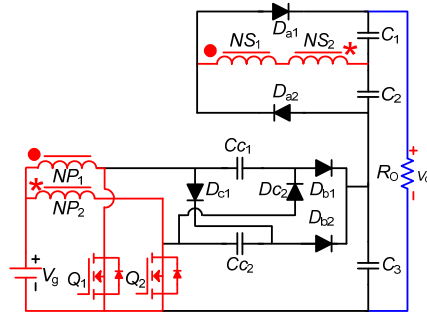


Fig. 24. interleaved boost converter with voltage multiplier [137]

### 3.3.9.3. ZVS Interleaved boost converter

Input current is interleaved using two inductors on the primary side in order to reduce conduction losses and current ripple of coupled inductors and across the power switch. ZVS interleaved boost converter with an active-clamping circuit is presented in Fig. 25 [138]. A SC and two coupled inductors with low turns ratio are employed to attain high voltage gain. This reduced turns ratio condenses byproducts of coupled; leakage inductance and copper losses. Additionally, voltage stresses are lessened at the output. Here, zero voltage switching (ZVS) is observed as active clamping circuit is employed. Also, issue of diode reverse recovery for every diodes is alleviated. Now, higher efficiency can be expected with fewer switching losses.

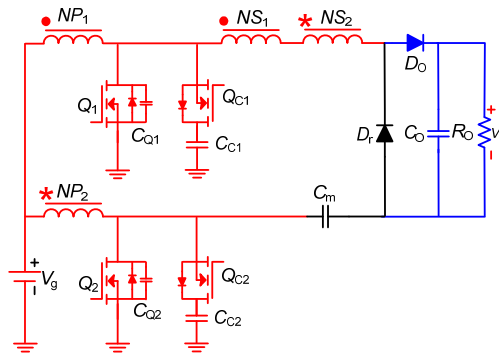
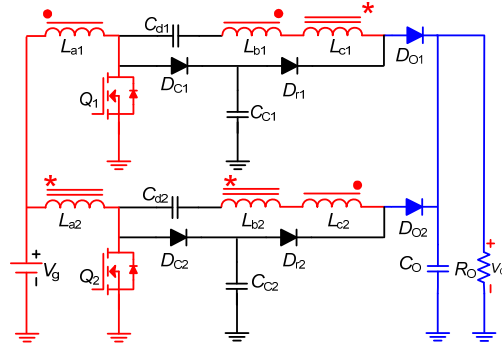


Fig. 25. ZVS interleaved TL boost converter [138]

### 3.3.9.4. Interleaved high step up converter

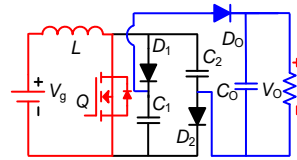
There are three windings on each core. Two coupled inductors are utilized in this topology. Where, the third winding is interleaved to the next phase as presented in Fig. 26. Here, this converter compared with the conventional boost converter can achieve high voltage gain. As the turns ratio and duty cycle increase higher voltage gain is attained. This feature allows the converter to surpass the requirement of operating the switching under extreme duty cycle, moreover the switch can avoid large peak current, as experienced by basic boost converter when utilized in high voltage applications. Additionally, voltage multiplier cells are connected in series with the power stage which creates an extra boost in high voltage gain under same duty cycle and similar turns ratio. As a result of the leakage inductance from third interleaved winding, switch  $S_1$  and  $S_2$  turn-on under ZCS condition, this minimizes the switching losses. Furthermore, leakage inductance from third interleaved winding reduces the output diode reverse recovery losses.



**Fig. 26.** Interleaved high step up converter [139]

### 3.4. Switched Capacitor based DC-DC Boost Converter with Extendable Voltage gain

Figure 27 presents an example to attain high voltage gain by incorporating 2-stage Switched Capacitor architecture to the basic boost converter. This SC converter design topology remains extendable and non-isolated. By implanting Switched Capacitor combinations with a boost converter, the switch ON time can be lessened while attaining a higher output voltage. In addition, voltage stress on the semiconductor devices is reduced. Moreover, the input current ripple is reduced as same voltage gain is achieved by utilizing lower duty cycle compared to the basic boost converter design. Table I compares the voltage gain and semiconductor component stress for both basic boost converter and 2-stage switched capacitor based boost converter. It is theoretically analyzed that by inserting a switched capacitor technique the voltage stress on the semiconductor devices can be halved against the basic boost converter.



**Fig. 27.** 2-Stage Switched Capacitor based boost converter

**TABLE I**  
CATEGORIZATION OF TOPOLOGIES

Parameters	Basic boost converter	Switched capacitor based boost converter
Gain	$\frac{1}{(1+D)}$	$\frac{2}{(1+D)}$
Switch voltage stress	$V_o$	$\frac{V_o}{2}$
Diode voltage stress	$V_o$	$\frac{V_o}{2}$

For a stand-alone PV system, the input voltage response of the presented 2-Stage Switched Capacitor converter operation utilizing conventional MPPT techniques [140, 141] can be theoretically analyzed as follows:

#### 3.4.1. Input Voltage response at high duty ratio

The effective resistance seen by the source for the boost converter can be presented as:

$$R_{pv} = \frac{V_{pv}}{I_{pv}} = R(1-D)^2 \quad (8)$$

Similar to the conventional Boost converter, the effective resistance for the 2-Stage Switched Capacitor Boost converter can be expressed as,

$$R_{pv} = \frac{V_{pv}}{I_{pv}} = \frac{R(1-D)^2}{4} \quad (9)$$

Convergence rate of the input voltage can be attained as,

$$\frac{\Delta V_{pv}}{\Delta D} = \frac{(D-1)}{2} k \quad (10)$$

### 3.4.2. Input Voltage response near MPP

Similarly, the change in voltage with respected to Duty cycle, closer to MPP can be realized as,

$$\frac{\Delta V_{pv}}{\Delta D} = \frac{(D-1)V_{MPP}}{(1-D)^2} \quad (11)$$

### 3.4.3. Input Voltage response at low duty ratio

Further, the change in voltage with respect to Duty cycle, away from MPP at low Duty ratio can be realized as,

$$\frac{\Delta V_{pv}}{\Delta D} = \frac{R}{4} \left( \frac{\Delta I_{pv}}{\Delta D} (1-D)^2 \right) + \frac{4(2D-2)V_{pv}}{(1-D)^2} \quad (12)$$

Therefore, owing to the varying input voltage response at different duty ratio for direct control implementation of MPPT, it is necessary to consider the design and dynamics of the proposed converter while employing for PV systems.

## 4. Discussion

List of all the topologies analyzed has been presented in Table II. Moreover, the high voltage gain values, switch, output diode and multiplier diodes voltage stress for all 32 modified topologies based on the TL boost converter are noted and equations given by the authors are listed in Tables II-V. Furthermore, Table II shows the characteristics for cascaded boost converter, 3-Level, interleaved, Multiport and switched inductor-based boost converters. Table IV shows the characteristics for switched capacitor-based boost converters. Table V shows the characteristics for coupled inductor, active network and boost converter with 3 state switching.

**TABLE II**  
CATEGORIZATION OF TOPOLOGIES

	#	Category	#	Topology
Topologies capable of delivering fixed voltage gain	1.	Conventional boost converter	1.	Fig. 2. (a) Conventional boost converter
	2.	Conventional 3-level Boost-based Converters	2.	Fig.5. (a) Conventional three level boost converter [82-87].
			3.	Fig.5. (b) Single switch quadratic boost converter [85, 86].

Topologies capable of delivering (n) times voltage gain		4. Fig.5. (c) Quadratic three level boost converter [88].
	3. Switched inductor-based boost converters	5. Fig.6. (a) <i>SL</i> boost converter [89].
		6. Fig.6. (b) High step up <i>SL</i> boost converter [90].
	4. Switched capacitor-based boost converters with fixed voltage gain	7. Fig.8. (a) Ćuk derived converter [91].
		8. Fig.8. (b) Zeta derived converter [91].
		9. Fig.8. (c) Type-1 boost-buck-boost-based [91].
		10. Fig.8. (d) Type-2 boost-buck-boost-based [91].
	5. Active network-based boost converters	11. Fig.9. (a) Active-network based DC-DC converter [90].
		12. Fig.9. (b) <i>SL</i> based <i>ANC</i> [92].
		13. Fig.9. (c) <i>SL</i> and <i>SC</i> based <i>ANC</i> [92].
	6. Cascaded Boost Converter	14. Fig.10. Conventional cascaded boost converter [93].
	7. Multiport-based boost converters	15. Fig.11. High voltage gain multiport converter [101].
	8. Switched capacitor-based boost converters with ( <i>n</i> ) times voltage gain	16. Fig.12. (a) Super-lift with Elementary Circuit [102].
17. Fig.12. (b) Modified voltage lifter [103].		
18. Fig.13. (a) Dickson multiplier-based boost converter [104].		
19. Fig.13. (b) Cockcroft Walton multiplier-based boost converter [104].		
20. Fig.14. (a) Boost derived MIESC <i>SC</i> -cell converter[91].		
21. Fig.14. (b) Buck–boost derived MIESC <i>SC</i> -cell converter[91].		
22. Fig.15. Hybrid boosting converter [113].		
9. Coupled inductor-based boost converters	23. Fig.16. Active clamp coupled-inductor-based converter [131].	
	24. Fig.17. active clamp-coupled inductor-based converter [132].	
	25. Fig.18. single-phase high step-up converter with coupled inductor multiplier [109].	
	26. Fig.19. coupled inductor high voltage gain DC-DC converter [133].	
	27. Fig.20. single-switch converter with high step-up gain [62].	
	28. Fig.21. High gain input-parallel output-series DC-DC converter with dual coupled inductors [134].	
10. Three-state switching-based boost converters	29. Fig.22. 3-State Switching Boost Converter Mixed With Magnetic Coupling and Voltage Multiplier [135].	
11. Interleaved boost converters	30. Fig.23. Conventional interleaved boost converter [136].	
	31. Fig.24. interleaved boost converter with voltage multiplier [137].	
	32. Fig.25. <i>ZVS</i> interleaved transformer less boost converter [138].	
	33. Fig.26. Interleaved high step up converter [139].	

**TABLE III**  
CHARACTERISTICS LISTED FOR VARIOUS MODIFIED BOOST-BASED TOPOLOGIES

Characteristics	Topology										
	1	2	3	4	5	6	7	8	9	10	11
Voltage stress across the switch	$V_o$	$\frac{V_o}{2}$	$V_o$	$\frac{V_o}{2}$	$\frac{V_o + V_{in}}{2}$	$\frac{V_o + V_{in}}{2}$	$\frac{V_o}{2}$	$\frac{1}{(1+D)}$	$\frac{V_o}{2}$	$\frac{1}{(1+D)}$	$\frac{V_{in} + 1}{V_{in}} V_o$
blocking voltage of the output diode	$V_o$	$\frac{V_o}{2}$	$V_o$	-	$\frac{V_o + V_{in}}{2}$	$\frac{V_o + V_{in}}{2}$	$\frac{V_o}{2}$	$\frac{1}{(1+D)}$	$\frac{V_o}{2}$	$\frac{1}{(1+D)}$	$\frac{V_{in} + 1}{V_{in}} V_o$
blocking voltage of the voltage multiplier diodes	$V_o$	-	$V_o$	$\frac{V_o}{2}$	-	-	$\frac{V_o}{2}$	$\frac{1}{(1+D)}$	$\frac{V_o}{2}$	$\frac{1}{(1+D)}$	/
Voltage gain	$\frac{1}{1-D}$	$\frac{2}{1-D}$	$\left(\frac{1}{1-D}\right)^2$	$\frac{1}{2 \cdot (1-D)^2}$	$\frac{1+D}{1-D}$	$\frac{1+D}{1-D}$	$\frac{2}{1-D}$	$-\frac{1+D}{1-D}$	$\frac{2}{1-D}$	$-\frac{1+D}{1-D}$	$\frac{1+3D}{1-D}$
Number of switches	1	2	1	2	1	2	1	1	1	1	2
Number of diodes	1	2	3	4	4	1	3	3	3	3	7
Number of capacitors	1	2	2	3	1	1	3	3	3	3	1
Number of inductors	1	1	2	2	2	2	1	1	1	1	4
Number of inductor cores	1	1	2	2	2	2	1	1	1	1	4
Total components	5	8	10	13	10	8	9	9	9	9	18
Tested switch at frequency	100 kHz	100 kHz		50 kHz	40 kHz	100 kHz	100 kHz	-	-	-	100 kHz
Tested input voltage	35			34	12 V	12 V	12 V	-	-	-	20-40
Tested output voltage	380 V			380 V	60 – 100 V	60 – 100 V	90 V	-	-	-	200 V
Number of input sources	1			1	1	1	1	-	-	-	1
Tested output power	100 W			350 W	50 W	100 W	40 W	-	-	-	200 W
Converter efficiency	85 %			85 %	91 %	92 %	91 %	-	-	-	91.1 %

**TABLE IV**  
CHARACTERISTICS LISTED FOR VARIOUS MODIFIED BOOST-BASED DC-DC CONVERTERS

Characteristics	Topology											
	12	13	14	15	16	17	18	19	20	21	22	
Voltage stress across the switch	$\frac{V_o + V_{in}}{4}$	$V_o$	$\frac{V_{in}}{(1-D)}$	$\frac{1}{3-D}$	$\frac{V_o}{2}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{V_o + V_i}{2}$	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{1}{3-D}$	
blocking voltage of the output diode	/	$V_o$	$\frac{V_{in}}{(1-D)}$	$\frac{1}{3-D}$	-	$\frac{1}{3}$	-	$2 \cdot V_o$	-	-	-	
blocking voltage of the voltage multiplier diodes	$\frac{V_o + V_{in}}{2}$	-	$\frac{V_{in1}}{(1-D)} + \frac{V_{in2}}{(1-D)}$	$\frac{1}{3-D}$	$\frac{V_o}{2}$	$\frac{1}{3}$	$\frac{1}{3}$	-	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{V_{in}}{(1-d)}$	
Voltage gain	$\frac{3+5D}{1-D}$	$\left(\frac{1}{1-D}\right)^N$	$\frac{N+1}{2} \cdot \frac{1}{(1-D)} + \frac{N+1}{2} \cdot \frac{1}{(1-D)}$	$\frac{3-D}{1-D}$	$\frac{2}{1-D}$	$\frac{3}{1-D}$	$\frac{3}{1-D}$	$\frac{(1+D)}{(1-D)}$	$\frac{2+(N-1)E}{1-D}$	$\frac{1+ND}{1-D}$	$\frac{3-D}{(1-D)}$	

Number of switches	2	2	2	1	1	1	1	2	1	1	1
Number of diodes	9	2	4	4	3	5	5	1	4	4	4
Number of capacitors	3	2	4	4	3	5	5	1	5	5	4
Number of inductors	4	2	2	1	1	1	1	2	2	2	1
Number of inductor cores	4	2	2	1	1	1	1	1	2	2	1
Total components	22	10	14	11	9	13	13	7	14	14	11
Tested switch at frequency	100 kHz	100 kHz	100 kHz	100 kHz	50 kHz	-	75 kHz	100 kHz	10 kHz	-	40 kHz
Tested input voltage	20-40 V	120 V	20 V	66-190 V	12 V	-	12 V	12 V	25-36-45 V	-	
Tested output voltage	400 V	400 V	400 V	660 V	80 V	-	110 V	60-100 V	380 V	-	380 V
Number of input sources	1	1	2	1	1	-	1	1	1	-	1
Tested output power	200 W	300 W	400 W	15 W	-	-	-	40 W	40 W	-	240 W
Converter efficiency	91.8 %	85 %	91.4 %	78 %	-	-	-	91 %	96 %	-	94.44 %

**TABLE V**  
CHARACTERISTICS LISTED FOR VARIOUS MODIFIED BOOST-BASED DC-DC CONVERTERS

Characteristics	Topology											
	23	24	25	26	27	28	29	30	31	32	33	
Voltage stress across the switch	$\frac{1}{3}$	$\frac{V_o}{N+1}$	$\frac{V_o}{2(N+1)}$	$\frac{1}{1-D} + \frac{D(N-1)}{2(1-D)}$	$\frac{V_o}{N(2+d)+3}$	$\frac{V_o}{2(N+1)}$	$\frac{V_o}{2(2N+3)}$	$V_o$	$\frac{V_o}{2(N+1)}$	$\frac{V_o}{2(N+1)}$	$\frac{V_o}{2(N+1)}$	
blocking voltage of the output diode	$\frac{1}{3}$	$V_o$	$\frac{V_o}{2}$	$\frac{1}{1-D} + \frac{D(N-1)}{2(1-D)}$	$\frac{(N+1)V_o}{N(2+D)+3}$	-	-	$V_o$	-	$V_o$	-	
blocking voltage of the voltage multiplier diodes	-	-	-	$\frac{1}{1-D} + \frac{D(N-1)}{2(1-D)}$	-	$\frac{N \cdot V_o}{(N+1)}$	$\frac{(2N+1)}{(2N+3)} V_o$	-	$\frac{N \cdot V_o}{(N+1)}$	$\frac{V_{in}}{(1-D)}$	$\frac{2 \cdot N + 1}{2(N+1)}$	
Voltage gain	$\frac{ND+1}{1-D}$	$\frac{N-1}{1-D}$	$\frac{2(1+N)}{(1-D)}$	$\frac{2+N}{1-D} + N$	$\frac{N(2+D)+3}{(1-D)}$	$\frac{2(N+1)}{(1-D)}$	$\frac{(2N+3)}{(1-D)}$	$\frac{1}{1-D}$	$\frac{2(N+1)}{(1-D)}$	$\frac{4(N+1)}{(1-D) + \sqrt{(1-D)}}$	$\frac{2(N+1)}{(1-D)}$	
Where: $Q = 16 \cdot f_s \cdot L_k / R_o$												
Number of switches	2	2	2	1	1	2	2	2	2	4	2	
Number of diodes	1	2	4	4	5	4	4	2	6	2	6	
Number of capacitors	1	1	4	4	5	4	4	1	5	5	5	
Number of inductors	3	2	2	3	2	2	2	2	2	4	2	
Number of inductor cores	3	1	1	2	1	2	2	2	2	2	4	
Total components	10	8	13	14	14	14	14	9	17	17	19	
Tested switch(es) at frequency	50 kHz	100 kHz	100 kHz	50 kHz	50 kHz	40 kHz	50 kHz	100 kHz	40 kHz	50 kHz	50 kHz	
Tested input voltage	25-40 V	40-56 V	40-56 V	24 V	24 V	18-36 V	16-22 V	40 V	40 V	12-14 V	30-45 V	



Tested output voltage	200 V	380 V	380 V	400 V	400 V	200 V	200 V	380 V	380 V	120 V	380 V
Number of input sources	1	1	1	1	1	1	1	1	1	1	1
Tested output power	100 W	500 W	500 W	200 W	100 W, 300 W	200 W	400 W	500 W	400 W - 1 kW	150 W, 500 W	1 kW
Converter efficiency	94.4 %	96.4 %	96.9 %	95.7 %	95.4 %, 93.9 %	94.37 %	-	85 %	97.1 % - 96.4 %	96.8 %, 91.2 %	95.1 %

It is tricky to give a comparative analysis of the performance of each topology simply based on the level of its voltage gain curve, particularly with different number of component count for different topologies. In most of these topologies. Higher voltage gain values can be attained either by increasing turns ratio of interleaved inductor topologies and coupled or by including more number of components. The demerits include higher cost, complexity and bulkiness of converter topologies. As *SC* cell-based topologies in Table IV at the cost of higher component count can achieve a higher voltage gain against the basic boost. Also, the coupled and interleaved inductor-based topologies in Table III and Table V can attain higher gain by high turns ratio which in response will increase its leakage inductance. As a result of this analysis, selection of the topology for application of micro PV inverters, uninterruptible power supplies, fuel cell and etc, must be made after looking at elements involved and attained voltage ratio. After achieving a higher voltage gain the output diode and switch voltage stress is a crucial factor as the overall cost of the system can increase by employing higher rated components. Furthermore, voltage stress on semiconductor components is evaluated. This can offer a two times higher voltage gain against the basic boost converter with 3-level and cascaded boost converter modifications, but the power losses are also doubled as these topologies involve two switches. Moreover, cascaded boost converters confronts the problem of equivalent switch stress and output voltage. Application with low voltage variation, *SC* cell-based boost converters with fixed voltage gain can be employed, which have simpler structure and higher efficiency. If a comparatively high voltage gain is required, the converters from *SC*-cell based boost converters with  $n$  times voltage gain can be utilized at the expense of additional components. In advantage the switches and diodes voltage stresses is reduced higher than one-half of voltage at the output. Therefore, overall cost of the system and switching losses can be subsided by utilizing lower voltage rated power devices with low resistance  $R_{DS(on)}$ . Moreover, by incorporating a coupled inductor, interleaved or 3-state switching based converters higher voltage gain can be attained. As a commendable merit these converters allow current sharing. However, voltage ringing is often resulted due to resonance between intrinsic capacitance and leakage inductance of active switch, which leads to poor efficiency. In addition, leakage inductance has the ability to compensate the falling current rates of diodes. Nullifying the diode reverse-recovery issues. Moreover, voltage stresses on the switch is one third of the output voltage and leakage-inductor energy is available to be reprocessed at the output. Table VI presents the modification techniques used in the basic boost converter.

**TABLE VI**  
MODIFICATION TECHNIQUES USED IN THE BOOST-BASED DC-DC CONVERTER TOPOLOGIES

#	Topology	Modification techniques used									
		Non-extendable voltage gain	Extendable voltage gain	SC-Cell	SI-Cell	Interleaved inductor	Coupled inductor	Multiport	Cascaded	SS3	Active network
1.	Fig. 1. (a)	-	-	-	-	-	-	-	-	-	-
2.	Fig.5. (a)	yes	-	-	-	-	-	-	-	-	-

3.	Fig.5. (b)	yes	-	-	-	-	-	-	-	-	-
4.	Fig.5. (c)	yes	-	-	-	-	-	-	-	-	-
5.	Fig.6. (a)	yes	-	-	yes	-	-	-	-	-	-
6.	Fig.6. (b)	yes	-	-	yes	-	-	-	-	-	-
7.	Fig.8. (a)	yes	-	yes	-	-	-	-	-	-	-
8.	Fig.8. (b)	yes	-	yes	-	-	-	-	-	-	-
9.	Fig.8. (c)	yes	-	yes	-	-	-	-	-	-	-
10.	Fig.8. (d)	yes	-	yes	-	-	-	-	-	-	-
11.	Fig.9. (a)	yes	-	-	yes	-	-	-	-	-	yes
12.	Fig.9. (b)	yes	-	-	yes	-	-	-	-	-	yes
13.	Fig.9. (c)	-	yes	yes	yes	-	-	-	-	-	-
14.	Fig.10.	-	yes	-	-	-	-	-	yes	-	-
15.	Fig.11.	-	yes	yes	-	-	-	yes	-	-	-
16.	Fig.12. (a)	-	yes	yes	-	-	-	-	-	-	-
17.	Fig.12. (b)	-	yes	yes	-	-	-	-	-	-	-
18.	Fig.13. (a)	-	yes	yes	-	-	-	-	-	-	-
19.	Fig.13. (b)	-	yes	yes	-	-	-	-	-	-	-
20.	Fig.14. (a)	-	yes	yes	-	-	-	-	-	-	-
21.	Fig.14. (b)	-	yes	yes	-	-	-	-	-	-	-
22.	Fig.15.	-	yes	yes	-	-	-	-	-	-	-
23.	Fig.16.	-	yes	-	-	yes	-	-	-	-	-
24.	Fig.17.	-	yes	yes	-	-	yes	-	-	-	-
25.	Fig.18.	-	yes	yes	-	-	yes	-	-	-	-
26.	Fig.19.	-	yes	yes	-	-	yes	-	-	-	-
27.	Fig.20.	-	yes	yes	-	-	yes	-	-	-	-
28.	Fig.21.	-	yes	yes	-	-	yes	-	-	-	-
29.	Fig.22.	-	yes	yes	-	-	-	-	-	yes	-
30.	Fig.23.	-	yes	-	yes	-	-	-	-	-	-
31.	Fig.24.	-	yes	yes	-	yes	-	-	-	-	-
32.	Fig.25.	-	yes	yes	-	yes	-	-	-	-	-
33.	Fig.26.	-	yes	yes	-	yes	-	-	-	-	-

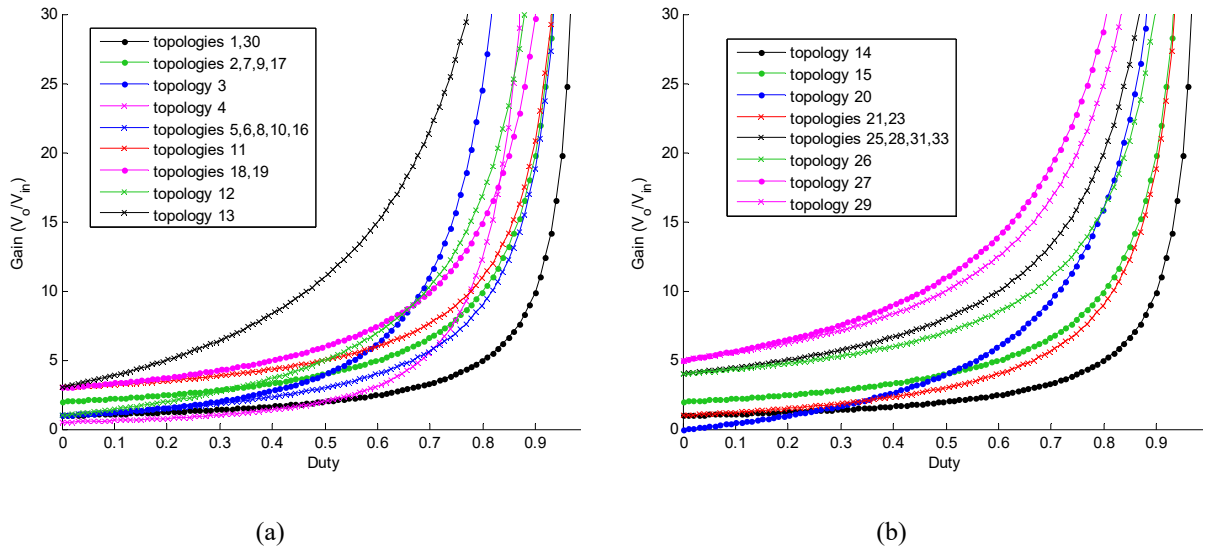


Fig. 27. (a) topologies with voltage gains (b) topologies with (n) times voltage gains.

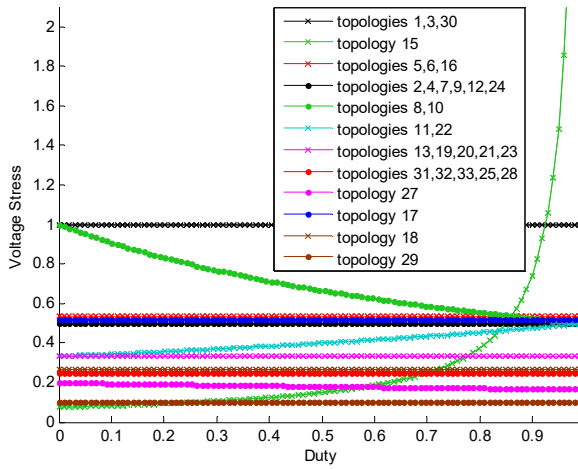


Fig. 28. Voltage stress on switch(es).

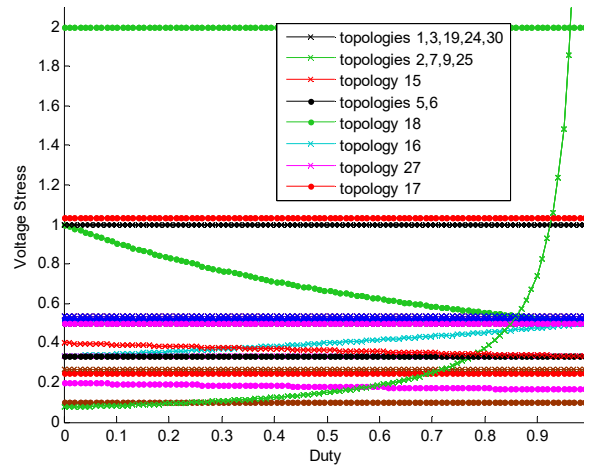


Fig. 29. Voltage stress on output diode.

## 5. Conclusion

The output voltage on conventional boost converter can only be stepped up by increasing the on time of the semiconductor components. Additionally, if on time of the switch is increased more than 90 %; the power losses amplify, which will lead to efficiency degradation. In light of the aforementioned problem, this paper presents a comparative analysis on wide range of topologies based on the structure of conventional boost converter. Moreover, the topologies are categorized

under their ability to provide fixed or  $n$  times voltage gain, additionally; topologies are compared based on the switch on time versus the voltage gain.

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