Solid Electrolytic Substrates for High Performance TMD Transistors and Circuits

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Introduction

Ionic liquids/gels have been used to realize field-effect-transistors (FETs) with two dimensional (2D) transition metal dichalcogenides (TMDs) [1]. Although near ideal gating has been reported with this biasing scheme, it suffers from several issues such as, liquid nature of the electrolyte, its humidity dependency and freezing at low temperatures [2]. Recently, air-stable solid electrolytes have been developed, thanks to the advancement in battery technology [3]. Although insulator-to-metal transition has been reported, the realization of 2D TMD FETs on solid electrolytic substrate has not been reported so far to the best of our knowledge [4]. In this work, we demonstrate a lithium ion (Li-ion) solid electrolytic substrate based TMD transistor and a CMOS amplifier, with near ideal gating efficiency reaching 60 mV/dec subthreshold swing, and amplifier gain ~34, the highest among comparable inverters.

Experimental Process

The schematic of the device is shown in Fig. 1(a). We used double sided polished Li-ion solid electrolytic substrate (LICGC™ from Ohara) to fabricate transistors. CVD MoS_2 was transferred from growth substrate to electrolytic substrate by conventional wet transfer method. Exfoliated materials were obtained by using blue tape/PDMS based exfoliation/transfer. E-beam lithography was used to pattern drain/source contacts. Ni (Pd) contact metals were deposited by e-beam evaporation, followed by lift-off process for MoS_2 (WSe_2). Active channel region was defined with CF_4/O_2 plasma etching. Backside was silver coated before electrical measurement.

Results

Fig. 1(a) shows the working mechanism of the electrolytic substrate. With the application of a positive back-gate voltage, the mobile Li ions are repelled from the back-gate/electrolyte (GE) interface, and accumulate at the electrolyte/ semiconductor interface (ES). This, in turn, leaves negative vacancies at GE interface and induces electrons inside semiconductor at ES interface. The equivalent capacitance is then the two capacitances, C_{GE} and C_{ES}, connected in series. Fig. 1(b) shows effective capacitance/phase angle vs. frequency of the electrolytic substrate obtained with an LCR meter. At 4Hz, the capacitance is ~ 2.10 μF/cm^2 with a phase angle of ~ -86°. Fig. 2 shows band diagram using chemical potentials. In OFF state, the Fermi levels (not shown) are aligned by the formation of two EDLs at the interfaces. Lithium ions diffuse towards the center of the electrolyte, leaving behind negative vacancies at both the interfaces. With the application of positive back-gate voltages, MoS_2 bands bend downwards, leading to the accumulation of electrons in the conduction band and the device turns on. Fig 3(a) shows transfer characteristics of a single layer CVD MoS_2 FET. An enhancement mode operation (V_{TH} ~ +0.30V) with the absence of hole branch, signifying unipolar conduction, is observed. Inset shows linear I_D-V_D, suggesting an Ohmic contact. Output characteristics are shown in Fig 3(b), with saturation being reached at higher drain voltages. Figs. 4(a) and (b) show transfer and output characteristics, respectively, for a WSe_2 FET. A CMOS inverter has been realized with n-MoS_2 and p-WSe_2 FET, as shown in Fig. 5(a). Output vs. input characteristics are shown in Fig. 5(b). Inset shows the gain, which reaches ~ 34 at an input voltage of 0.38V, compared with other reported works in Fig. 5(c). To gain insight into microscopic conduction, microwave impedance microscopy (MIM) technique is used. At around 0.30V gate voltage a homogeneous channel is formed as evident from local conductivity data shown in Fig. 6(c), signifying a smooth interface between the semiconductor channel and underlying substrate.

Conclusion

In summary, we have demonstrated near ideal gating in both n-type and p-type TMD FETs and a gain ~34 in CMOS inverter realized on Li ion electrolytic substrate. Solid electrolytic substrates can be a platform to replace ionic liquids for advanced transistor device and surface physics study.

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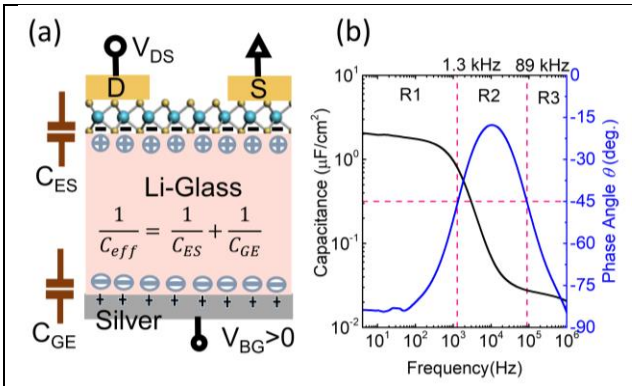

Fig. 1. (a) Schematic diagram of a Li ion electrolytic substrate with TMD channel on top and a silver coating at the bottom. The operation of the device is shown for positive back-gate voltage. (b) Capacitance/phase angle vs. frequency characteristics of the glass obtained with Ni/Li-glass/Ni configuration.

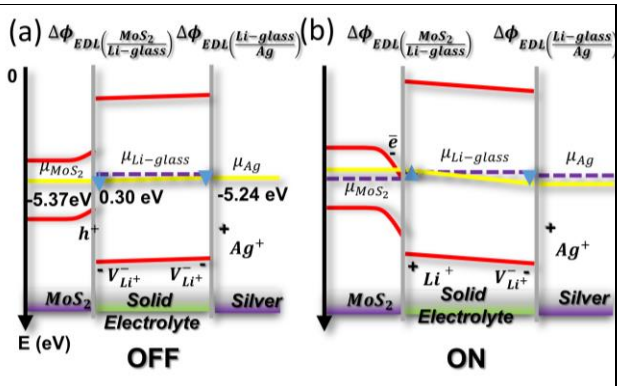

Fig. 2. Energy band diagram of TMD FET on Li-glass. Dashed violet and solid yellow lines represent the initial and final chemical potentials. (a) Channel is OFF. (b) Channel is turned on by applying a back-gate voltage.

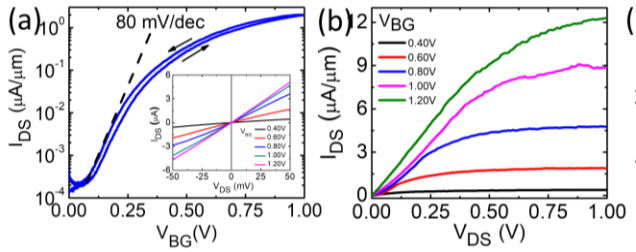

Fig. 3. (a) Transfer characteristics for a 1L CVD MoS_2. V_{TH} ~ 0.3V, ON/OFF ratio ~ 10^4 and hysteresis < 70mV. Inset shows linear I_D-V_D, suggesting an Ohmic contact. (b) Output characteristics of the same FET showing saturation for higher drain voltages.

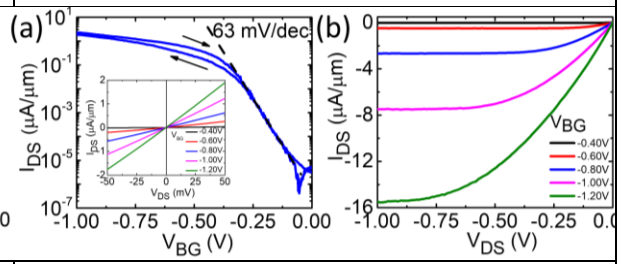

Fig. 4. (a) Transfer characteristics for a 4L WSe_2. V_{TH} ~ 0.34V, ON/OFF ratio ~ 10^7 and hysteresis < 120 mV. Inset shows linear I_D-V_D, suggesting an Ohmic contact. (b) Output characteristics of the same FET showing saturation for higher drain voltages.

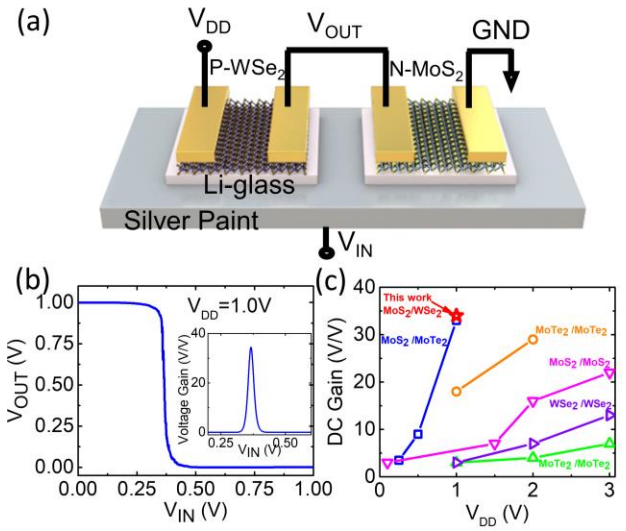

Fig. 5. (a) Schematic diagram of a CMOS inverter with n-type MoS_2 and p-type WSe_2. (b) Output vs. input characteristics. Inset shows the gain. (c) Comparison with other reported data in literature.

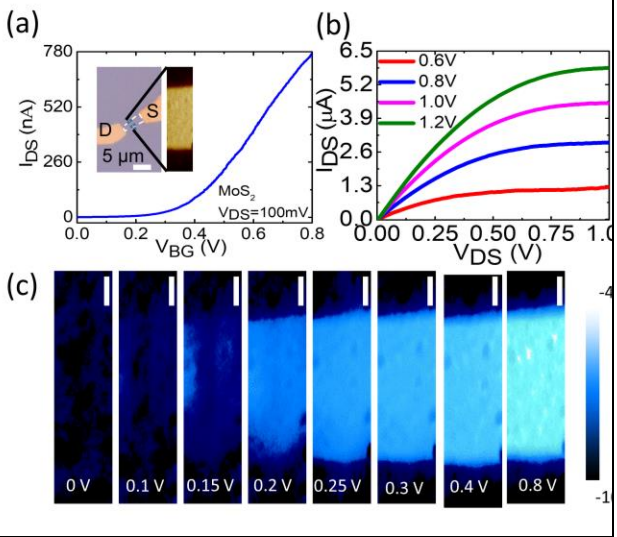

Fig. 6. (a) Transfer (b) Output characteristics of a MoS_2 FET. Inset of (a) shows the section of the channel. (c) Sheet conductivity map for the selected channel region. Scale bar 500nm.