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Design and Analysis of Efficient QCA Reversible Adders

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***Abstract*—**Quantum-dot Cellular Automata (QCA) as an emerging nanotechnology is envisioned to overcome the scaling and the heat dissipation issues of the current CMOS technology. In a QCA structure, information destruction plays an essential role in the overall heat dissipation, and in turn in the power consumption of the system. Therefore, reversible logic, which significantly controls the information flow of the system, is deemed suitable to achieve ultra-low power structures. In order to benefit from the opportunities QCA and reversible logic provide, in this paper, we first review and implement prior reversible full-adder art in QCA. We then propose a novel reversible design based on three- and five-input majority gates, and a robust one-layer crossover scheme. The new full-adder significantly advances previous designs in terms of the optimization metrics, namely, cell count, area, and delay. The proposed efficient full-adder is then used to design reversible Ripple Carry Adders (RCAs) with different sizes (i.e. 4, 8 and 16 bits). It is demonstrated that the new RCAs lead to 33% less garbage outputs, which can be essential in terms of lowering power consumption. This along with the achieved improvements in area, complexity, and delay introduces an ultra-efficient reversible QCA adder that can be beneficial in developing future computer arithmetic circuits and architectures.

***Index Terms*—** Reversible Computing, Quantum-Dot Cellular Automata (QCA), Full-Adder, Ripple Carry Adder, One-Layer Crossover Scheme, Five-input Majority Gate.

1. Introduction

Reversible logic was devised mainly to decrease energy dissipation and achieve low power circuits [1]. According to Landauer's investigations [2], each bit of information lost in a circuit produces *KTln2* Joules of heat energy, where *k* is the Boltzmann's constant and *T* is the absolute temperature. In order to avoid information loss and to minimize power dissipation in a circuit, all the computations must be performed in a reversible way [1]. In a reversible circuit, constructed from reversible gates, the information loss is avoided by providing a one to one mapping between the input and output vectors of the circuit. Therefore the input vector can be uniquely recovered from the output vector and vice versa.

Quantum-dot Cellular Automata (QCA) as a new nanotechnology has been explored for designing circuits such as full-adders [3-10], restoring and non-restoring array dividers [11], multiplexers and flip flops [13-15]. QCA as one of the candidate nanotechnologies to implement reversible logic gates [16-18], promises a dense and high speed structure at a nano scale. Different studies performed on QCA-based reversible circuits include: testable reversible latches [17], testable reversible sequential circuits [18], multi-function reversible gates [19], reversible multiplexers [20], reversible logic gates [21] and their testability [22]. This paper presents a novel reversible QCA full-adder based on three- and five-input majority gates, which outperforms previous designs in terms of area, delay, and complexity. The proposed circuit uses a reversible design that

compared to conventional QCA circuits, significantly improves the control of the information flow of the system and is deemed suitable to achieve ultra-low power structures. The new design has a one-layer structure and uses a robust and coplanar crossover scheme [23]. This design also uses robust three-input majority gates to achieve a reliable structure with respect to sneak noise paths [24-25]. The new high-performance full-adder is used to design reversible Ripple Carry Adders (RCAs) with different sizes (i.e. 4, 8 and 16 bits). These adders, compared to their counterparts, lead to significant improvements in terms of the number of garbage outputs, area, delay, and complexity. This can be beneficial in developing future efficient computer arithmetic circuits and architectures.

The remainder of this paper is organized as follows: In section 2, a brief background on QCA is provided. Section 3 surveys previous reversible full-adder designs. The proposed QCA reversible full-adder is introduced in section 4. Section 5 presents the design and analysis of RCAs. It also provides a detailed comparison of various reversible adders. Finally, section 6 gives concluding remarks.

2. QCA Background

A basic QCA cell contains four quantum dots and two excess electrons, through which a binary representation can be achieved by two stable arrangements of the electrons inside the cell (Fig. 1(a)). QCA circuits operate based on a specific clocking scheme as demonstrated in Fig. 1(b). This figure presents four QCA clocking waveforms with a 90^0 phase delay based on the Landauer clocking mechanism [4]. The fundamental building block of QCA circuits is a QCA majority gate. The layout of a robust three-input majority gate is shown in Fig. 1(c) [24-25]. Since in a three-input majority gate, the inputs may arrive from different paths and with different delays, three clocking zones with a 90^0 phase delay can be used to avoid the impact of the sneak noise paths on the output [24-25] (clocking zones 0, 1 and 2 in Fig. 1(c)).

Multi-layer and coplanar crossover schemes have been introduced to cross wires in QCA circuits [5, 23, 26-28]. Since the required technology for implementing a multi-layer QCA circuit has not yet been completely developed [4], the coplanar crossover scheme is used to design one-layer QCA circuits. The QCA layout of a robust coplanar crossover scheme [23] is shown in Fig. 1(d). This scheme is based on 90^0 QCA cells and uses two QCA clocking zones with 180^0 phase delay at the crossing point. In this scheme, when the horizontal QCA cells at the crossing point are in switch and hold phases, the QCA cells of the vertical wire are in release and relax phases and the signals can be transmitted to the outputs without any impact on each other [23]. Although this scheme, in contrast to another crossover technique [28] uses additional clocking zones at the vertical and horizontal wires (clocking zones 1 and 3 at the outputs *a* and *b* in Fig.1 (d)), based on the calculation of kink energy, these additional clocking zones are inevitable to address the sneak noise paths and to achieve a robust coplanar crossover scheme [23]. In order to have robust QCA designs, in this paper, this crossover scheme is used to design efficient and robust reversible full-adder and Ripple Carry Adders.

3. Reversible Gates and Full-Adders

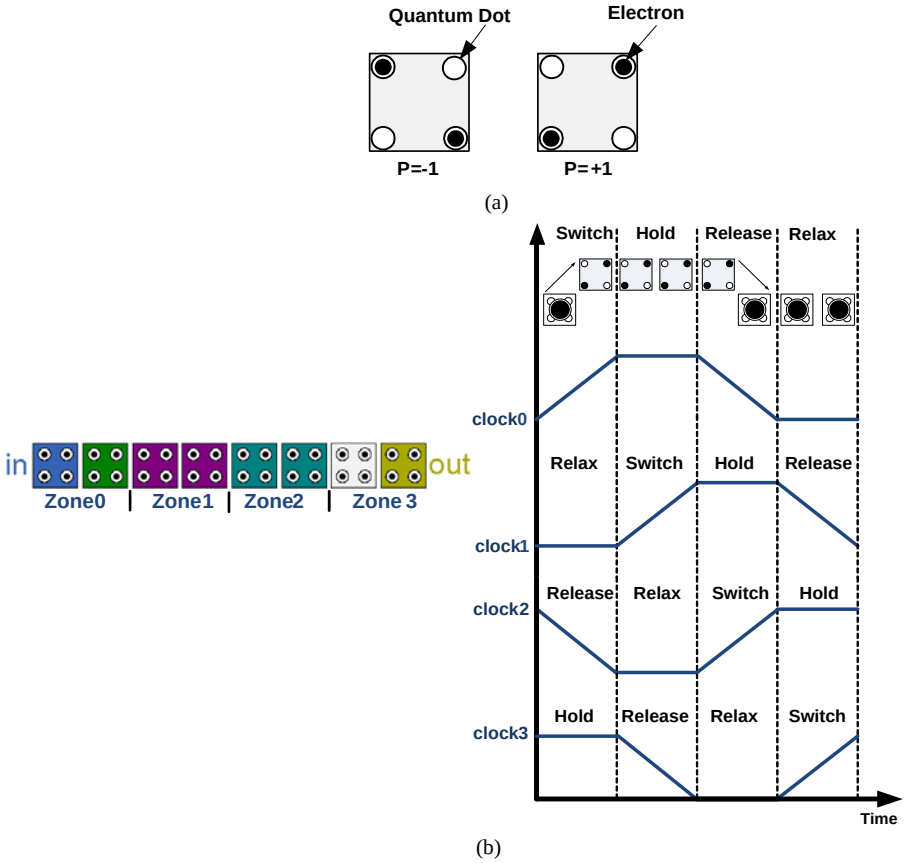
A reversible gate, as the basic building block of a reversible circuit, provides a one to one mapping between its input and output vectors. In other words, a unique output vector is generated from each input vector, and vice versa [29]. In order to achieve the reversibility condition, some extra inputs and/or outputs should be added to a reversible gate. These are called additional inputs and garbage outputs.

Fig. 2 depicts the structures of the most popular reversible gates including NOT, CNOT (Feynman), Toffoli [29], Peres [30] and Fredkin gates [31]. The quantum cost associated with a reversible gate is defined as the number of 1×1 and 2×2 reversible gates or quantum logic gates, where the n×n notation indicates a reversible gate with n inputs and n outputs [32].

To date, using the reversible gates, different types of reversible circuits have been introduced. In [33] novel reversible gates have been used to design carry look-ahead and carry skip BCD subtractors. Considering the importance of the field programmable gate arrays (FPGAs) in many applications [34], in [35] a 3 input reversible Programmable Logic Array architecture (RPLA) has been introduced. This design is constructed using Fredkin and Feynman gates and can be used to generate 28 functions. Also it can be configured to act as a 1-bit full adder and subtractor.

In addition, since the reversible arithmetic units such as subtractors, adders and multipliers are considered as the essential components of a quantum computing system, different studies have been done on designing efficient reversible units. In [36], a reversible half subtractor using reversible Fredkin and Feynman gate has been introduced. This structure is the used to design a reversible full subtractor. This study also presents a reversible binary parallel subtractor using the reversible half and full subtractors [36]. In [37], efficient reversible Carry look-ahead binary adders as one of the essential units to use in high performance computing were introduced. The presented designs use the properties of the reversible Peres gate and the TR gate to optimize the logic depth, quantum cost, and gate count compared to the existing designs.

Generally, the quantum cost, delay, and the number of garbage outputs are used as the major metrics of optimization in a reversible gate [38]. In QCA, however, other optimization metrics such as delay, area, complexity (number of QCA cells), and the number of majority gates, should also be taken into design consideration [18].



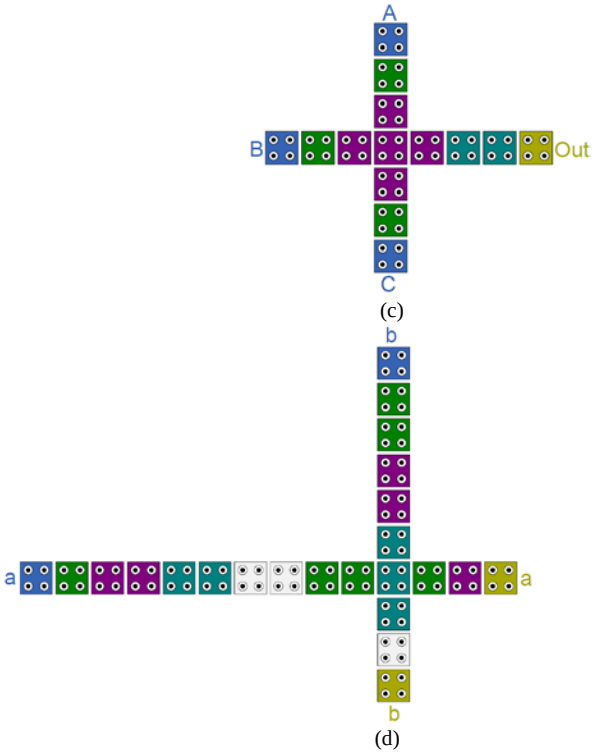
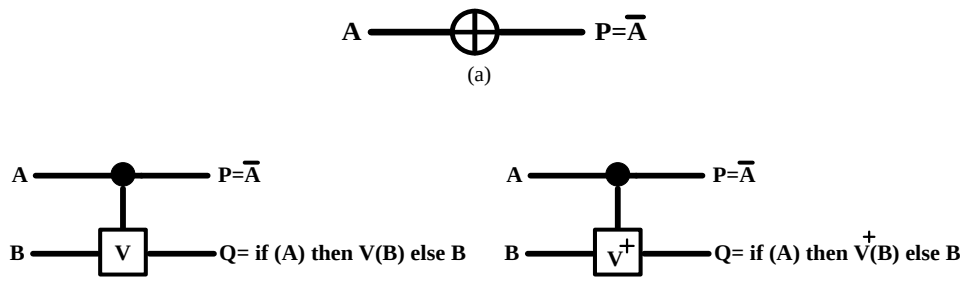


Fig. 1. (a) The 90^0 QCA cell and its binary encoding (b) A QCA wire constructed using four clocking zones based on the Landauer QCA clocking mechanism [4]. (c) The QCA layout of a robust three-input majority gate [24-25]. (d) The one-layer and robust crossover scheme [23].

As shown in Fig. 2 (a) and (b), the NOT and CNOT are 1×1 and 2×2 reversible gates, respectively. On the other hand, the Peres, Toffoli and Fredkin gates are 3×3 reversible gates (Fig. 2 (c-e)). The Toffoli gate as one of the most popular reversible gates is a two-through reversible gate in which two outputs are the same as inputs (the two outputs *P* and *Q* presented in Fig.2 (d)) [38]. As can be seen in Fig.2 (d), a Toffoli gate is implemented using 2 V gates, 1 V^+ gate and 2 CNOT gates.

Various design approaches have been proposed for implementing a reversible full-adder [39-54]. Table I lists a number of these designs and provides the schematics for each of them. Furthermore, two designs have so far been presented for a QCA reversible full-adder [55-56]. These QCA-based designs are demonstrated in Table II. The design in [55] is a 3*5 reversible gate. In contrast to [56], this design is constructed using six three-input majority gates (presented as first and second QCA1 in Table II). The design in [56] is a 4*4 gate with two garbage outputs. It consists of two Toffoli and two Feynman gates to operate as a reversible full-adder. Note that, both these designs use the multi-layer crossover scheme, which imposes challenges in terms of fabrication.



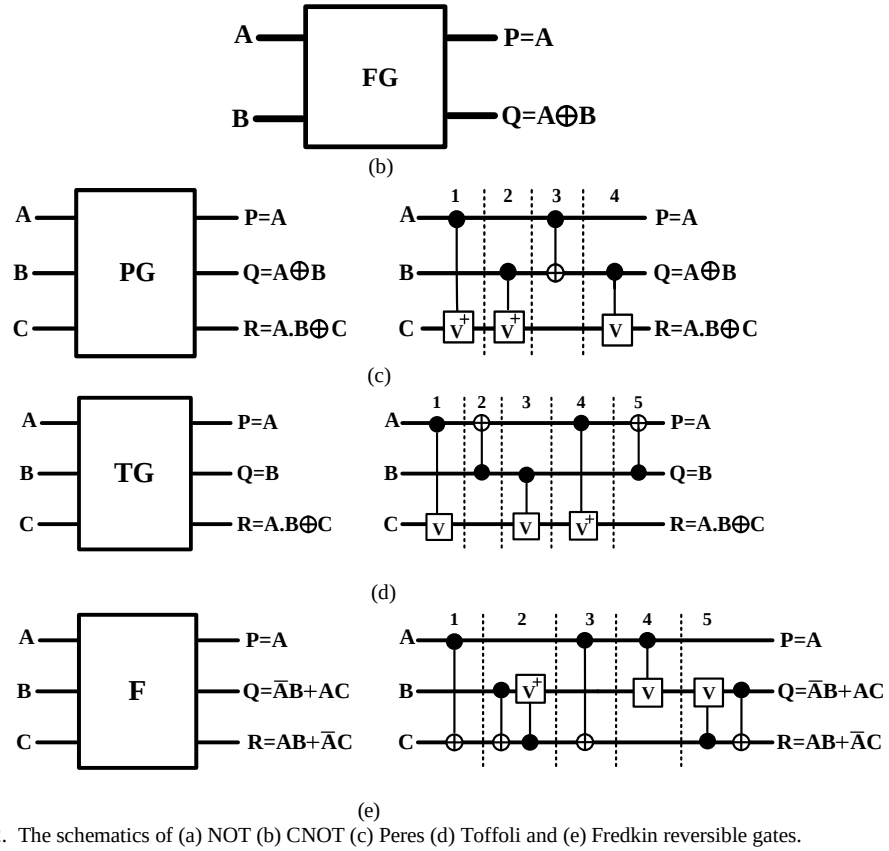


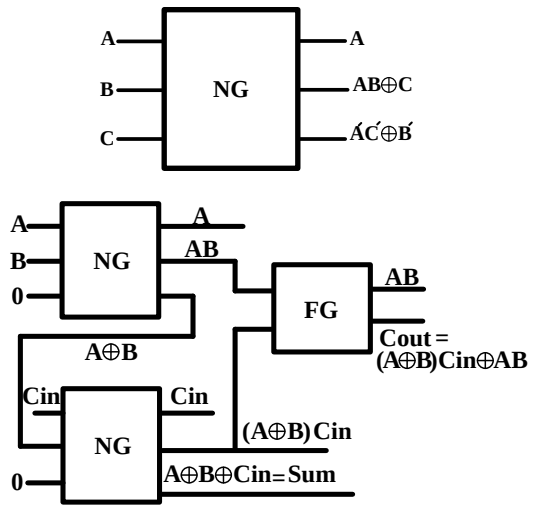
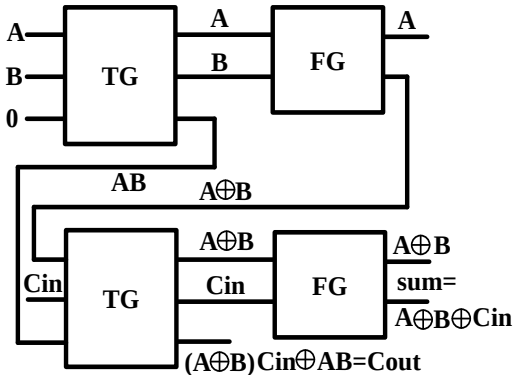
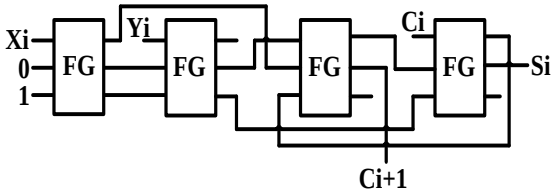
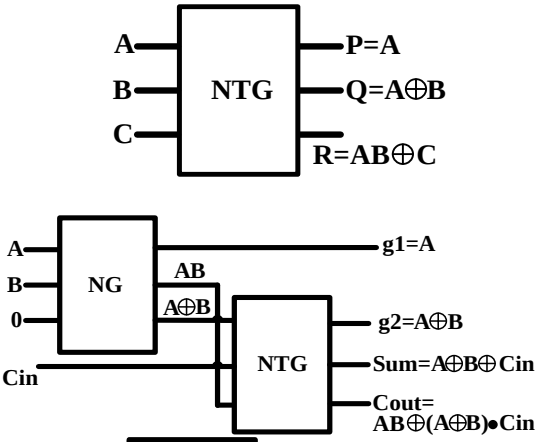
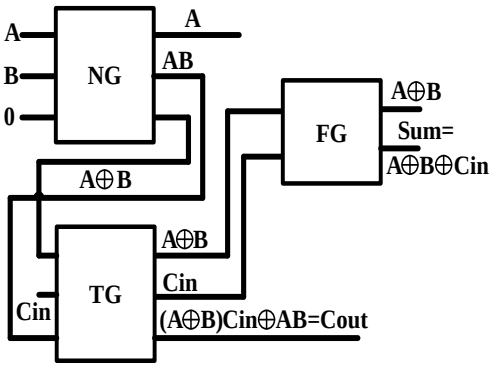
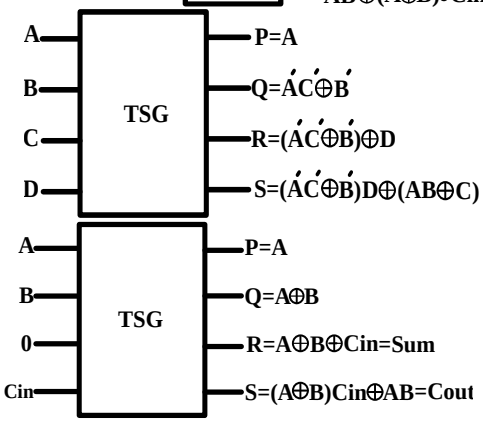
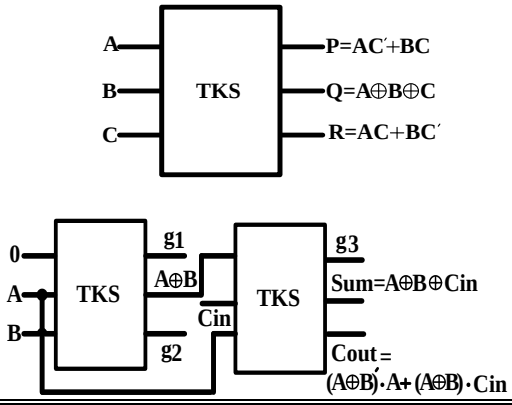
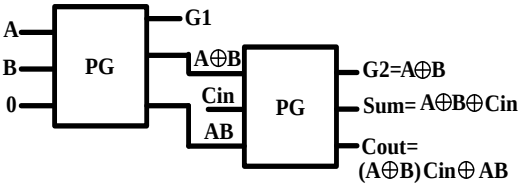
Fig. 2. The schematics of (a) NOT (b) CNOT (c) Peres (d) Toffoli and (e) Fredkin reversible gates.

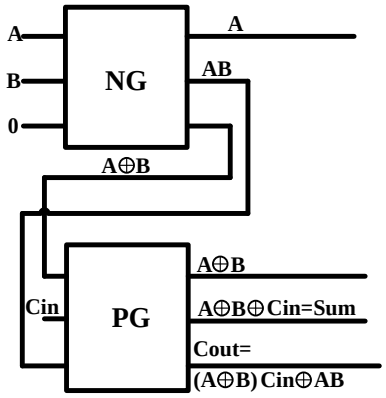
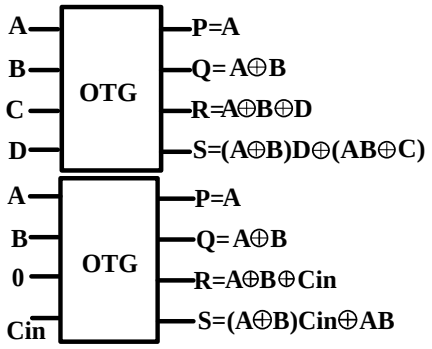
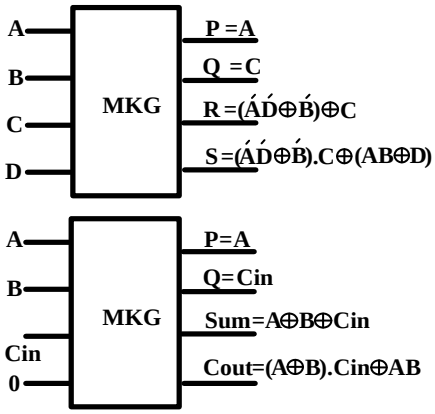
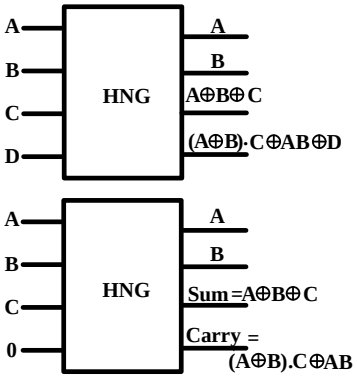
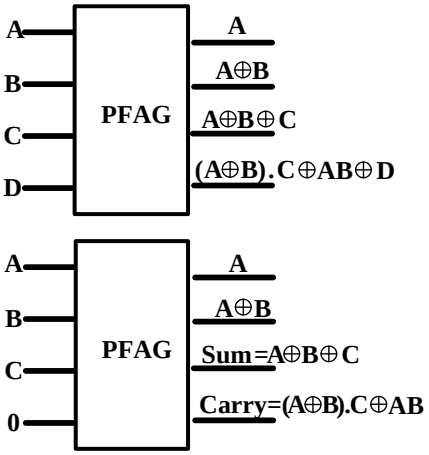
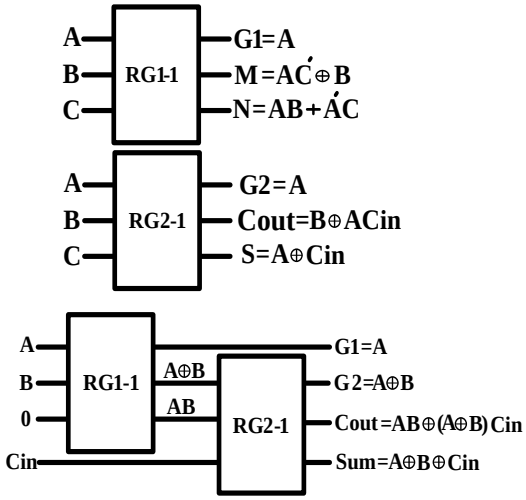
In order to compare the structure of previous reversible designs, we have investigated all the surveyed reversible full-adders [39-56], in terms of the number of inputs/outputs, the number of garbage outputs and the number of three-input majority gates. For those designs that have not been implemented using majority gates, we have used a simple rule to calculate the number of majority gates required to implement them. Since in QCA, an XOR gate can be implemented using three three-input majority gates and an AND/OR operation is implemented using one three-input majority gate, the total number of three-input majority gates in Table III is calculated based on the required number of XOR and AND/OR gates in a reversible full-adder. As Table III suggests, the QCA reversible design presented in [56] incurs the minimum number of three-input majority gates. This significantly improves, compared to other designs, the area, delay, and complexity metrics.

In the next section we introduce a new reversible full-adder, which further improves all the optimization metrics of a QCA reversible design. This structure, in contrast to its counterparts, deploys three- and five-input majority gates. It has a one layer structure and uses the robust and coplanar crossover scheme in [23]. It also uses the QCA clocking rule in [24-25] to achieve robust three-input majority gates against sneak noise paths. Further, the new full-adder is used to design highly efficient Reversible Ripple Carry Adders with different sizes.

TABLE I
The schematics of reversible full-adders in [39-54]

Ref	Reversible FA	Ref	Reversible FA

Ref	Reversible FA	Ref	Reversible FA
[39]		[40]	
[41]		[42]	
[43]		[44]	
[45]		[46]	

Ref	Reversible FA	Ref	Reversible FA
[47]		[48]	
[49]		[50]	
[51]		[52]	

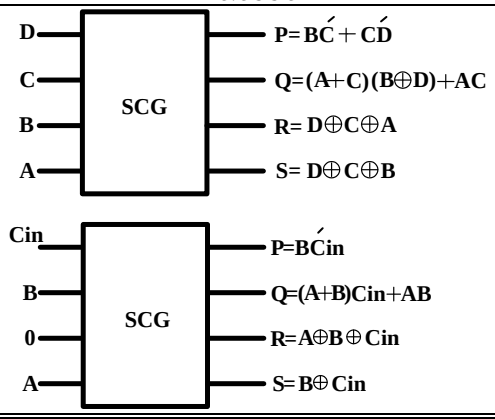
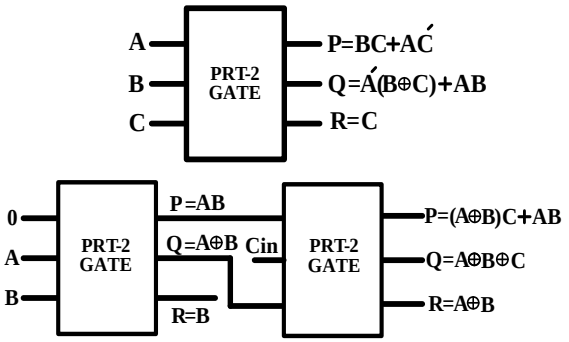
Ref	Reversible FA	Ref	Reversible FA
[53]		[54]	

TABLE II
THE QCA BASED REVERSIBLE FULL-ADDERS IN [55-56]

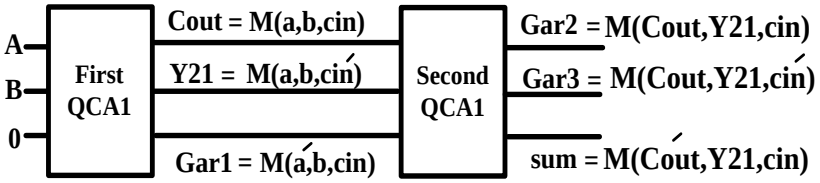
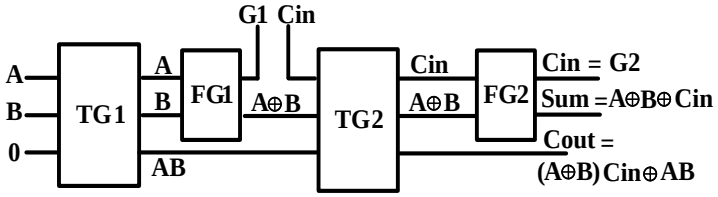
Ref	Reversible FA
[55]	
[56]	

TABLE III
A comparison of reversible full-adders in [39-56]

Reversible full-adder	Number of inputs/outputs	Number of garbage outputs	Number of three-input majority gates
[39]	5×5	3	19
[40]	4×4	2	14
[41]	5×5	3	40
[42]	4×4	2	15
[43]	4×4	2	15
[44]	4×4	2	15
[45]	4×4	2	24
[46]	4×4	2	14
[47]	4×4	2	15
[48]	4×4	2	14
[49]	4×4	2	15
[50]	4×4	2	14
[51]	4×4	2	14
[52]	4×4	2	14
[53]	4×4	2	19
[54]	4×4	2	18
[55]	4×4	2	14
[56]	3×5	3	6

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4. New QCA Reversible Full-Adder

Various designs for QCA and reversible QCA full-adders have been proposed to improve robustness, complexity, area and delay in QCA-based arithmetic and logic circuitry [5-8, 55-56]. Here, we propose a novel reversible gate, which deploys a five-input majority gate as proposed in one of our previous works on QCA full-adder (Fig. 3) [8]. This design is aimed at advancing previous reversible QCA designs to reach very high efficiency.

Fig. 4 presents the schematic of the proposed novel reversible gate, which is composed of two other reversible gates *N1* and *N2*. The truth tables of these gates are shown in Tables IV and V, respectively. In the proposed gate, the inputs are presented as *A*, *B*, *Cin* and *D* while the outputs are shown as *O1*, *O2*, *G1* and *G2*. In this design, if the input *D* is set to zero (as presented in Fig. 5), the proposed gate acts as a reversible full-adder gate. In this case, as shown in Table VI, the outputs *O1* and *O2* are used to transfer the *sum* and *carry* value of the reversible full-adder, while *G1* and *G2* are the two garbage outputs.

Fig. 6 presents the QCA layout of the proposed reversible design which uses the five-input majority gate layout in [9]. As demonstrated in this figure, in order to achieve a robust structure against sneak noise paths [24-25] three clocking zones with a 90^0 phase delay are used in each of the three-input majority gates. Also, this layout uses the robust coplanar crossover scheme in [23] to achieve a one layer and robust structure. This results in a reliable and efficient design. In the next section the proposed design's functionality is firstly verified and then it is compared against previous designs. Next, it is used to design 4, 8 and 16-bit reversible Ripple Carry Adders.

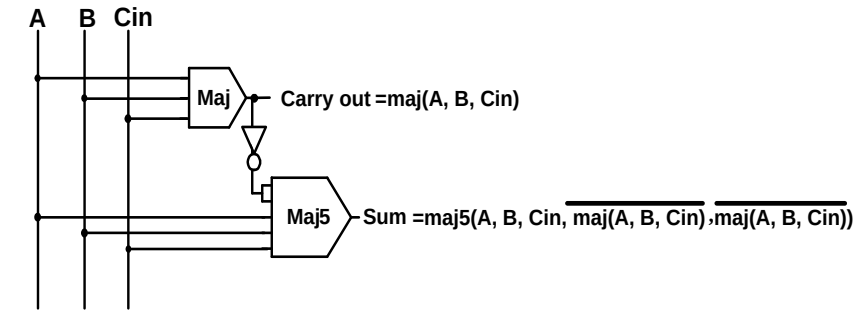

Fig. 3. The schematic of the QCA full-adder constructed using three and five-input majority gates [8]

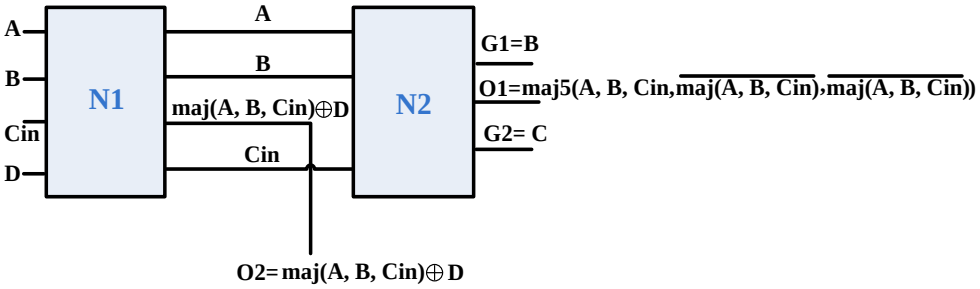

Fig. 4. The proposed reversible gate

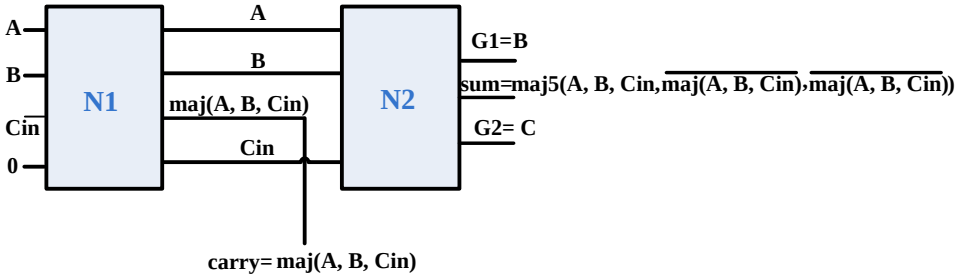

Fig. 5. The schematic of the new reversible full-adder based on Fig.4

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TABLE IV
The truth table of the new reversible gate N1 in Fig.4

inputs				*outputs*			
A	*B*	*C*	*D*	*B*	*A*	*XOR(Maj(A,B,C),D)*	*C*
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	0	1	0	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	0	0	1
1	1	0	0	1	1	1	0
1	1	0	1	1	1	0	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1

TABLE V
The truth table of the new reversible gate N2 in Fig.4

inputs			*outputs*		
A	*B*	*C*	*B*	$Maj(A,B,C,\overline{maj(A,B,C)},\overline{maj(A,B,C)})$	*C*
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	1	1	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	1	0	0	1
1	1	0	1	0	0
1	1	1	1	1	1

TABLE VI
The truth table of the proposed reversible full-adder (Fig.5)

inputs				*outputs*			
A	*B*	*C*	*D*	*G1=B*	*G2=C*	*O2*	*O1*
0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	1
0	1	0	0	1	0	0	1
0	1	1	0	1	1	1	0
1	0	0	0	0	0	0	1
1	0	1	0	0	1	1	0
1	1	0	0	1	0	1	0
1	1	1	0	1	1	1	1

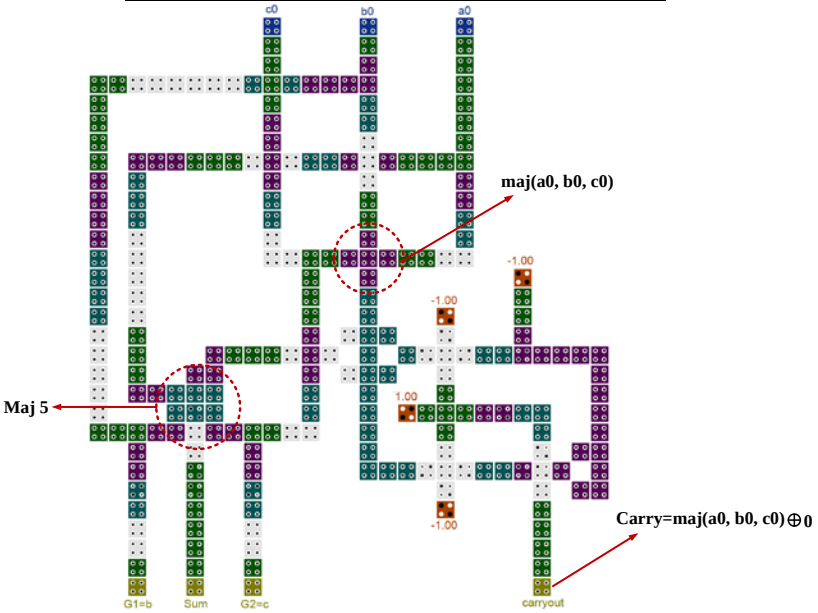

Fig. 6. The QCA layout of the new reversible full-adder in Fig.5

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5. Simulation and Comparison Results

In order to verify the functionality of the proposed design, it was simulated using both bi-stable and coherence vector simulation engines of QCA designer version 2.0.3. Same results were achieved using both simulation engines, which indicates the accuracy of the proposed design. Fig. 7 demonstrates the simulation results for the reversible full-adder design presented in Fig. 6, using the default parameters of both simulation engines. In this figure, based on the QCA layout of the new design, the outputs are valid after the fourth falling edge of clock0.

In order to compare the proposed design to the best previous reversible full-adders [39-54] and to previous QCA reversible full-adders [55-56], we first required to redesign these full-adders, using the same robust methodology that we utilized for our proposed design. The previous QCA reversible full-adders [55-56] are implemented using the multi-layer crossover scheme and without considering the required clocking rule that is required to achieve a robust three-input majority gate [24-25]. As mentioned earlier, since the required technology for implementing the multi-layer wire crossing has not yet been introduced, the robust coplanar crossover scheme in [23] is used in all redesigned reversible structures. Besides, in all these designs, the QCA clocking rule in [24-25] (presented in Fig.1 (c)) is used to achieve robust structures against sneak noise paths.

The number of majority gates has a direct relationship with the complexity (the number of cells) of the design. In addition, wire crossings are usually the source of uncertainties in QCA logic, so careful wire crossing is essential. Furthermore, cell arrangement plays an essential role in the total occupied area of any QCA circuit. Hence, the required number of majority gates, the needed wire crossings, and the cell arrangements were considered as the key factors of their suitability for implementing in QCA, when selecting the best previous reversible full-adders.

The selected reversible full-adders ([42], [46], [50] and [54]) were then designed in QCA using the robust coplanar crossover and with considering the required clocking rule for a three-input majority gate.

As shown in Table III, the reversible full-adder in [56] is the best previous structure in terms of the required number of three-input majority gates. The redesigned layout of this full-adder using the aforementioned robust methodology is shown in Fig. 8. Table VII presents the comparison of our new reversible full-adder (Fig. 6) and the QCA layouts of the full-adders presented in [42, 46, 50, 54-56] in terms of area, delay and complexity. According to this comparison, the proposed reversible full-adder achieves the improvement ratios of 31%, 22% and 3% compared to [56] in terms of area, complexity, and delay, respectively. Furthermore, as shown in Table VIII, the proposed design surpasses the best previous reversible design in terms of the number of inputs/outputs, the number of majority gates, and the number of garbage outputs.

The proposed efficient reversible full-adder is used to design high performance reversible Ripple Carry Adders (RCAs) with different sizes (i.e. 4, 8 and 16 bits). Fig. 9 shows the structure of the n-bit reversible Ripple Carry Adder constructed using the proposed design. The QCA layouts of the 16 bit reversible RCAs constructed using the proposed design (Fig. 6) and its best counterpart (Fig. 8) are also demonstrated in Fig. 10 and Fig. 11, respectively. Table IX presents a detailed comparison of RCAs in terms of area, delay, complexity and the number of garbage outputs. Based on these results, the new RCAs achieve significant improvements in terms of the optimization metrics. The 16 bit RCA constructed using the proposed reversible full-adder achieves the improvement ratios of 54%, 24% and 6% compared to the redesigned layout of [56] in terms of area, complexity, and delay, respectively. Based on this comparison, the proposed reversible full-adder can be used as an efficient component to design reversible arithmetic circuits.

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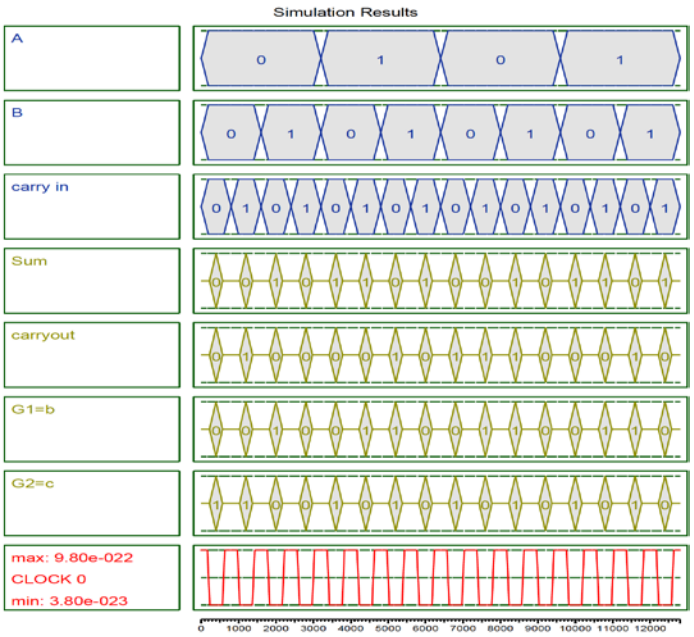

Fig. 7. The simulation results of the proposed QCA reversible full-adder in Fig.6

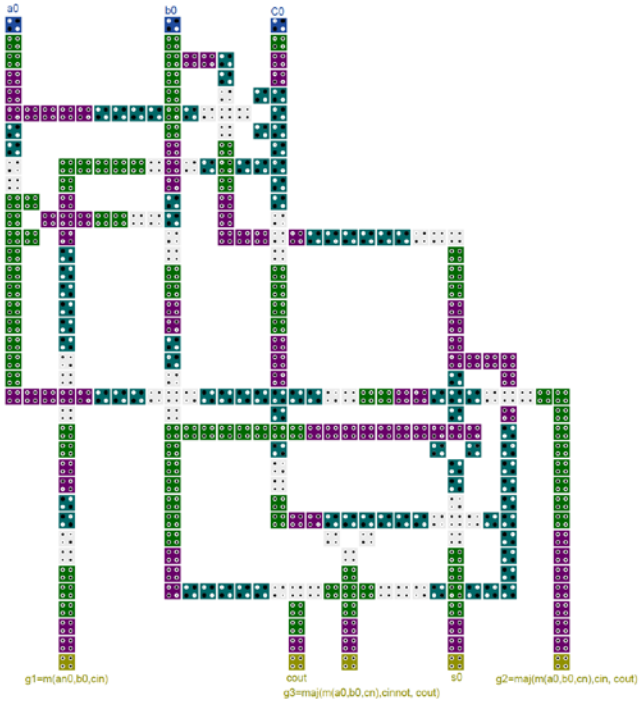

Fig. 8. The QCA layout of redesigned reversible full-adder of [56] with considering three-input majority gate clocking rule [24-25] and using the robust and one layer crossing scheme [23].

TABLE VII
A comparison of new reversible full-adder and redesigned structures

Reversible Full-Adder	area (μm^2)	cell count (complexity)	delay (clock cycle)
[42]	1.32	744	7.75
[46]	0.69	510	5
[50]	0.72	561	5
[54]	1.06	770	7.5
[55]	0.84	484	5
[56]	0.47	305	3.2
New reversible FA in Fig. 6	0.32	236	3.1

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TABLE VIII
A comparison of the new reversible full-adder and the redesigned layout of ([56])

Reversible Full-Adder	Number of inputs/outputs	Number of three-input majority gates	Number of five-input majority gates	Number of garbage outputs
Redesigned reversible full-adder of [56] (Fig.8)	5×3	6	----	3
New design in Fig.6	4×4	4	1	2

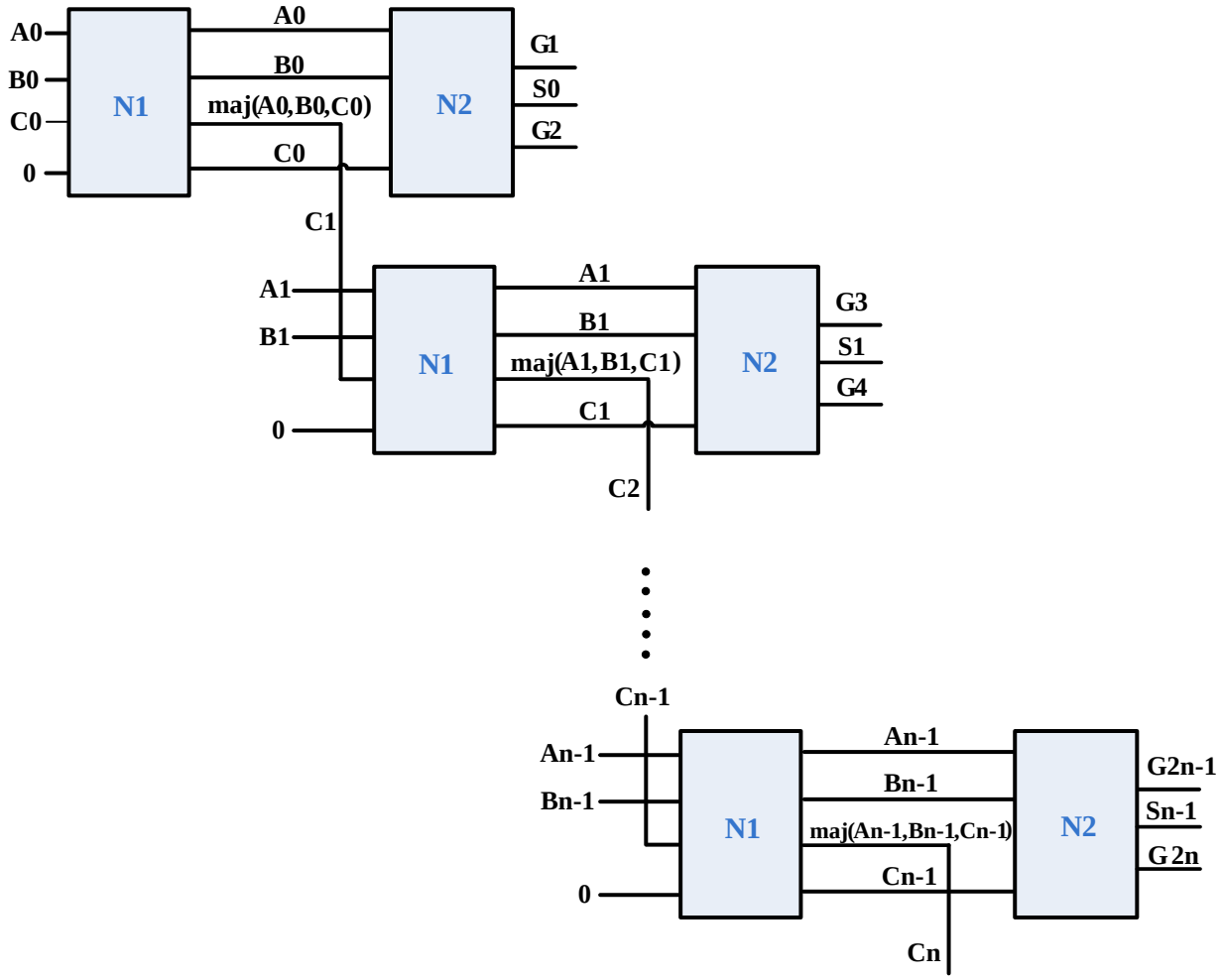

Fig. 9. The schematic of the n-bit reversible Ripple Carry Adder constructed using the new design in Fig. 6.

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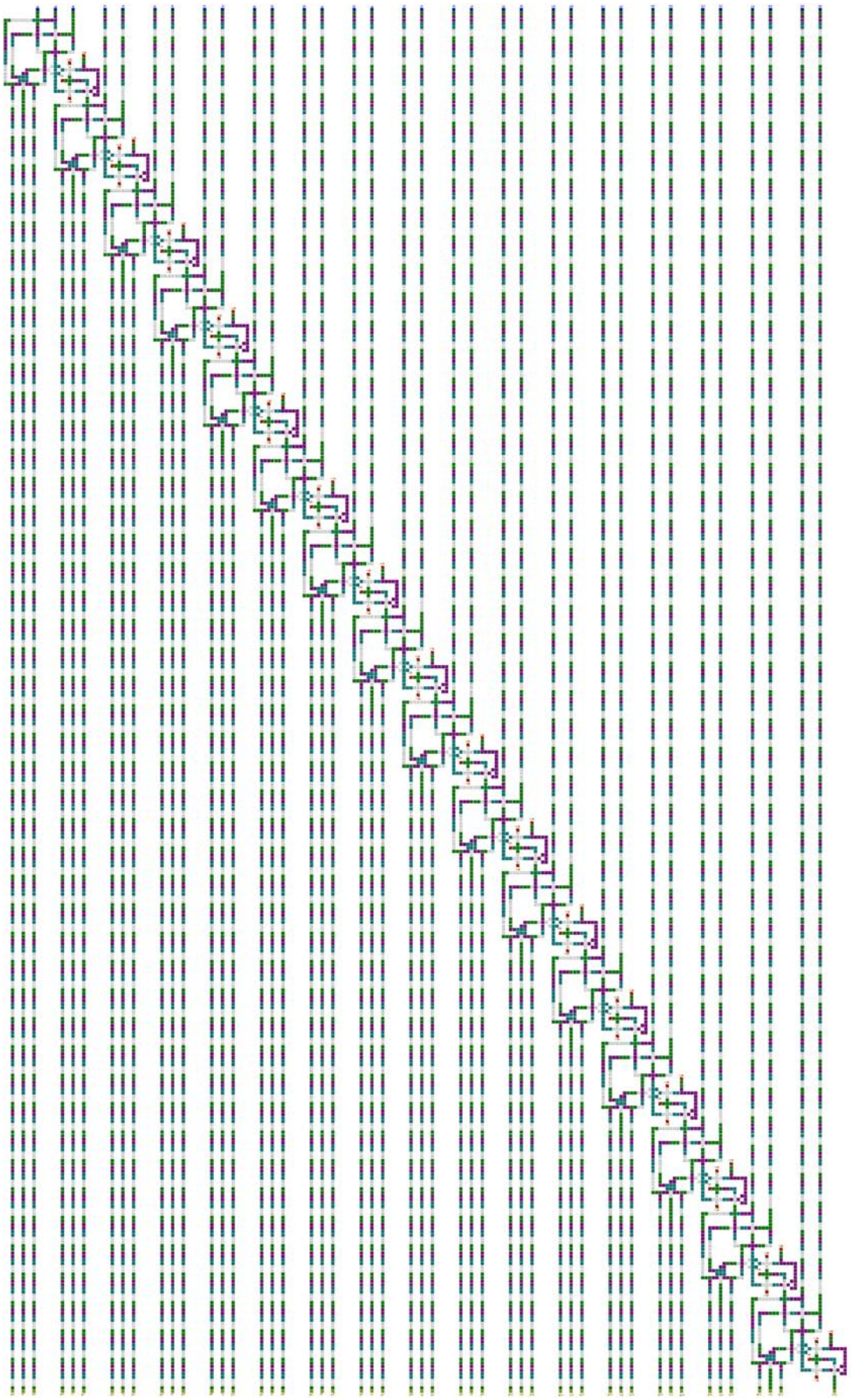

Fig. 10. The QCA layout of a 16 bit reversible Ripple Carry Adder constructed using the new design in Fig. 6.

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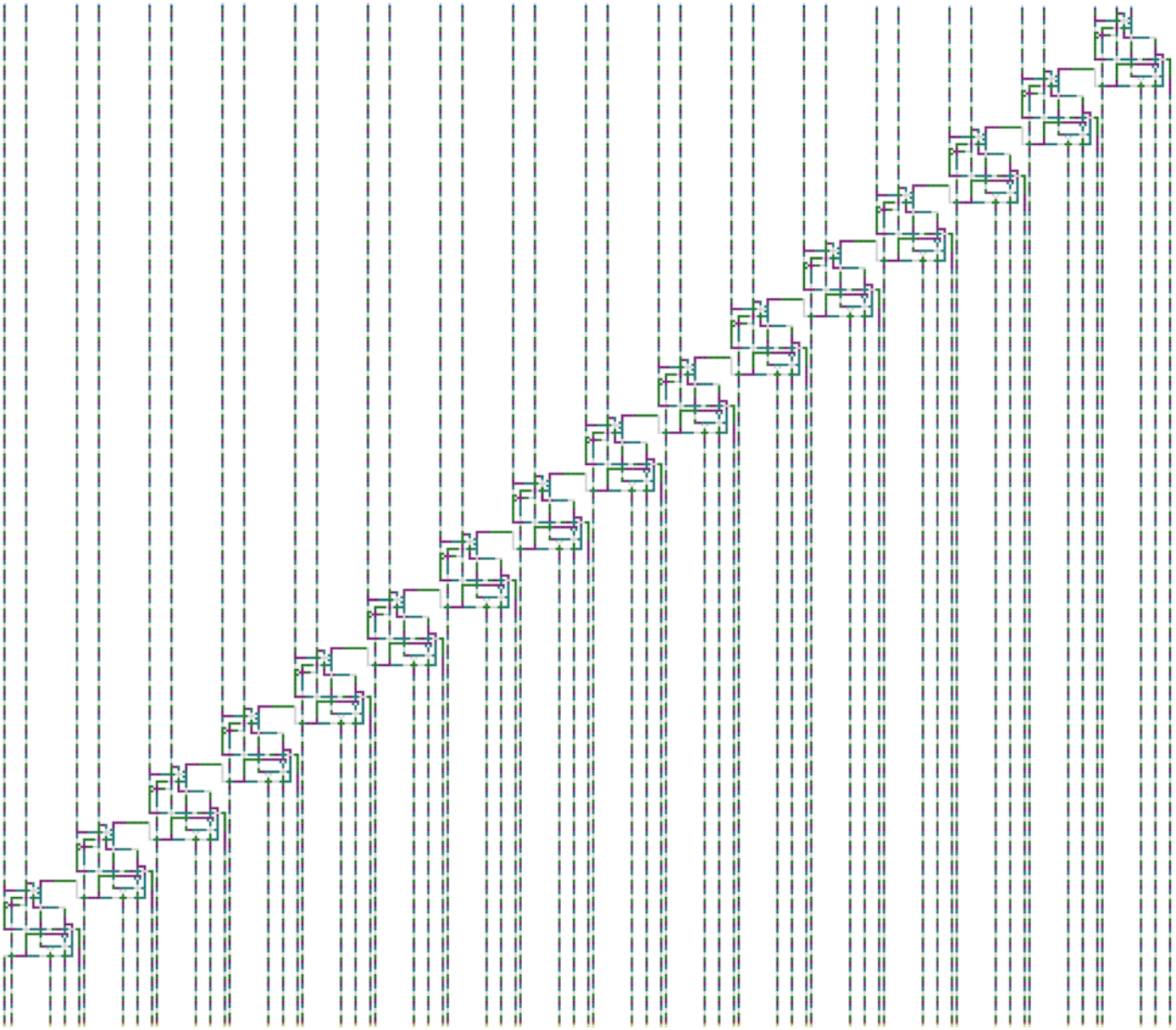

Fig. 11. The QCA layout of a 16 bit reversible Ripple Carry Adder constructed using the redesigned layout of [56].

TABLE IX
A comparison of RCAs constructed using the new reversible full-adder and redesigned layout of [56]

Reversible RCAs		Number of garbage outputs	area (μm^2)	cell count (complexity)	delay (clock cycle)
Redesigned layout of [56]	4 bit	12	6.45	2559	15.2
	8 bit	24	22.4	7425	27.2
	16 bit	48	82.85	24073	51.2
Proposed reversible FA	4 bit	8	2.81	1646	12.1
	8 bit	16	9.94	5206	24.1
	16 bit	32	37.74	18134	48.1

6. Conclusion

A novel reversible full-adder in QCA, which is optimized in terms of the number of garbage outputs, area, delay, and complexity, is introduced. It has a one-layer layout and uses a robust crossover scheme. It also utilizes reliable three-input majority gates to achieve a forceful structure against sneak noise paths. We have demonstrated designing reversible Ripple Carry Adders based on the proposed new design.

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Simulation results using both bi-stable and coherence vector simulation engines of QCAdesigner indicate the accuracy and efficiency of the proposed designs. These designs, surpass the RCAs constructed using the best previous designs in terms of the number of garbage outputs, area, delay, and complexity. The new design, therefore, can improve the implementation of reversible QCA-based devices and computers.

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