Active Capacitor Multiplier in Miller-Compensated Circuits

Author:

Gabriel A. Rincon-Mora
Power Management Products
Texas Instruments Incorporated
8505 Forest Lane, MS 8700
Dallas, Texas 75243
E-mail: rincon-mora@ti.com
Ph: (972) 480-2135
FAX: (972) 480-2264

Abstract

A technique is presented whereby the compensating capacitor of an internally compensated linear regulator, Miller-compensated two-stage amplifier, is effectively multiplied. Increasing the capacitance with a current-mode multiplier allows the circuit to occupy less silicon area and to more effectively drive capacitive loads. Reducing physical area requirements while producing the same or perhaps better performance is especially useful in complex systems where most, if not all, functions are integrated onto a single IC. Die area in such systems is a luxury. The increasing demand for mobile battery-operated devices is a driving force towards higher integration. The enhanced Miller-compensation technique developed in this paper helps enable higher integration while being readily applicable to any process technology, be it CMOS, bipolar, or biCMOS. Furthermore, the technique

applies, in general, to amplifier circuits in feedback configuration. Experimentally, the integrated linear regulator (fabricated in a 1 μm biCMOS process technolgoy) proved to be stable for a wide variety of loading conditions: load currents of up to 200 mA, Equivalent Series Resistance (ESR) of up to 3 Ω, and load capacitors ranging from 1.5 nF to 20 μF. The total quiescent current flowing through the regulator was less than 30 μA during zero load-current conditions.

Active Capacitor Multiplier in Miller-Compensated Circuits

Gabriel Alfonso Rincon-Mora

Texas Instruments Incorporated

Dallas, Texas 75243

I. Introduction

A popular technique for compensating amplifier feedback circuits is the use of the Miller capacitor. The poles of a two-stage amplifier are split, one towards low frequencies and the other towards high frequencies, when this configuration is adopted. The pole at the output of the first stage becomes dominant. Figure 1 illustrates a typical two-stage amplifier circuit model. Transconductors g_1 and g_2 are assumed to be ideal (infinite input and output impedance), resistors r_1 and r_2 model the effective impedance to ground at their corresponding nodes, and C_L and C_c are the load capacitor and the compensating capacitor, respectively. The dominant low frequency pole is located at node n1 (P_{n1}) and is defined by

$$P_{n1} \approx \frac{1}{2\pi r_1 (A_2 C_c)} \approx \frac{1}{2\pi r_1 (g_2 r_2 C_c)}, \qquad (1)$$

where A_2 refers to the gain of the second stage. The non-dominant pole is located at the output. At high frequencies, capacitor C_c shunts the output to node n1 thereby making the output transistor look like a diode-connected device, in other words, look like a $1/g_2$ resistor. As a result, the output pole is effectively moved towards higher frequencies,

$$P_o \approx \frac{g_2}{2\pi C_L} \ . \qquad (2)$$

These two poles must be separated sufficiently to guarantee some phase margin, as dictated by Nyquist criterion [1]. The corresponding Unity-Gain Frequency (UGF) or Gain-BandWidth (GBW) product of the model presented is

$$GBW = \frac{g_1}{2\pi C_c} \ , \qquad (3)$$

assuming that pole P_o lies in the vicinity of the UGF or at higher frequencies. A Right-Hand Plane (RHP) zero also results in the topology described ($Z_{RHP} \approx 1 / 2\pi g_2 C_c$). This zero exists because capacitor C_c provides a non-inverting feed-forward path, which becomes significant at high frequencies. At low frequencies, the feed-forward contribution of C_c is negligible relative to the inverted signal provided by the transconductor of the second stage ($-g_2$). A resistor in series with C_c is typically used to cancel the zero and even used to pull the zero into the Left-Hand Plane (LHP) [2].

Integrated capacitors, unfortunately, occupy significant physical space relative to other components like CMOS transistors. This characteristic is even more critical in single Integrated Circuit (IC) solutions where compactness is intrinsic and die real estate is scarce. Higher levels of integration tends to yield better frequency performance as a result of a reduction in parasitic components, i.e., bondwire inductance/impedance [3]. For the same reason and others, the direction of process technology is towards higher packing densities [4]. A limitation of typical Miller-compensated and other linearly compensated circuits is silicon area; large capacitors

needed for stability purposes occupy substantial space. As such, a tradeoff between cost (area) and performance exists in most amplifier circuits. Minimizing the size of these compensating capacitors (i.e., C_c in Figure 1) without sacrificing performance alleviates the tradeoff thereby maximizing profit. The technique proposed takes advantage of the minimal area requirements of active components to further multiply the effect of capacitor C_c (already multiplied by the Miller effect). Most of the active devices used to multiply this effective capacitance are already present in most amplifier circuits. In the end, the area required by a given amplifier circuit is considerably reduced by the capacitor multiplying technique presented.

The theory behind the proposed method is presented in section II. In it, voltage-mode and current-mode capacitor multipliers are introduced to ultimately develop the enhanced-Miller compensated circuit. The theory established is then used to develop a practical circuit in section III, a linear regulator. The functionality of the regulator is described and the tradeoffs of implementing the multiplied-Miller capacitor are discussed. Experimental measurements and results are offered in section IV. Finally, a recapitulation of the subject matter is given in section V.

II. Proposed Technique

2.1 Capacitor Multipliers

The Miller effect results because the equivalent capacitance seen at the output of the first stage is a multiplied factor of capacitor C_c, which is connected between the input and the output of the second gain stage. The circuit essentially adopts a voltage-mode capacitor multiplier technique to achieve this result. Figure 2 (a) illustrates the components that allow the technique to work properly; Figure 1 is the circuit realization of the same system. The equivalent

capacitance to ground at node n1 is derived from the displacement current flowing through capacitor C_c. This current is

$$I_c \equiv \Delta V_c SC_c = (V_{n1} - V_o)SC_c = V_{n1}(1 + A_2)SC_c \ , \tag{4}$$

where ΔV_c is the voltage across the capacitor ($I_c \equiv V_c / Z_c$, where Z_c is the impedance of the capacitor). As a result, the equivalent capacitance to ground (C_{eq}) is

$$C_{eq} \equiv \frac{I_c}{SV_{n1}} = (1 + A_2)C_c \ . \tag{5}$$

As noted in the equations, the effective load capacitance of the first stage is capacitor C_c multiplied by the voltage gain across the second stage.

Figure 2 (b), on the other hand, illustrates the principle behind the current-mode counterpart of the multiplier. The gist of the concept is to sense the current flowing through the capacitor, multiply it by a factor greater than one ($k_x > 1$), and reapply it back to the same node by means of a current-controlled current source. The amplification may be realized through current mirrors. The current through the capacitor is $V_{n1}C_cS$ and the equivalent capacitance seen at node n1 is therefore

$$C_{eq} \equiv \frac{I_{ceq}}{SV_{n1}} = \frac{I_c + k_x I_c}{SV_{n1}} = \frac{I_c(1 + k_x)}{SV_{n1}} = (1 + k_x)C_c \ . \tag{6}$$

Figure 3 shows a practical circuit of the current-mode capacitor multiplier described in Figure 2 (b). Transistor mp1 is added to illustrate how the circuit is used within the context of a gain stage. The current through capacitor C_c is sensed by transistor mn1. Transistor mn2 pulls an amplified version of the current from node n1. In a steady-state condition, mn2 sinks the current required to bias mp1 (dc current equal to k_xI_b). During a transient condition, however, the current flowing through capacitor C_c is summed with current I_b and therefore sensed and ultimately multiplied by k_x. Transistor mn1, while sensing the current, loads capacitor C_c with a diode-connected NMOS transistor, effectively a series $1/g_{mn1}$ resistor. Multiplier k_x, with respect to the capacitor current, is frequency dependent, as a result, thereby affecting the frequency response of the equivalent capacitance. This dependence is ascertained by deriving the relation for current I_c and substituting it back in the last equation derived for equivalent capacitance C_{eq},

$$C_{eq} = \frac{I_c(1 + k_x)}{sV_{n1}} = \frac{(V_{n1} - V_y)sC_c(1 + k_x)}{sV_{n1}} , \tag{7}$$

where V_y is the voltage at the gates of mn1 and mn2,

$$V_y = \frac{V_{n1}}{\left(\frac{1}{g_{mn1}} + \frac{1}{sC_c}\right)} \cdot \frac{1}{g_{mn1}} = \frac{V_{n1}sC_c}{sC_c + g_{mn1}} , \tag{8}$$

thus

$$C_{eq} = \frac{V_{n1}\left(1 - \frac{sC_c}{sC_c + g_{mn1}}\right)sC_c(1 + k_x)}{sV_{n1}} = \frac{C_c(1 + k_x)}{\left(\frac{sC_c}{g_{mn1}} + 1\right)} . \tag{9}$$

In effect, a pole attenuates the amplification factor k_x. The frequency response of the circuit, as a whole, therefore becomes

$$\frac{V_{n1}}{V_{in}} = \frac{-g_{mp1}r_o}{(1+r_oSC_{eq})} = \frac{-g_{mp1}r_o}{\left[1+r_o\left(\frac{C_c(1+k_x)}{\frac{SC_c}{g_{mn1}}+1}\right)S\right]} \approx \frac{-g_{mp1}r_o\left(\frac{SC_c}{g_{mn1}}+1\right)}{[1+r_o(1+k_x)SC_c]}, \qquad (10)$$

where r_o is the equivalent impedance to ground at node n1, which is the parallel combination of $r_{ds\text{-}mn2}$ and $r_{ds\text{-}mp1}$. As can be observed, the attenuating pole of the multiplication factor introduces a LHP zero in the overall response. This zero lies at relatively high frequencies; however, it may be used to optimize frequency compensation. If designed to be near the second dominant pole (somewhere past the unity-gain frequency), it adds phase thereby mitigating the negative effects of the secondary pole and other parasitic poles possibly present in the same frequency band. The dominant pole, of course, is defined by a multiplied version of C_c and r_o, $1 / 2\pi k_x r_o C_c$. Placing the LHP zero right at the unity-gain frequency may degrade gain margin to intolerable levels though, which is not generally desired in the design of operational amplifiers unless it is used to cancel a specific pole.

2.2 Multiplied-Miller Capacitor

Complementing the already existing voltage-mode gain factor with a current-mode capacitor multiplier enhances the effects of the Miller capacitor. Figure 4 models such a circuit configuration. The equivalent capacitance to ground that results at node n1 is not only multiplied

by the Miller effect ($A_2 \approx g_2 r_2$) but by the current-mode multiplier (k_x). The difference between this topology and that of a typical Miller configuration (Figure 1) is that capacitor C_c is no longer connected to the output of the first stage directly. Instead, its current is sensed, multiplied by current mirrors, and reapplied to node n1 via a current-controlled current source. As before, the current flowing through C_c is

$$I_c \equiv -V_o SC_c = V_{n1} A_2 SC_c = V_{n1} g_2 r_2 SC_c \ , \tag{11}$$

thus

$$C_{eq} \equiv \frac{I_{ceq}}{SV_{n1}} = \frac{k_x I_c}{SV_{n1}} = k_x g_2 r_2 C_c \ ! \tag{12}$$

Gain factor A_2 refers to the gain across the second stage. The significance of this relation is that, given a particular design, the size of C_c required to properly compensate the circuit is k_x times smaller using the proposed approach than using the standard Miller-compensation technique. The resulting dominant pole and gain-bandwidth product are described by

$$P_{n1} \approx \frac{1}{2\pi r_1 (k_x g_2 r_2 C_c)} \tag{13}$$

and

$$GBW = \frac{g_1}{2\pi k_x C_c} \ . \tag{14}$$

In the end, gain factor k_x amplifies the effects of capacitor C_c. Furthermore, the RHP zero present in typical Miller-compensated circuits is no longer existent in the proposed topology because there is no feed-forward path around the inverting transconductor of the second stage.

III. Circuit Realization

A linear regulator is designed in a 1 μm biCMOS process to test the proposed technique. The regulator is a two-stage amplifier with a class "A" output stage. Most regulators have a dc open-loop gain of approximately 40 – 60 dB. Open-loop gain is limited to guarantee stability due to the harshness of the loading conditions, load-current range is large and output capacitor is high. Within a given application, the load current can vary from zero to anywhere above 100 mA. As a result, the output pole varies with load current (output impedance is a function of load current). Furthermore, typical load capacitors range from 1 to 20 μF thereby pulling the output pole to low frequencies.

The output stage of the regulator is a P-type common-source class "A" gain stage. This choice results because the load only demands the IC to drive and not sink significant amounts of current. Figure 5 shows the simplified version of the schematic using a folded-cascode architecture as the first gain stage. Compensation is realized by combining the circuits shown in Figures 3 and 4. Capacitor C_c is connected from the output to a diode-connected transistor, mn22a. This transistor is used to bias the amplifier in steady-state conditions (when the capacitor current is zero) and is also used to sense the displacement current flowing through capacitor C_c. The ac current is thusly mirrored and injected back into high impedance node n_31 by means of transistors mn22b, mn22, mp22, and mp21. Node n_31 is the output of the first

gain stage (equivalent to node n1 in Figure 4). Transistor mn32 is a natural NMOS transistor. Its low threshold voltage (approximately 0 V) prevents mp22 from being crushed.

A buffer is used between the first and the second stage to drive the gate of the large output PMOS device. A weak drive delays the response time during fast transient load-current changes. The buffer, shown in detail in Figure 6, senses the load current by mirroring a fraction of it through transistor mpox. This mirrored current is ultimately used to define the location of the parasitic pole at the gate of power PMOS mpo. For high power efficiency and stability, its location must be a function of the load. Like before, transistor mn31 is a natural NMOS device. Its low threshold voltage allows the feedback circuit to effectively shut-off, when required, the PMOS pass device. Bulk effects can be cancelled if a deep n+ trench diffusion and a buried n+ layer are available to isolate the natural device (isolate a p-epi region in which a natural device can be built). The buffer and its benefits are described in [5]. Capacitor C_{c2} along with readily available components in the amplifier are used to realize the circuit of Figure 3. As a result, node n_31 is further loaded with an equivalent capacitor equal to a multiplied version of C_{c2}. This capacitor is used to compensate the high frequency feedback path through C_c, mn21b, mn22, mp22, mp21, buffer, and mpo. This high frequency path has two main poles: one at the output and one at node n_31. Capacitor C_{c2} makes node n_31 dominant at high frequencies.

Careful layout is exercised to maximize the matching capabilities of mn21a, mn21b, mn22a, mn22b, and their corresponding current sources. Input offset performance is sensitive to these devices since they all determine how well the currents through transistors mn22a and mn22b match. This characteristic is a disadvantage relative to standard Miller compensation where only mn22b and mn21b, of the group mentioned earlier, need to match well, i.e., a degradation of roughly 5 mV. Ultimately, more sources of input offset errors are significant in

the circuit when the proposed technique is utilized. The current gain k_x (chosen to be 10) is defined by the mirror ratio between mn21a and mn21b (mn22a and mn22b) and is therefore restricted by the physical constraints of the same. The tradeoff for matching is high gain; a large spread between the matching devices yields high gain and, unfortunately, poor matching characteristics and thus increased input offset voltages. On the positive side, the only additional components required to compensate the circuit are C_c, C_{c2}, mn22a, and mn21a. Transistors mn21a and mn22a are relatively small devices and capacitors C_c and C_{c2} are already minimized by the aforementioned technique.

Figure 7a shows the simulated open-loop response of the circuit without compensation, with standard Miller compensation (C_c = 20 pF), and with enhanced-Miller compensation (C_c = 2 pF and k_x = 10) under nominal conditions. As mentioned earlier, low loop gain is necessary in a regulator circuit because of the variability of the load, i.e., load current ranges two orders of magnitude, ESR may be zero or several Ohms, and the load capacitor can vary by 50 to 100 % with temperature and process. The nominal load of the simulation shown in Figure 7a consisted of a 0.1 µF capacitor to ground and a current sink of 10 mA. The ac response of the Miller and enhanced-Miller compensated circuits are almost identical. In fact, the standard version, using a C_c an order of magnitude larger, has less gain margin than the new version. This effect results because, like in Figure 3, a high frequency LHP zero is introduced by C_c and the transconductance of mn22a ($1/g_{mn22a}$), which adds phase near the vicinity of the unity-gain frequency. The circuit was stable up to a load capacitance of 21 µF and a load current of 220 mA over process and temperature. It was also stable with various values of Equivalent Series Resistance (ESR) for the load capacitor (Figure 7b). Typical ESR's can range up to several Ohms. High frequency capacitors, on the other hand, can exhibit ESR's of less than 0.5 Ω [6].

The phase-margin response of the circuit shown in Figure 7b (circuit under various harsh loading conditions) is degraded from that of Figure 7a because large load capacitors pull the output pole to lower frequencies and high load currents push the unity-gain frequency towards higher frequencies close to the location of other parasitic poles. Load capacitors for linear regulators normally range from 1 to 10 μF depending on the application and the particular design. The cumulative effect of ESR and the bondwire resistance is a LHP zero. Stability, for this design, is independent of ESR as is shown in Figure 7b. Without any ESR, the zero introduced by the bondwire resistance is in the MHz region, i.e., $1 / 2\pi$ (60 mΩ) 1 μF ~ 2.6 MHz, which helps keep phase margin but not significantly since it lies beyond the frequency range of interest.

IV. Experimental Results and Discussion

Figures 8 and 9 show the experimental performance of the circuit under rapid load-current changes. The load current is pulsed from zero to 200 mA and back down to zero with rise and fall times of less than 100 ns. Any susceptibility towards instability would result in oscillations under this test since the abrupt stimulus injects noise that spans a wide frequency spectrum [7]. Figure 8 shows the transient response when no additional ESR is added in series with the load capacitor (C_L). The only ESR present is inherent to the capacitors and is below 0.1 Ω. Figure 9 shows the same type of response except that a 3 Ω series resistor has been added as intentional ESR. Figures 8 (a) and 9 (a) show the full period response while 8 (b) and 9 (b) only show the negative transition, where oscillations are most prone to initiate. The total quiescent current of the circuit is less than 30 μA during zero load-current conditions.

The overshoot and the slow decay on the rising edge are a function of the load capacitor and its ESR. High capacitance and low ESR prevents the node from overshooting significantly. During the recovery from this positive overshoot, the output slews back down to its steady-state value. This part of the response occurs because the output of the circuit is a class "A" output stage with a small sink current determined by a resistive ladder (two 250 kΩ resistors). The falling edge, shown in Figures 8 (b) and 9 (b), has a different response because of the active pull-up transistor in the output stage. During this transition, the regulator initially stays off thereby allowing the full load to quickly discharge the output capacitor. Bandwidth and internal slew-rate conditions at the gate of the large PMOS pass device determine how long the regulator takes to start conducting current. Once it starts, the positive-feedback loop within the buffer helps speed up the process until the negative-feedback gain is large enough to take control again. Positive and negative overshoots occur during this period as a result.

It is evident that the regulator is stable with varying degrees of phase margin (depicted by the settling time response) for a variety of load-capacitor values (up to 20 μF) with and without additional ESR of up to 3 Ω. The response was the same for several devices subjected to the same tests. The circuit tends to be more stable with additional ESR. This results because ESR effectively adds a Left-Hand Plane (LHP) zero at $1 / 2\pi R_{ESR}C_L$ thereby adding phase between 1 and 60 kHz depending on the value of C_L. The zero is also inclined to push the unity-gain frequency towards higher frequencies thereby improving time response, in other words, decreasing the time required for the circuit to react. Resistor R_{ESR} also increases the peak overshoots because of the voltage drop created when capacitor C_L charges and discharges. Relatively low phase margin, rapid load pulses, and an internal positive feedback loop in the buffer account for the large positive and negative overshoots of the signals in Figure 8.

In conclusion, the circuit proved to be stable under a variety of loading conditions. Table 1 shows a summary of the performance parameters pertinent to the regulator. Load capacitor C_L needed to be at least 1.5 nF to prevent oscillations. Under the test setup utilized, the output transiently goes below ground when C_L is less than 1.5 nF. At this point, the load (an NPN power transistor) is saturated thereby interacting with the circuit and causing oscillations during recovery. The output is momentarily pulled to ground because capacitor C_L is quickly discharged by the load current during the time the IC takes to respond, while mpo is not sourcing any current. Most relevant applications require output capacitors of more than 10 nF anyway.

V. Conclusion

A linear regulator, which is essentially a two-stage amplifier, is designed and fabricated using a modified Miller-compensating scheme where an integrated capacitor is multiplied "actively," and in a controlled fashion, to compensate the circuit. A current-mode capacitor multiplier is used to enhance the voltage-mode multiplying effects of Miller compensation. The drawback, for the particular design in question, is deteriorated input offset voltage. This disadvantage is alleviated with careful design and layout. Furthermore, in high frequency applications, careful consideration must be given to the placement of the Left-Hand Plane (LHP) introduced by the circuit: a low LHP zero degrades gain margin. This zero is manipulated by controlling the transconductance of the diode-connected device, mn22a (adding more current decreases the impedance thereby pushing the zero to higher frequencies). Additionally, during a fast load transient event, the diode-connected device may turn-off temporarily thereby degrading overall recovery time. Placing an additional current source (gates are passively de-coupled or totally disconnected from the ones used by the technique) in parallel with mn21b and mn22b

mitigates this negative effect. Although the technique has been applied to a folded-cascode topology, the basic concept may be extended to other amplifier topologies. Simulations and experimental results confirm the validity of the concept. The fabricated IC proves to be stable for load currents of up to 200 mA, Equivalent Series Resistance (ESR) of up to 3 Ω, and load capacitors ranging from 1.5 nF to 21 μF. These results are achieved by using a significantly lower compensating capacitor than would have been used had the teachings of standard Miller compensation been adopted. The number of additional components required to compensate the circuit is minimal and its overhead, in terms of silicon area, is negligible. Mitigating silicon area requirements allows the circuit to be smaller thereby reducing overall cost. Furthermore, the technique applies to the compensation of feedback circuits in general, Miller or otherwise.

References

[1] A.S. Sedra and K.C. Smith, *Microelectronic Circuits*. New York: Holt, Rinehart and Winston, Inc., 1987.

[2] P.R. Gray and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: John Wiley & Sons, Inc., 1993.

[3] M. Ingels and M.S.J. Steyaert, "Design Strategies and Decoupling Techniques for Reducing the Effects of electrical Interference in Mixed-Mode IC's," *IEEE Journal of Solid-State Circuits*, Vol 32 # 7, pp. 1136-1141, July 1997.

[4] R. Cavin and W. Liu, *Emerging Technologies, Designing Low Power Digital Systems*. Piscataway, NJ: Institute of Electrical and Electronics Engineers, 1996.

[5] G.A. Rincon-Mora and P.E. Allen, "A Low Voltage, Low Quiescent Current, Low Drop-out Regulator," *IEEE Journal of Solid-State Circuits*, Vol 33, pp. 36-44, January 1998.

[6] M. Kay, "Design and Analysis of an LDO Voltage Regulator with a PMOS Power Device," Preliminary paper pending publication, Texas Instruments.

[7] B. C. Kuo, *Automatic Control Systems*. Englewood Cliffs, New Jersey: Prentice Hall, 1991.

Table 1. Performance summary.

	Measured Results
Line Regulation (V_{supply} = 3 – 8 V)	2 mV/V
Load Regulation (I_{Load} = 0 – 200 mA)	0.275 mV/mA
C_{Load}	1.5 nF to 20 µF
ESR	≤ 3 Ω
Quiescent Current (I_{Load} = 0 A)	≤ 30 µA
V_{supply}	1.25 to 8 V
$V_{input\text{-}referred\text{-}offset}$ (referred to $V_{bandgap}$)	±15 mV

Figure Captions

Figure 1. Two-stage Miller-compensated amplifier.

Figure 2. Voltage-mode and current-mode capacitor multipliers.

Figure 3. Current-mode capacitor multiplier in a practical gain-stage circuit.

Figure 4. Enhanced Miller-compensated two-stage amplifier.

Figure 5. Simplified schematic of the linear regulator using the enhanced-Miller technique.

Figure 6. Detailed schematic of the regulator.

Figure 7a. Simulated Bode plot of the proposed circuit without compensation, with standard Miller compensation, and with enhanced-Miller compensation under nominal conditions.

Figure 7b. Simulated Bode plot of the proposed circuit with enhanced-Miller compensation under various loading conditions.

Figure 8. Experimental transient response of the fabricated regulator with zero ESR: (a) load current is rapidly pulsed from zero to full range and back to zero and (b) load current is pulsed from zero to full range only.

Figure 9. Experimental transient response of the fabricated regulator with 3 Ω of ESR: (a) load current is rapidly pulsed from zero to full range and back to zero and (b) load current is pulsed from zero to full range only.

Figure 10. Die Plot.

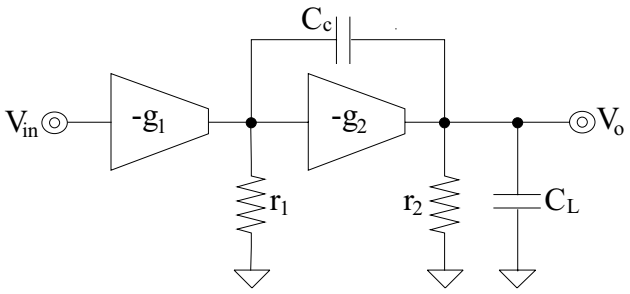

Figure 1. Two-stage Miller-compensated amplifier.

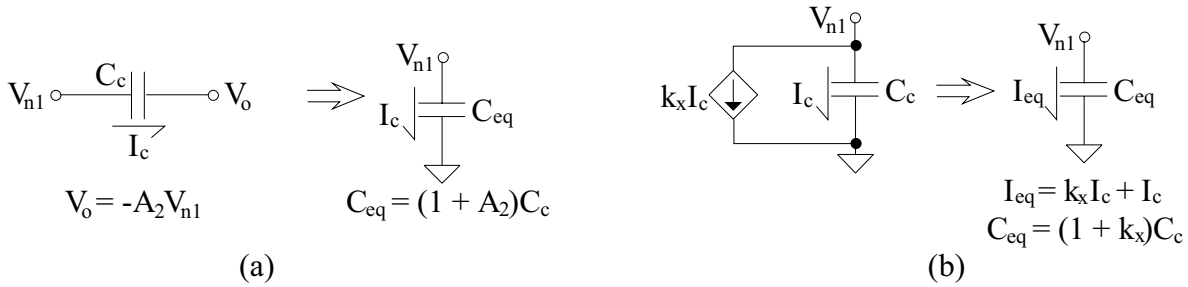

Figure 2. Voltage-mode and current-mode capacitor multipliers.

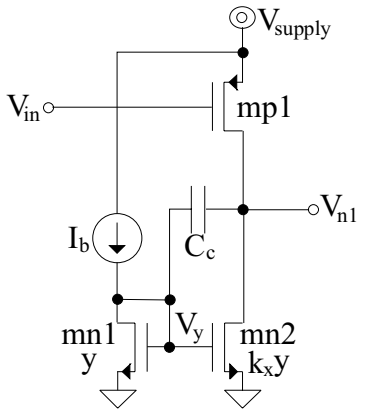

Figure 3. Current-mode capacitor multiplier in a practical gain-stage circuit.

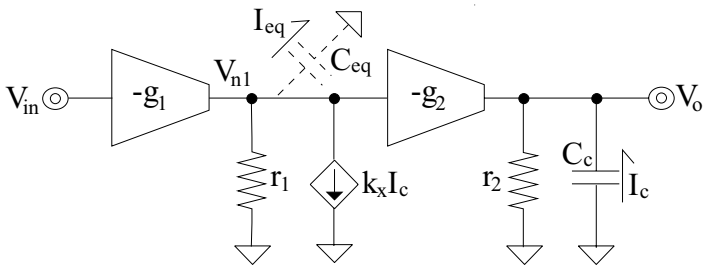

Figure 4. Enhanced Miller-compensated two-stage amplifier.

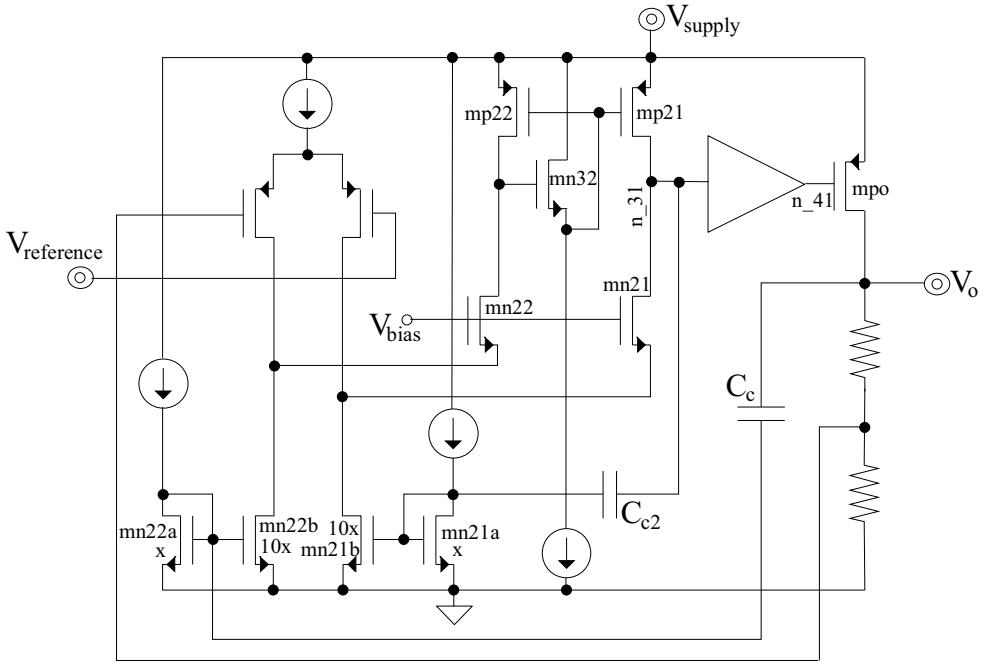

Figure 5. Simplified schematic of the linear regulator using the enhanced-Miller technique.

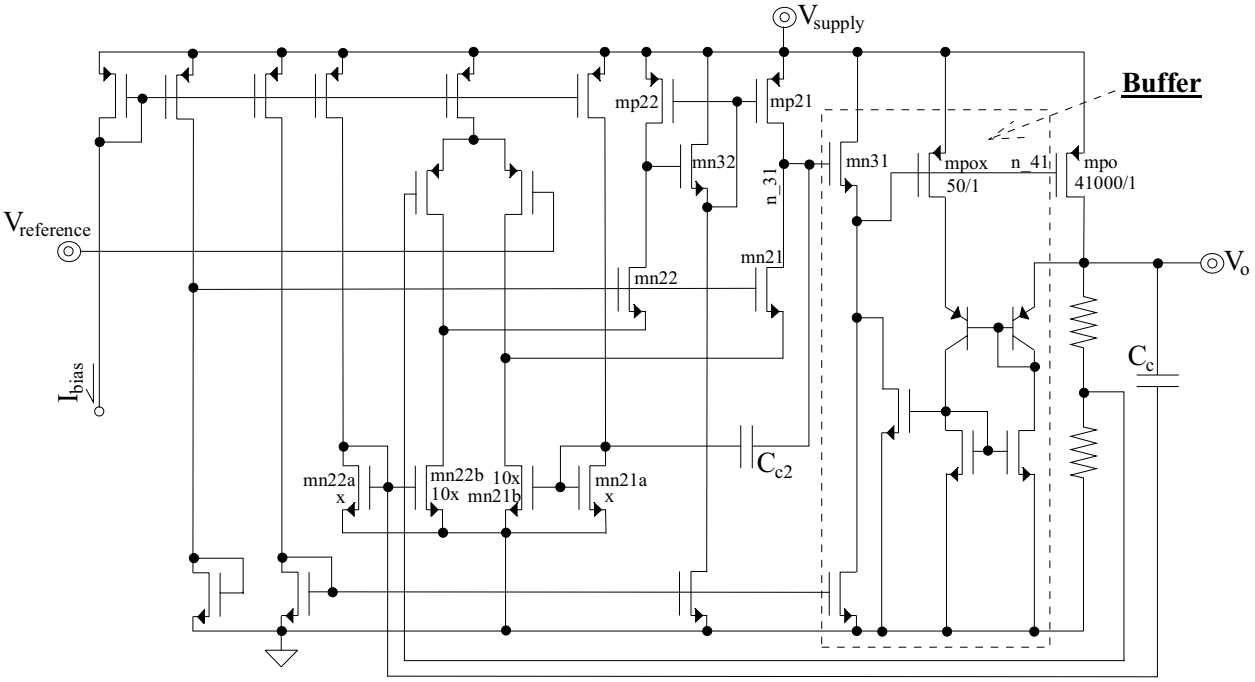

Figure 6. Detailed schematic of the regulator.

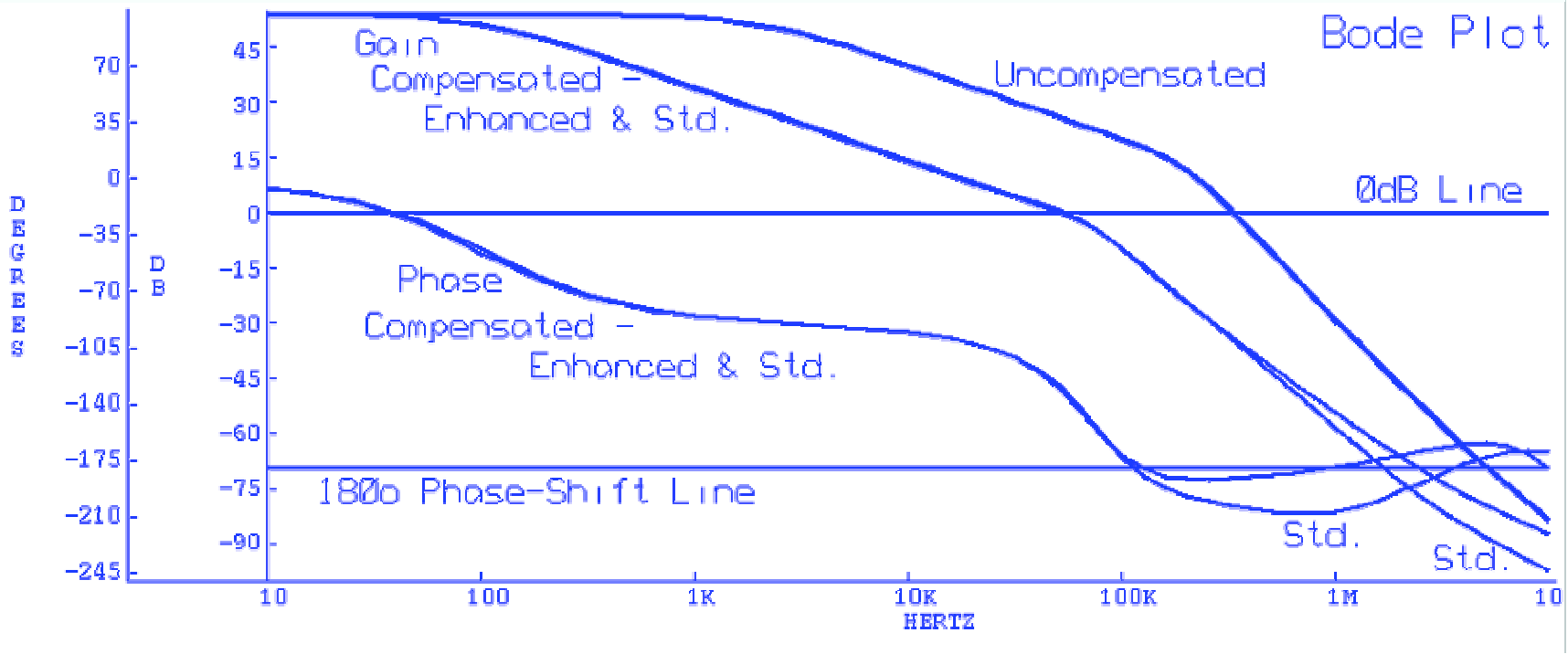

Figure 7a. Simulated Bode plot of the proposed circuit without compensation, with standard Miller compensation, and with enhanced-Miller compensation under nominal conditions.

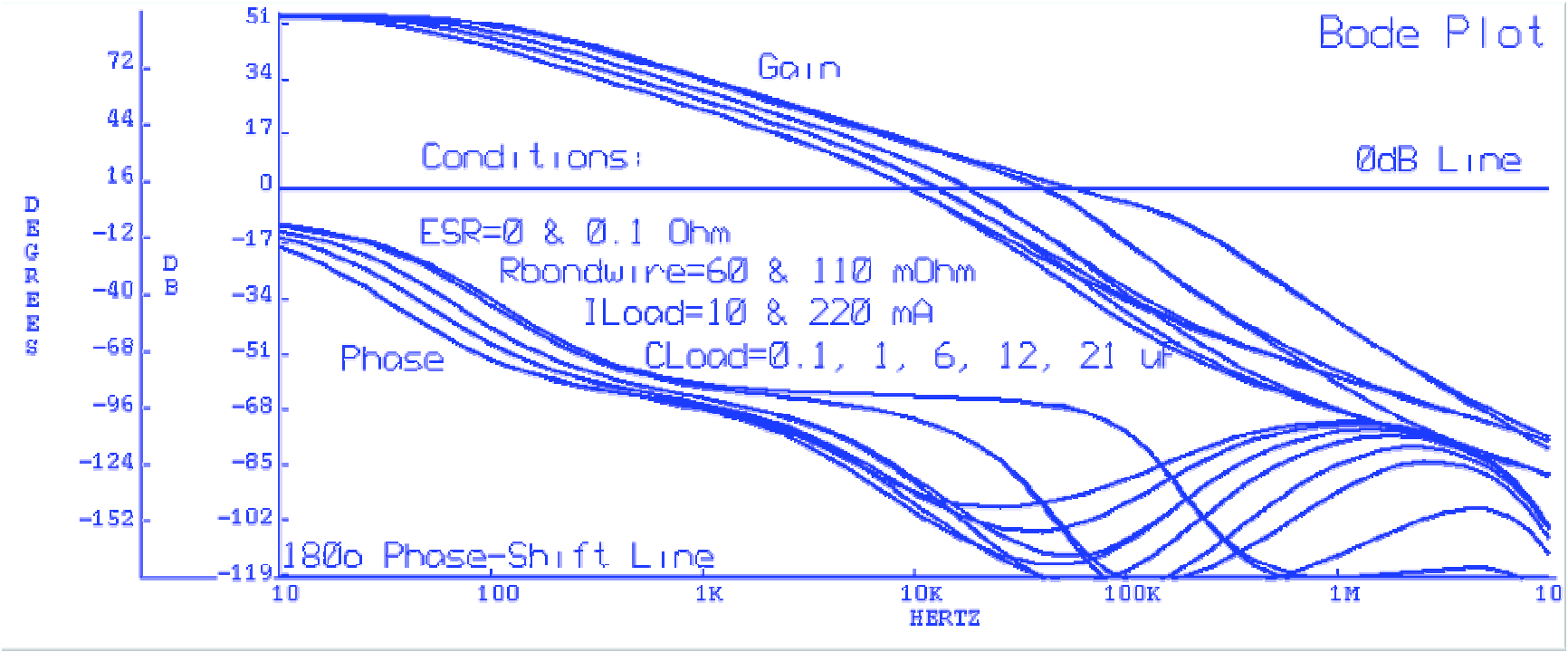

Figure 7b. Simulated Bode plot of the proposed circuit with enhanced-Miller compensation under various loading conditions.

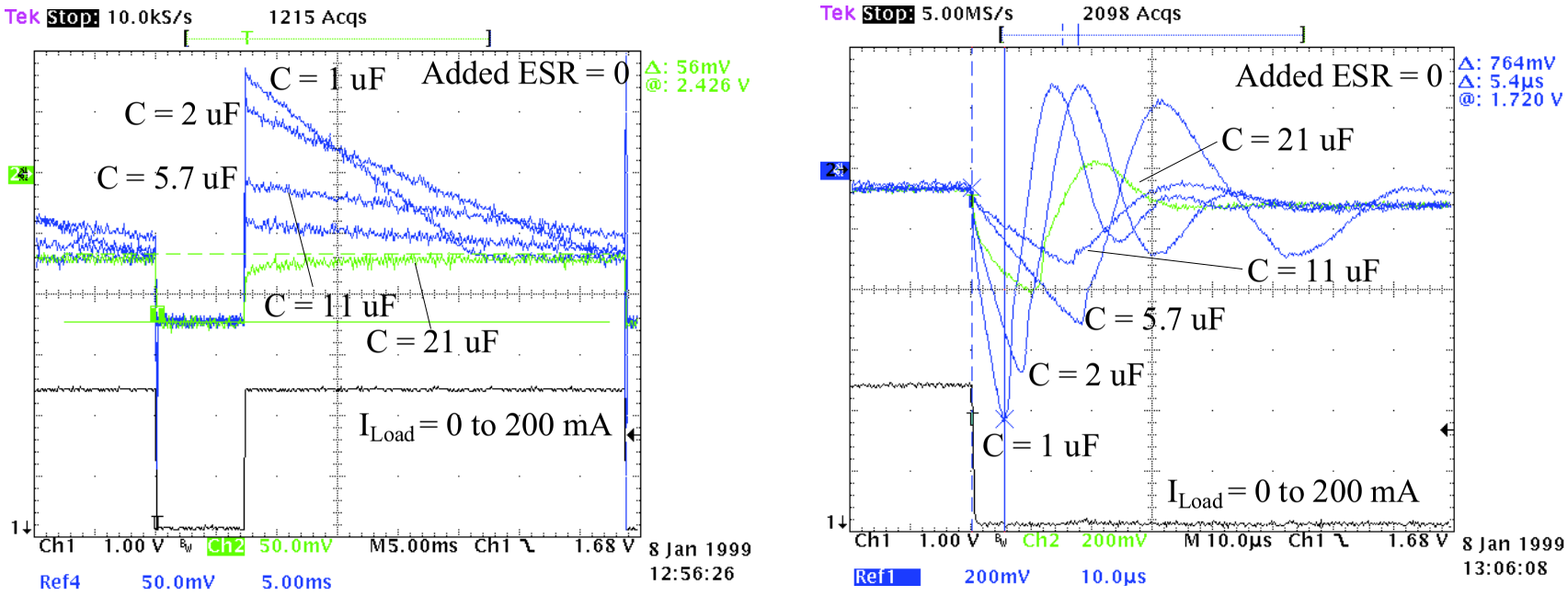

Figure 8. Experimental transient response of the fabricated regulator with zero ESR: (a) load current is rapidly pulsed from zero to full range and back to zero and (b) load current is pulsed from zero to full range only.

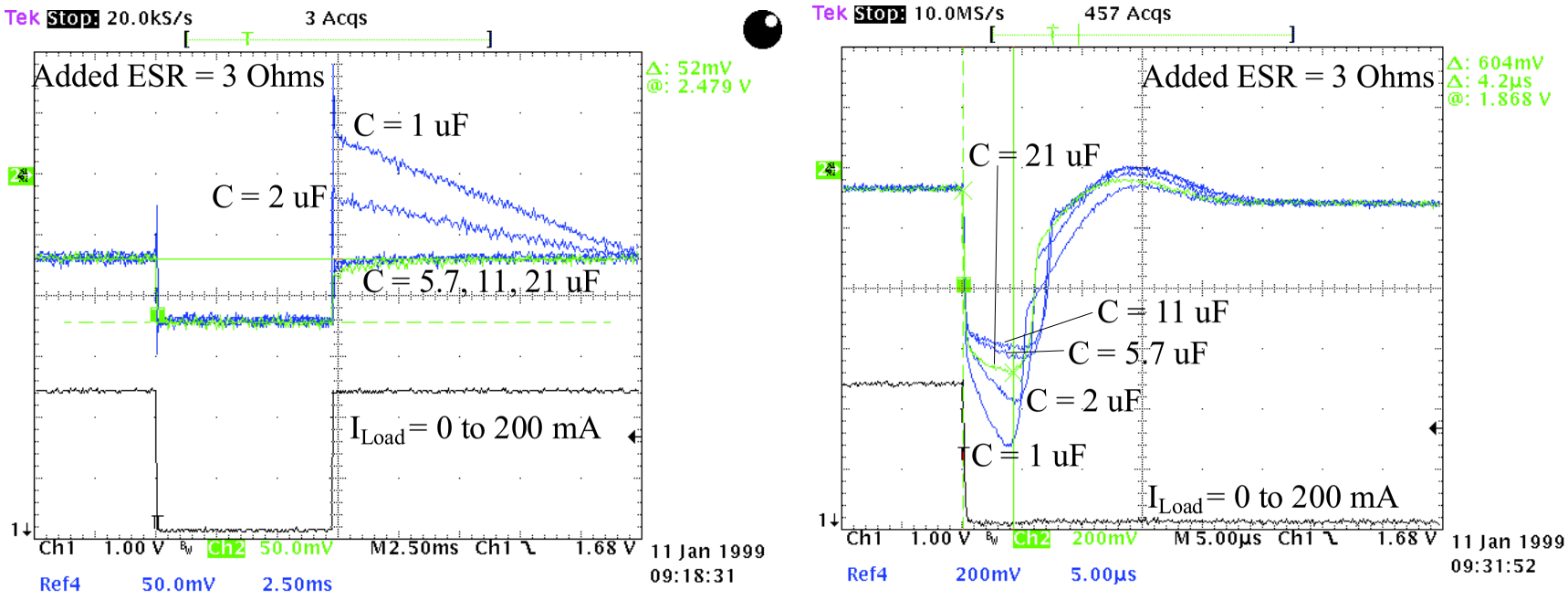

Figure 9. Experimental transient response of the fabricated regulator with 3 Ω of ESR: (a) load current is rapidly pulsed from zero to full range and back to zero and (b) load current is pulsed from zero to full range only.

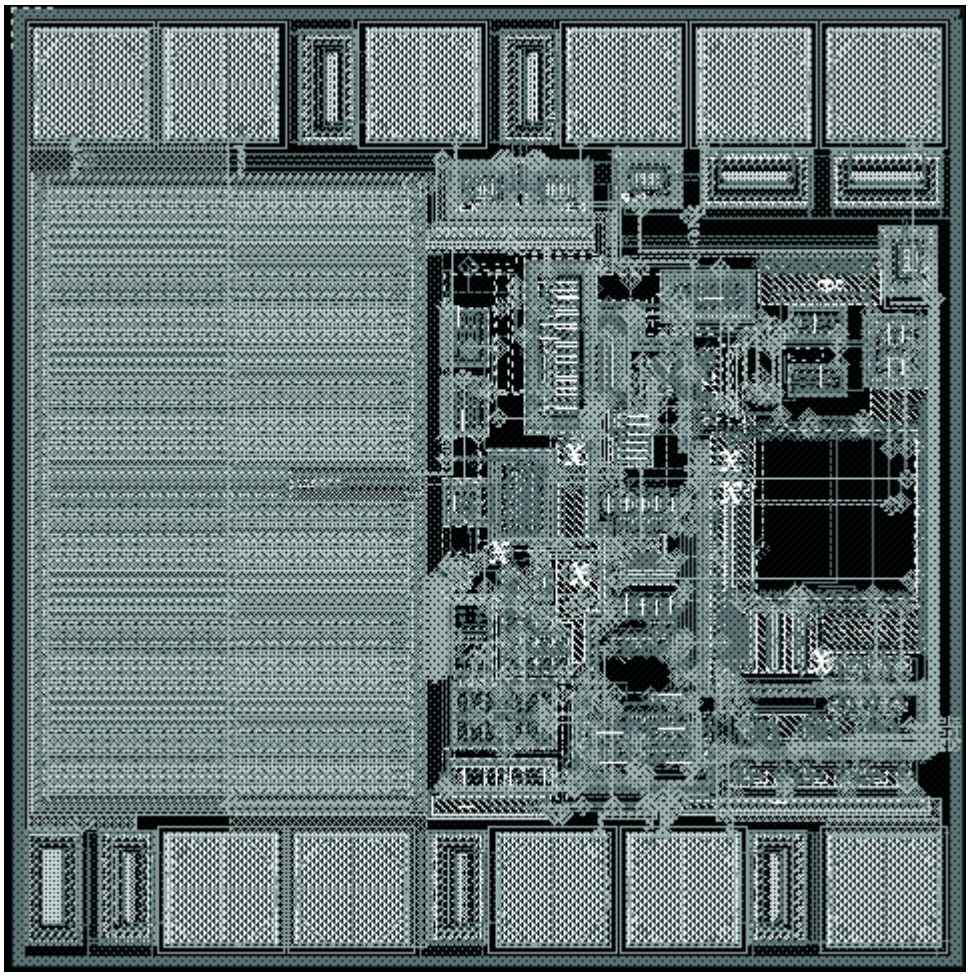

Figure 10. Die Plot.