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· Supplementary File ·

A novel multi-threshold coupling InAlN/GaN double-channel HEMT for improving transconductance flatness

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Appendix A Device fabrication

The structure of the novel multi-threshold coupling InAlN/GaN double-channel HEMTs (MC-DC HEMT) investigated in this article is shown in Figure A1(a). For convenient comparison, the planar HEMT, all-recessed gate HEMT, and novel MC-DC HEMT were made on the same wafer. The heterojunction was grown by metal-organic chemical vapor deposition (MOCVD) on SiC substrate. The lower heterojunction consists of a 300 nm i-GaN and an 8 nm $In_{0.17}AlN$ barrier. The upper heterojunction consists of a 10 nm i-GaN and an 8 nm $In_{0.17}AlN$ barrier layer. And the channel-to-channel distance ($d_{c\text{-}c}$) is 18 nm. The Hall measurements at room temperature yielded a carrier density of 2.1×10^{13} cm^{-2} and a 2DEG mobility of 1991 $cm^2 \cdot V^{-1} \cdot s^{-1}$.

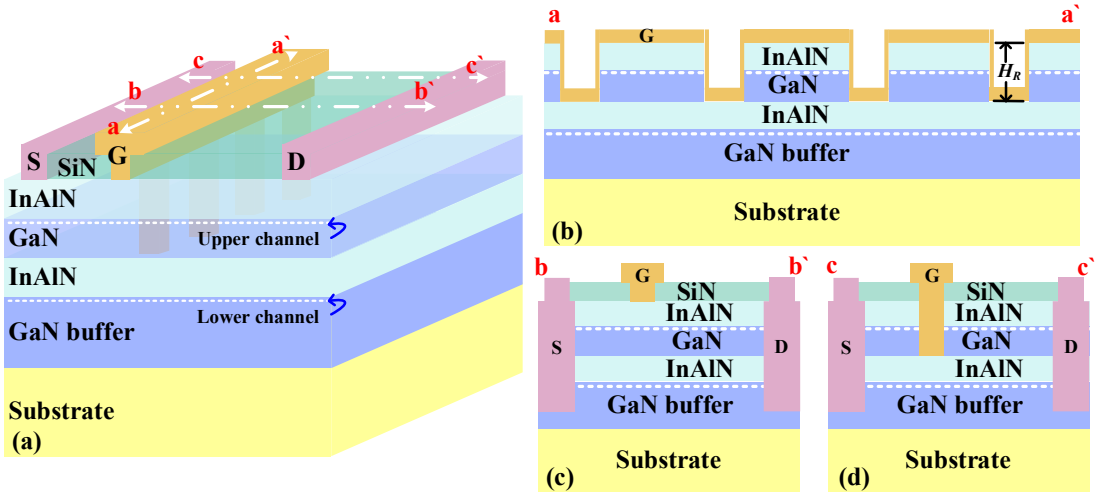

Figure A1 (Color online) (a) Structure diagram of the novel InAlN/GaN MC-DC HEMT; Cross-sectional views of the MC-DC HEMT at (b) the aa` direction: along the gate width, (c) the bb` direction: planar region along the source-drain direction, and (d) the cc` direction: recess region along the source-drain direction.

Device fabrication was started with ohmic contact formed by Ti/Al/Ni/Au evaporation at the source and drain area, followed by rapid annealing for 50 seconds at 810℃ in N_2 atmosphere, ensuring that ohmic contact is effective to the lower channel. After ion injection of the nitrogen to confirm electrical isolation, then through the transmission line measurement (TLM) achieved the ohmic contact resistance of 0.43 Ω·mm. Using the plasma-enhanced chemical vapor deposition (PECVD) to deposit a 120 nm SiN passivation layer. The gate foot is defined by electron beam lithography (EBL), and the SiN layer is removed by inductively coupled plasma (ICP) etching to create a 200 nm gate foot. The EBL is also utilized to define the periodic patterns under the gate, then self-aligned Cl_2-based ICP etching was applied to etch

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the InAlN barrier and the GaN channel in the gate region, as shown in Figure A2(a). To investigate the influence of etching recess depth (H_R) for the G_m profile, three etching recess depths of H_R = 5 nm, 12 nm, and 18 nm were designed. Figure A2(c) shows the TEM image of such a scheme. As shown in Figure A2(b), the Ni/Au/Ni metal stacks were finally deposited by electron beam evaporation to form a 600 nm gate cap. For comparison, all the devices including the planar HEMT, all-recessed gate HEMT, and novel MC-DC HEMT are designed with the same gate length (L_g) of 200 nm.

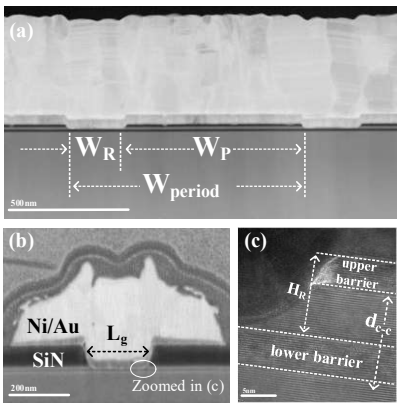

Figure A2 (Color online) (a) SEM view of the cross-section along the gate width, the width of the recess region (W_R), and the proportion of the width of the planar region (W_P) to a period width (W_{period}) called the etching ratio (α), where W_{period} = 1 μm, W_P = 800 nm, W_R = 200 nm, α = W_P/ W_{period} = 0.8; (b) SEM view of the cross-section at recess region along the gate length, using the T-type gate supported by SiN material; SEM view of the oval-shaped in (b) zoomed in (c), the etching recess depth (H_R) is defined as the downward etching distance of the upper barrier surface, where H_R = 18 nm.

Appendix B Influence of the recess depth (H_R) on the transfer characteristics

To compare the effect of H_R on the transfer characteristics, the devices with H_R =5, 12, and 18 nm were fabricated and measured by Keithley 4200 semiconductor parameter analyzer. Figure B1 shows the transfer characteristics of the planar HEMT and all-recessed gate HEMTs with three etching depths at drain voltage (V_{ds}) equals to 10 V. For planar HEMT, the maximum drain current density ($I_{d\text{-}max}$) is 1657 mA/mm and the V_{th} is -9.7 V. As the etching depth increases, the V_{th} of the device constantly floats positively [1], and the profile of the G_m curves change from double peak to a single one. According to the transconductance compensation technology [2]-[4], the planar and all-recessed gate HEMT are combined in a certain proportion to fill the lowest part of the G_m profile of the planar HEMT to achieve a larger GVS, defining the difference of the corresponding gate voltage at 80% of the $G_{m\text{-}max}$ (equals to 20% decrease) as GVS. According to Figure B1(a), at H_R = 5 nm, the G_m curve still shows double peaks and does not meet the transconductance compensation conditions. When H_R = 12 nm、18 nm, both can compensate for the lowest part of planar HEMT G_m curves. It is known that the closer the distance from the gate to the 2DEG in the channel, the greater the control ability of the gate, and the value of the $G_{m\text{-}max}$ becomes larger [5],[6], which allows for a higher G_m platform with the same GVS, therefore H_R is selected as 18 nm. Due to the recess segments did not break the lower 2DEG, which can also provide control to the lower channel, so the planar and recess segments with various threshold voltages (V_{th}) in parallel along the gate width will turn on sequentially, then achieve a broader transconductance (G_m) profile.

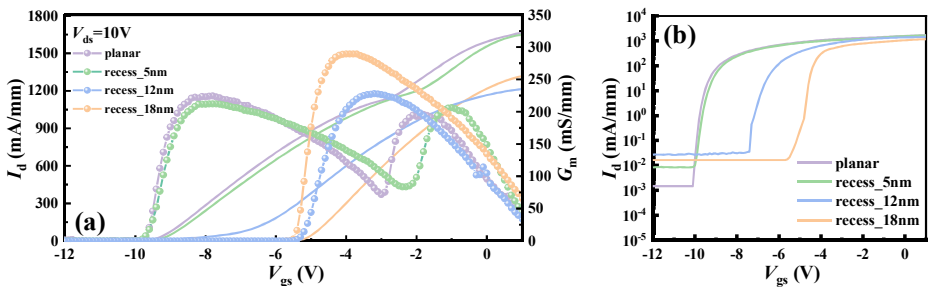

Figure B1 (Color online) (a) Comparison of transfer characteristics of the planar HEMT and all-recessed gate HEMTs with three different H_R, (b) the semi-log scale version of transfer characteristics.

The semi-log scale version of transfer characteristics is shown in Figure B1(b). The planar HEMT exhibits excellent off-state characteristics, due to the distance of the gate to the lower channel being only 26 nm, and the relatively large 200nm L_g to ensure the gate control capability. And the off-state drain currents of all-recessed gate HEMTs with different etching depths gradually degrade due to etching damage as the etch depth deepens [6].

Appendix C Influence of the etching ratio (α) on the transconductance flatness

To investigate the impact of duty ratio on transfer characteristics, the planar DC HEMT and all-recessed gate HEMT with H_R = 18 nm were selected to make a combination in parallel along the gate width to obtain MC-DC HEMTs. Figure C1(a) shows with α increasing, single $G_{m\text{-}max}$ features gradually transformed into double peaks, and the $G_{m\text{-}max}$ value decreased from 279.2 mS/mm at α = 0.5 to 216.3 mS/mm at α = 0.8, but GVS reaches a maximum amplitude of 7.8 V. And the threshold voltage drifted negative to -9.3 V, $I_{d\text{-}max}$ increase to 1622 mA/mm, as shown in Figure C1(b).

It is known that when the power amplifier enlarges an input signal of frequency f, the base wave output signal and G_m are positively correlated, while the harmonic output at frequencies 2f and 3f are also positively correlated with the first and second-order derivatives of G_m [2]. Figures C1(c) and (d) reveal that when α = 0.8, the derivatives of G_m of the novel MC-DC HEMT improve slightly in the transition region from the subthreshold to the peak value. In the linear increase region, the G_m profile of the novel MC-DC HEMT is much flatter, thus suppressing the undesired harmonic component. The results show that the novel MC-DC HEMT structure effectively improves the transconductance flatness.

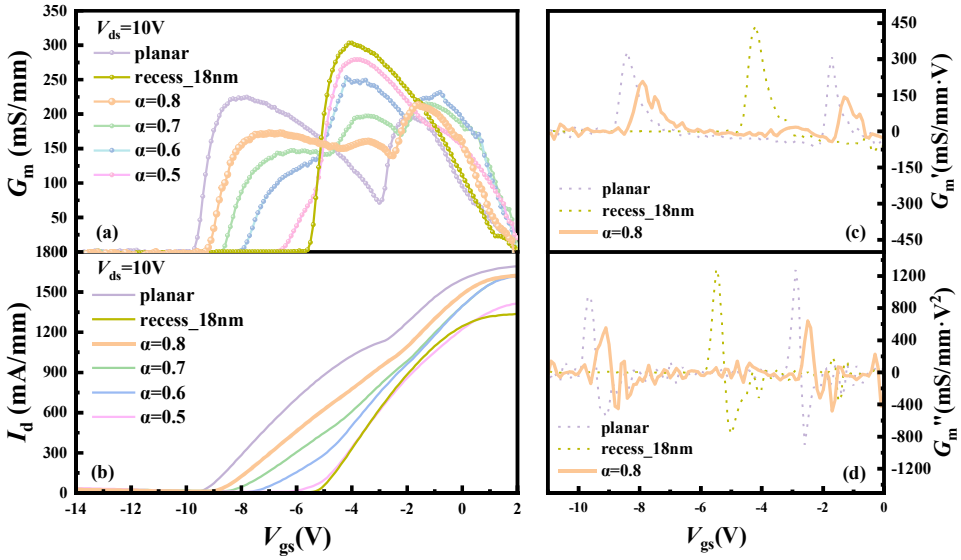

Figure C1 (Color online) Effect of α on the novel DC HEMT (a) G_m profile and (b) transfer characteristics, at α = 0.8 (c) first and (d) second-order derivatives of G_m profiles of HEMT.

Appendix D The small signal characteristics of the novel device

To characterize the small-signal performance of the novel MC-DC HEMT, the S-parameters of the device with fixed W_R = 0.2 μm, H_R = 18 nm, α = 0.8 were measured around $G_{m\text{-}max}$ using an Agilent 8363B network analyzer in the frequency range of 100 MHz to 40 GHz. The f_T and f_{max} are obtained by the slope of -20 dB/decade extrapolated current gain (H_{21}) and maximum stable gain (MSG). As shown in Figures D1(a) and (b), the maximum f_T/f_{max} for planar HEMTs and MC-DC HEMTs are 33/80 GHz and 34/72 GHz, respectively. f_T and f_{max} gradually decrease as the upper channel of planar HEMT turns on with increasing gate voltage, but MC-DC HEMTs can maintain f_T and f_{max} constant over a very wide gate voltage range of GVS over 7 V, as shown in Figure D1(c) and (d).

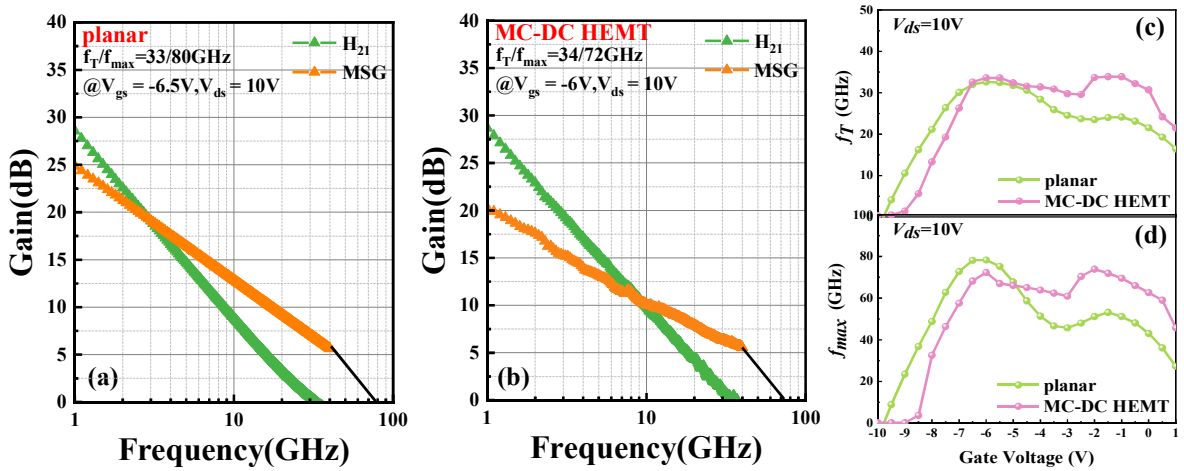

Figure D1 (Color online) V_{ds} = 10 V, H_{21} and MSG in relationship with frequency (a) planar and (b) MC-DC HEMTs; (c) f_T and (d) f_{max} versus V_{gs}.

Appendix E The large signal characteristics of the novel device

To validate the improved linearity of MC-DC HEMT and the reduction of intermodulation distortion, two-tone intermodulation distortion was measured with a central frequency (f_0) of 3.6 GHz and a tone spacing (Δf) of 10 MHz at V_{ds} = 10 V. Figure D1 shows the two-tone characteristics of planar DC HEMT and MC-DC HEMT at 3.6 GHz with 10 MHz tone spacing. The OIP_3 of the planar DC HEMTs is 28 dBm, while the OIP_3 of MC-DC HEMT is 38 dBm, corresponding to the input third-order intercept point (IIP_3) of 27 dBm. This result shows a good agreement with the flatter G_m curve, and the G_m', G_m'' of the MC-DC HEMT is closer to zero over a wide range of V_{gs}, effectively suppressing harmonics and OIP_3 degradation, making MC-DC HEMT a competitive candidate in realizing high linearity at high power conditions.

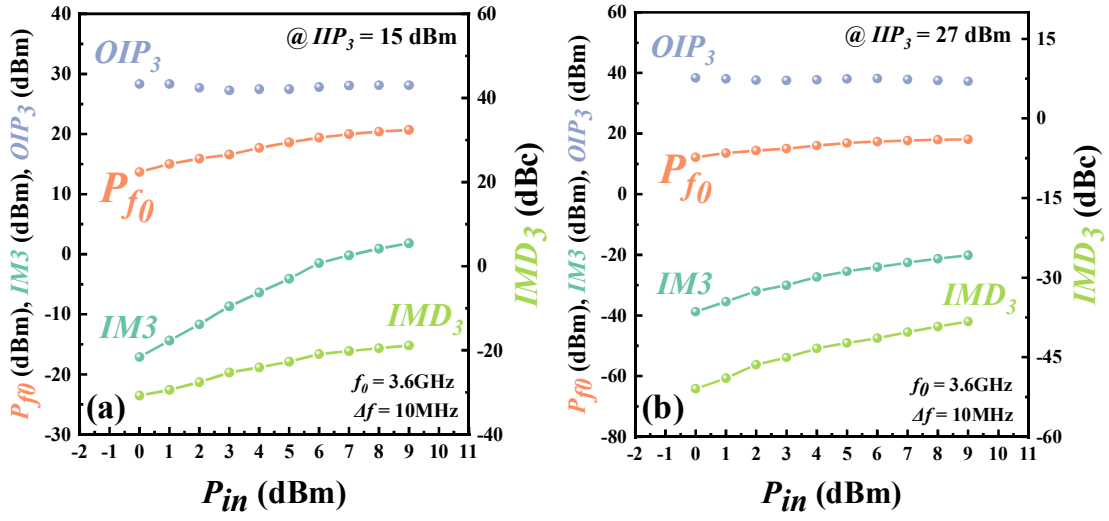

Figure E1 (Color online) two-tone power linearity measurements at 3.6 GHz with a tone spacing of 10 MHz for (a) planar DC HEMT and (b) MC-DC HEMT of W_R = 200 nm, H_R = 18 nm, α = 0.8.

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