Toward functional verifying a family of systemC TLMs

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Problems & Ideas

- To verify a family of SoC TLM designs:
  - Many combinations of features to form a design
  - Each design is verified one by one
  - Some may be unable to be verified
- Ideas: Should all the features to be considered in verifaction?
  - Identify mute- future-modules that would be pruned for the given property
  - To reduce the number of designs in a family for the given property to be verified

Main Contributions

- **It is the first time a method is proposed for verifying a family of SoC designs;**
- **An extended cone-of-influence(COI) method to identify unrelated modules according to the given property;**
- **An extended formal model is proposed to modeling fea- ture modules in SystemC and the correctness of our method is proven based on it.**

Experimental results

Property	Memory (MB)				Verification Time (s)			
	*CPU*0	*CPU*1	*CPU*2	*CPU*3	*CPU*0	*CPU*1	*CPU*2	*CPU*3
P1	15.9	17.8	NT	NT	8.2	10.7	NT	NT
P2	23.1	33.2	/	NT	15.7	28.4	/	NT
P3	/	/	47.3	NT	/	/	35.8	NT
P4	12.7	23.3	31.8	NT	7.7	18.4	29.9	NT
P5	/	/	57.8	NT	/	/	50.1	NT