nature materials

SUPPLEMENTARY INFORMATION

DOI: 10.1038/NMAT2748

Supplementary

Complementary resistive switches for passive nanocrossbar memories

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DOI: 10.1038/NMAT2748

S1 3D-Stacking

A test of multilayer stacking to demonstrate the feasibility of 3D integration is shown in figure S1.1.

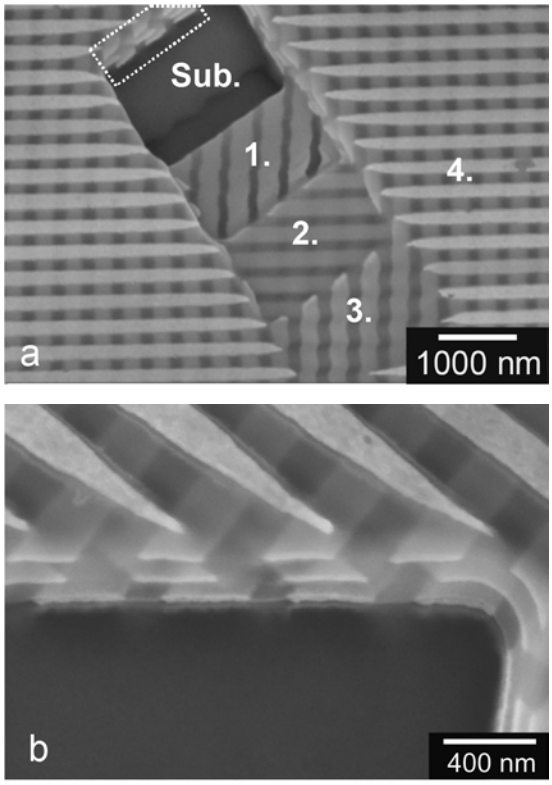

Fig. S1.1

a) Focused Ion Beam (FIB) cut of a multilayer crossbar array. The orthogonally arranged metal layers (1. to 4.) are visible [1].

b) SEM image of a FIB cut into a multilayer crossbar array. In this cross section view the vertical structure is shown [2].

S2 Initialization process

Data from an initialization process is shown in the following figure S2.1. A differently processed sample has been used for S2.1 than for figure 2g. The resulting HRS to LRS ratio is similar in both cases, but altogether larger R values are obtained here (see figure S2.1). It should be mentioned that under standard fabrication conditions in the semiconductor industries variations of the virgin resistance of less than 10% are achieved.

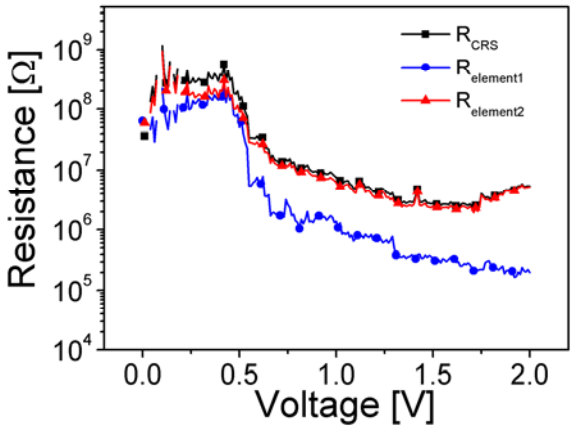

Fig. S2.1

Resistance measurement of a CRS during initialization process. Black squares indicate the resistance of the CRS. Blue circles and red triangles denote the resistances of memristive element 1 and 2, respectively.

Both memristive elements are initially in the HRS exhibiting a resistance of around 100 MΩ, thus the CRS is in the HRS/HRS (OFF) state. This state only exists after fabrication and plays no role during normal operation. To store information in this CRS, a voltage is applied. Due to the fact that both memristive elements form a voltage divider, the required voltage is at least $2V_{th,1}$ or $2V_{th,3}$ depending on polarity and resistance variations after fabrication. At a voltage of around 550 mV, one of the memristive elements switches to the LRS, visible as a distinctive decrease of the resistance in figure S2.1. The other memristive element remains in the HRS due to the voltage polarity. However, a decreasing resistance of this element is notable, which is due to the voltage dependency of the HRS (see Ref. 27). Nevertheless, this element functions as a current compliance for the successfully switched memristive element. When finishing the initialization process at a voltage of 2 V, a resistance ratio between both elements of 27 is achieved in this case.

Thus, information was stored in the as-fabricated CRS proving the successful transition from the HRS/HRS state to the LRS/HRS state.

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S3 Spike read scheme

From figure 3b one can see that current spikes occur, if the CRS changes its state. Those spikes can be used for the read procedure, if enough charge is generated to be detected by CMOS sense amplifiers. The detection limit of the sense amplifier directly influences the amount of charge needed to generate a sufficient voltage drop. For a CRS based RAM $\Delta V = Q_{spike} / C_{BL}$ holds. (Q_{spike} is the charge of a current spike, C_{BL} the bitline capacity and ΔV the read voltage margin.)

The minimum spike charge needed for a CMOS sense amplifier is:

$$Q_{spike,min} = \Delta V_{min} \bullet C_{BL}$$

The minimum spike charge is derived under the assumption of a feature size of F = 10 nm, ΔV = 50 mV with C_{BL} calculated according to a scaling model [3, 4]:

$$C_{BL}(F) = C_{BL}(50\ \text{nm})\left(\frac{F}{50\ \text{nm}}\right)^{0.7}$$

$$C_{BL}(50\ \text{nm}) = 20\ \text{fF}$$

$$C_{BL}(F = 10\ \text{nm}) = C_{BL}(50\ \text{nm})\left(\frac{10\ \text{nm}}{50\ \text{nm}}\right)^{0.7} = 20\ \text{fF}\left(\frac{10\ \text{nm}}{50\ \text{nm}}\right)^{0.7} = 6{,}48\ \text{fF}$$

The minimum spike charge is then:

$$Q_{spike,min} = \Delta V_{min} \bullet C_{BL} = 50\ \text{mV} \bullet 6.48\ \text{fF} = 3.24 \bullet 10^{-16}\ \text{C} \approx 2000\ \text{electrons}$$

Assuming LRS = 1 kΩ and V = 1 V we can calculate the current in the ‘ON’-state of the CRS:

$$I_{ON} = \frac{V}{R_{ON}} = \frac{1\ \text{V}}{2\ \text{k}\Omega} = 500\ \mu\text{A} \quad \text{with } R_{ON} = 2\ \text{LRS} = 2\ \text{k}\Omega$$

The minimum needed switching time $t_{on,min}$ to assure a proper read is:

$$t_{on,min} = \frac{Q_{spike,min}}{I_{ON}} = \frac{2000\ e}{500\ \mu\text{A}} = 0{,}64\ \text{ps}$$

If the switching time of the CRS is larger than 0.64 ps, a proper read-out will be possible.

DOI: 10.1038/NMAT2748

S4 Symmetrization by an additional series resistor

I-V-characteristics of resistive switching elements often have an asymmetry in terms of switching voltage ($|V_{th,SET}| > |V_{th,RESET}|$). Such an asymmetric *I-V*-characteristic can be balanced by integration of a series resistor.

In general, $|V_{read,min}| = |V_{th,1}| = |V_{th,3}| = |V_{th,SET}|$ and $|V_{read,max}| = |V_{th,2}| = |V_{th,4}| = |V_{th,SET}| + |V_{th,RESET}|$ hold for a symmetric CRS and a proper read voltage must be in the range of $|V_{read,min}| < |V_{read}| < |V_{read,max}|$ (see figure 2 and 3). For an asymmetric CRS with $\left|V_{th,RESET}\right| < \frac{\left|V_{th,SET}\right|}{2}$ the CRS will not switch to a stable 'ON' state because $|V_{read}| = |V_{read,min}|$ is already large enough to switch the CRS to state '0' or state '1', respectively. With an additional series resistor (figure S4.1) this problem can be solved. The voltage drop over memristive element A is then:

$$\left|V_A\right| = \frac{R_{LRS}}{2R_{LRS} + R_{series}}\left|V_{read}\right|$$

For $|V_{read}| = |V_{read,max}|$, the voltage over memristive element A should be $|V_A| \leq |V_{th,RESET}|$:

$$\left|V_{th,RESET}\right| \geq \frac{R_{LRS}}{2R_{LRS} + R_{series}}\left(\left|V_{th,RESET}\right| + \left|V_{th,SET}\right|\right)$$

It follows:

$$R_{series} \geq R_{LRS}\left[\frac{\left|V_{th,SET}\right|}{\left|V_{th,RESET}\right|} - 1\right] \quad (1)$$

With equation (1) the series resistor can be dimensioned properly to symmetrise an asymmetric *I-V*-characteristic of a CRS.

For $|V_{th,SET}|$ = 1 V and $|V_{th,RESET}|$ = 0.5 V (figure S4.2a) e.g. a series resistor with $R_{series} = R_{LRS}$ should be inserted, which would result in $|V_{th,1}| = |V_{th,3}|$ = 1 V and $|V_{th,2}| = |V_{th,4}|$ = 1.5 V (figure S4.2b).

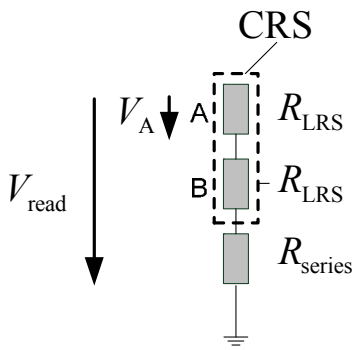

Fig S4.1

Equivalent circuit for a CRS with series resistor.

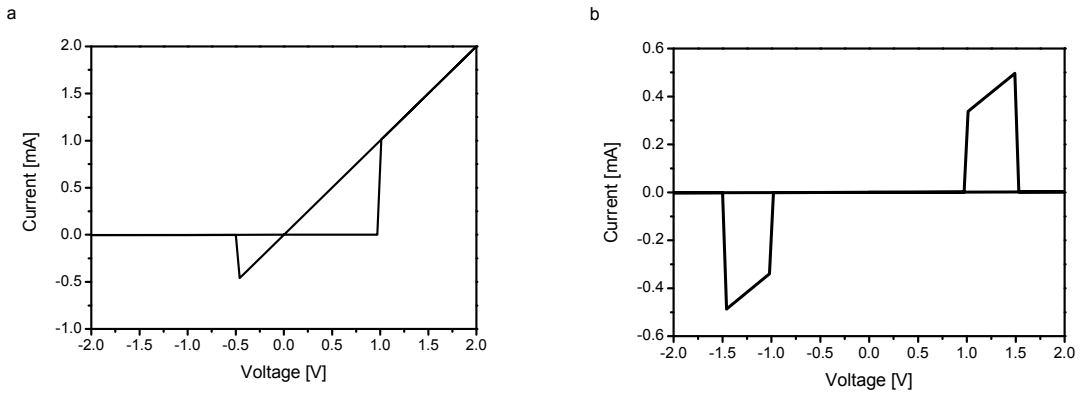

Fig. S4.2

a) asymmetric *I*-*V*-characteristic of a single memristive element with $|V_{th,SET}|$ = 1 V and $|V_{th,RESET}|$ = 0.5 V.

b) *I*-*V*-characteristic of a CRS built of two memristive elements with a characteristic from a) and a series resistor $R_{series} = R_{LRS}$.

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S5 Comparison of a single memristive elements based array and a CRS based array

Assume two crossbar arrays (see figure S5.1), which both store the same digital information (worst case pattern), one made of memristive elements (case 1) and one made of CRS (case 2). When reading a word (one row) the measurable normalized read voltage margin $\Delta V / V_{pu}$ is the important parameter.

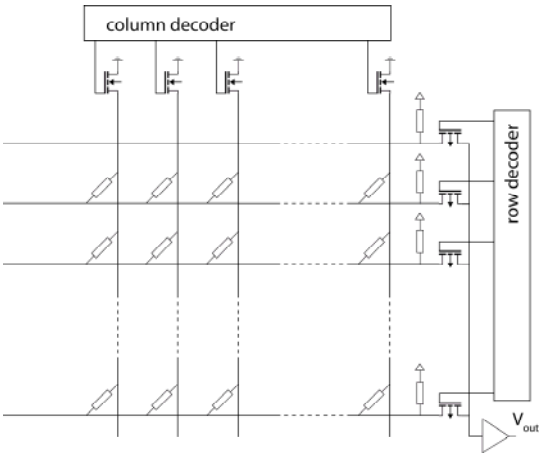

Fig. S5.1

crossbar array and periphery

We consider a read scheme[5] where all bit lines are pulled up. The pull up resistor is set to $R_{pu,1} = R_{LRS}$ for a crossbar with single memristive elements and to $R_{pu,2} = R_{ON}$ for a crossbar with CRS. The equivalent circuit of the crossbar can be seen in figure S5.2a and S5.2b, respectively.

Case 1:

The sneak resistances R_{sneak_a} and R_{sneak_b} for case 1 (star-mesh transformation):

$$R_{sneak\_a,1} = \frac{\left(\frac{R_{LRS}}{M-1} + \frac{R_{LRS}}{(N-1)(M-1)}\right) \cdot \frac{R_{LRS}}{N-1} + \frac{R_{pu,1}}{N-1} \cdot \frac{R_{LRS}}{N-1} + \left(\frac{R_{LRS}}{M-1} + \frac{R_{LRS}}{(N-1)(M-1)}\right) \cdot \frac{R_{pu,1}}{N-1}}{\frac{R_{pu,1}}{N-1}}$$

$$R_{\text{sneak\_b,1}} = \frac{\left(\frac{R_{\text{LRS}}}{M-1} + \frac{R_{\text{LRS}}}{(N-1)(M-1)}\right) \cdot \frac{R_{\text{LRS}}}{N-1} + \frac{R_{\text{pu,1}}}{N-1} \cdot \frac{R_{\text{LRS}}}{N-1} + \left(\frac{R_{\text{LRS}}}{M-1} + \frac{R_{\text{LRS}}}{(N-1)(M-1)}\right) \cdot \frac{R_{\text{pu,1}}}{N-1}}{\frac{R_{\text{LRS}}}{N-1}}$$

The effective sensable resistance value for both digital values:

$$R_{\text{HRS,sense}} = \frac{R_{\text{sneak\_a,1}} \cdot R_{\text{HRS}}}{R_{\text{sneak\_a,1}} + R_{\text{HRS}}}$$

$$R_{\text{LRS,sense}} = \frac{R_{\text{sneak\_a,1}} \cdot R_{\text{LRS}}}{R_{\text{sneak\_a,1}} + R_{\text{LRS}}}$$

Furthermore:

$$R_{\text{pu,eff,1}} = \frac{R_{\text{sneak\_b,1}} \cdot R_{\text{pu,1}}}{R_{\text{sneak\_b,1}} + R_{\text{pu,1}}}$$

The resulting measurable normalized read voltage margin:

$$\frac{\Delta V}{V} = \frac{R_{\text{HRS,sense}}}{R_{\text{HRS,sense}} + R_{\text{pu,eff,1}}} - \frac{R_{\text{LRS,sense}}}{R_{\text{LRS,sense}} + R_{\text{pu,eff,1}}}$$

Case 2:

The sneak resistances $R_{\text{sneak\_a}}$ and $R_{\text{sneak\_b}}$ for case 2 (star-mesh transformation):

$$R_{\text{sneak\_a,2}} = \frac{\left(\frac{R_{\text{state\_0or1}}}{M-1} + \frac{R_{\text{state\_0or1}}}{(N-1)(M-1)}\right) \cdot \frac{R_{\text{ON}}}{N-1} + \frac{R_{\text{pu,2}}}{N-1} \cdot \frac{R_{\text{ON}}}{N-1} + \left(\frac{R_{\text{state\_0or1}}}{M-1} + \frac{R_{\text{state\_0or1}}}{(N-1)(M-1)}\right) \cdot \frac{R_{\text{pu,2}}}{N-1}}{\frac{R_{\text{pu,2}}}{N-1}}$$

$$R_{\text{sneak\_b,2}} = \frac{\left(\frac{R_{\text{state\_0or1}}}{M-1} + \frac{R_{\text{state\_0or1}}}{(N-1)(M-1)}\right) \cdot \frac{R_{\text{ON}}}{N-1} + \frac{R_{\text{pu,2}}}{N-1} \cdot \frac{R_{\text{ON}}}{N-1} + \left(\frac{R_{\text{state\_0or1}}}{M-1} + \frac{R_{\text{state\_0or1}}}{(N-1)(M-1)}\right) \cdot \frac{R_{\text{pu,2}}}{N-1}}{\frac{R_{\text{ON}}}{N-1}}$$

DOI: 10.1038/NMAT2748

The effective sensable resistance values for both digital values:

$$R_{\text{state\_0,sense}} = \frac{R_{\text{sneak\_a,2}} \cdot R_{\text{state\_0}}}{R_{\text{sneak\_a,2}} + R_{\text{state\_0}}}$$

$$R_{\text{ON,sense}} = \frac{R_{\text{sneak\_a,2}} \cdot R_{\text{ON}}}{R_{\text{sneak\_a,2}} + R_{\text{ON}}}$$

Furthermore:

$$R_{\text{pu,eff,2}} = \frac{R_{\text{sneak\_b,2}} \cdot R_{\text{pu,2}}}{R_{\text{sneak\_b,2}} + R_{\text{pu,2}}}$$

The resulting measurable normalized read voltage margin:

$$\frac{\Delta V}{V} = \frac{R_{\text{state\_0,sense}}}{R_{\text{state\_0,sense}} + R_{\text{pu,eff,2}}} - \frac{R_{\text{ON,sense}}}{R_{\text{ON,sense}} + R_{\text{pu,eff,2}}}$$

Values for the plots in figure 4:

$R_{\text{state\_0or1}} = R_{\text{state\_0}} = R_{\text{state\_1}} \approx R_{\text{HRS}} = 1 \cdot 10^8\ \Omega$

$R_{\text{LRS}} = R_{\text{pu,1}} = 1 \cdot 10^3\ \Omega$

$R_{\text{ON}} = 2R_{\text{LRS}} = R_{\text{pu,2}} = 2 \cdot 10^3\ \Omega$

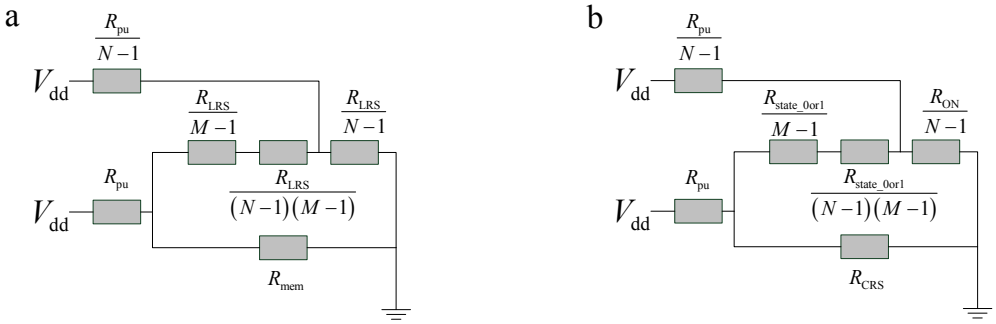

Fig. S5.2

Equivalent circuit for single memristive crossbar array (a) and CRS based crossbars (b).

In our calculations we assumed the line resistance R_{Line} to be small compared to R_{LRS}. This is true if the R_{LRS} is sufficient large and R_{Line} sufficient small. In the following examples we calculate the line resistance for various feature sizes. We incorporate the size effect of the wire by application of the Fuchs-Sondheimer approximation[6] to include a rough estimation of the size effect:

$$\rho_{Cu}(F) = \rho_{Cu,0}\left(1+\frac{3}{4}\frac{\lambda_0}{F}(1-p)\right)$$

F is the feature size, $\rho_{Cu,0}$ is bulk resistivity of copper ($\rho_{Cu,0}$ = 2.2 μΩcm)[7], ρ_0 is the bulk mean free path (ρ_0 = 35 nm)[7] and p is the specularity (p = 0.5)[8].

The worst case line resistance for an element in the middle of an array and an assumed aspect ratio of the interconnect line of 10 is:

$$R_{Line} = \rho_{Cu}(F)\frac{L}{A} = \rho_{Cu}(F)\frac{2\cdot N\cdot F}{F\cdot 10F} = \rho_{Cu}(F)\frac{2\cdot N}{F\cdot 10}$$

The results are summarized in the table:

Feature size *F*	$\rho_{Cu}(F)$	***N* = 10^3**	***N* = 10^4**	***N* = 10^5**
200 nm	2.3 μΩcm	23 Ω	230 Ω	2.3 kΩ
100 nm	2.5 μΩcm	50 Ω	500 Ω	5.0 kΩ
50 nm	2.8 μΩcm	110 Ω	1.1 kΩ	11 kΩ
22 nm	3.5 μΩcm	210 Ω	2.1 kΩ	21 kΩ

If we assume R_{LRS} = 30 kΩ and allow 10% of R_{LRS} for R_{Line}, that is 3 kΩ, the green shaded fields depict possible array size and feature size.

There is a trade-off between sufficient high R_{LRS} and retention time of bipolar resistive switching materials. However, the suitable operation window is large enough as shown for example in [9].

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