# Ultra-fast switching memristors based on two-dimensional materials

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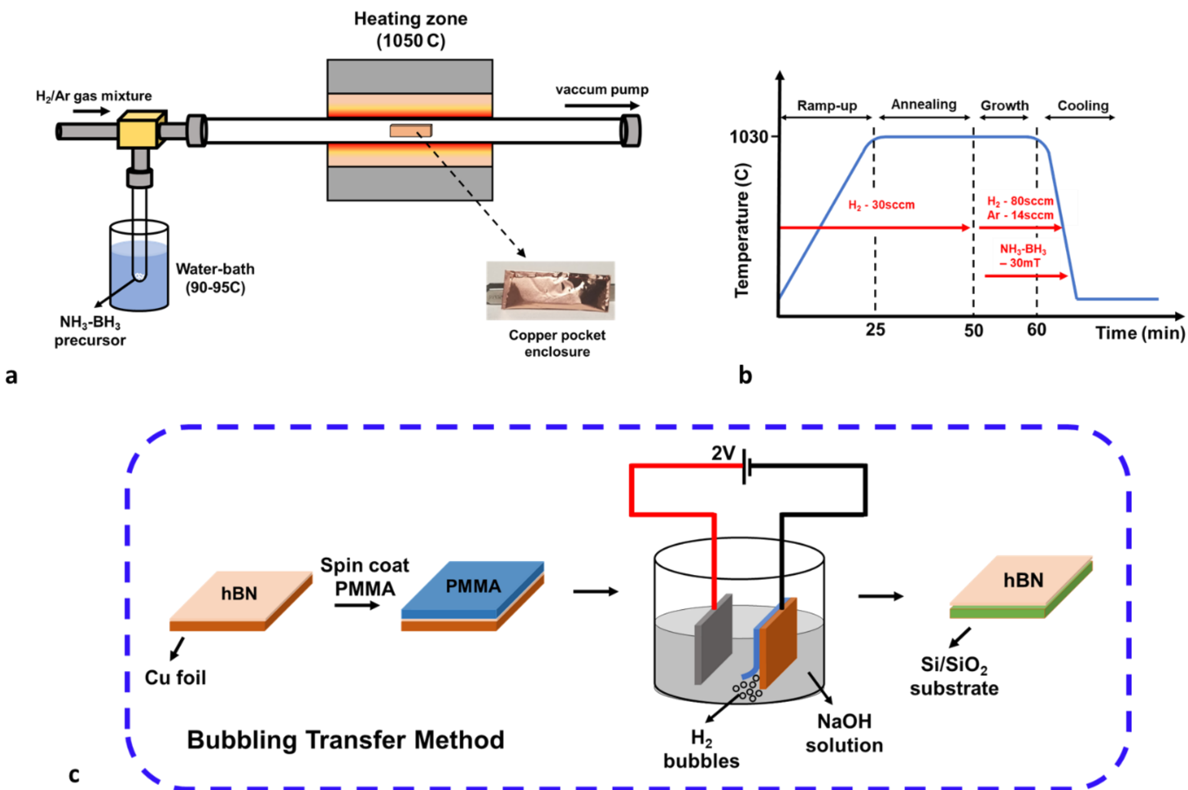
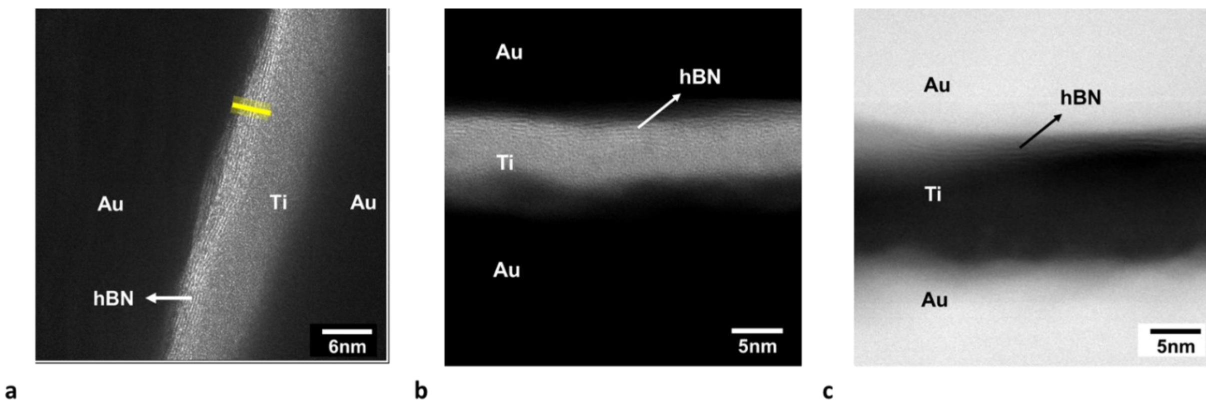
## Supplementary information

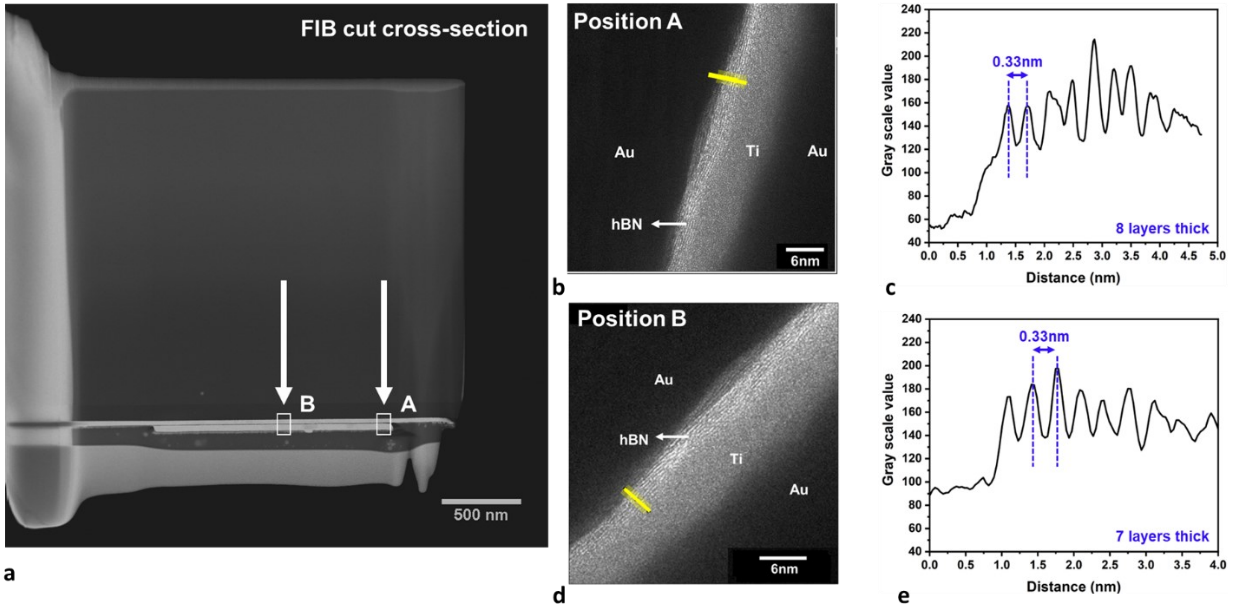



**Supplementary Figure1: (a)** Schematic of low pressure CVD growth chamber used for hBN synthesis on copper foils **(b)** Temperature profile of the furnace during the growth process **(c)** Schematic of the bubbling transfer method.

Few layer hBN stacks are grown by Chemical Vapor deposition (CVD) on copper foils [S1-S3] that are electropolished [S4-S5] to reduce surface roughness. The growth is conducted at 1030C using ammonia borane precursor [S1-S4]. The copper foil is folded into a pocket that creates a copper-saturated environment on the inside which limits the sublimation of copper, resulting in a smoother surface [S6-S7]. The smooth surface reduces the nucleation density promoting large-area growth with reduced grain boundaries. Grain boundaries can be detrimental to memristor performance since they accelerate ion migration and reduce the endurance of the device. The base pressure of the CVD system is 6mT before the growth. During annealing, the pressure reaches around 230mT with 30sccm $H_2$ flowrate. The pressure is increased to 650mT at the beginning of the growth with 80sccm $H_2$ and 14sccm Ar. A valve separates the main chamber from the precursor ampoule, as shown in Supplementary Fig. 1a. The ammonia borane decomposes when heated, and the pressure builds up within the ampoule. To ensure uniform growth pressure, the valve to the main chamber is opened only after the pressure within the ampoule reaches 50mT. This pressure is maintained throughout the growth duration. The grown hBN films were transferred from copper foil onto $Si/SiO_2$ (285nm) substrate through the bubbling transfer method [S8-S9].

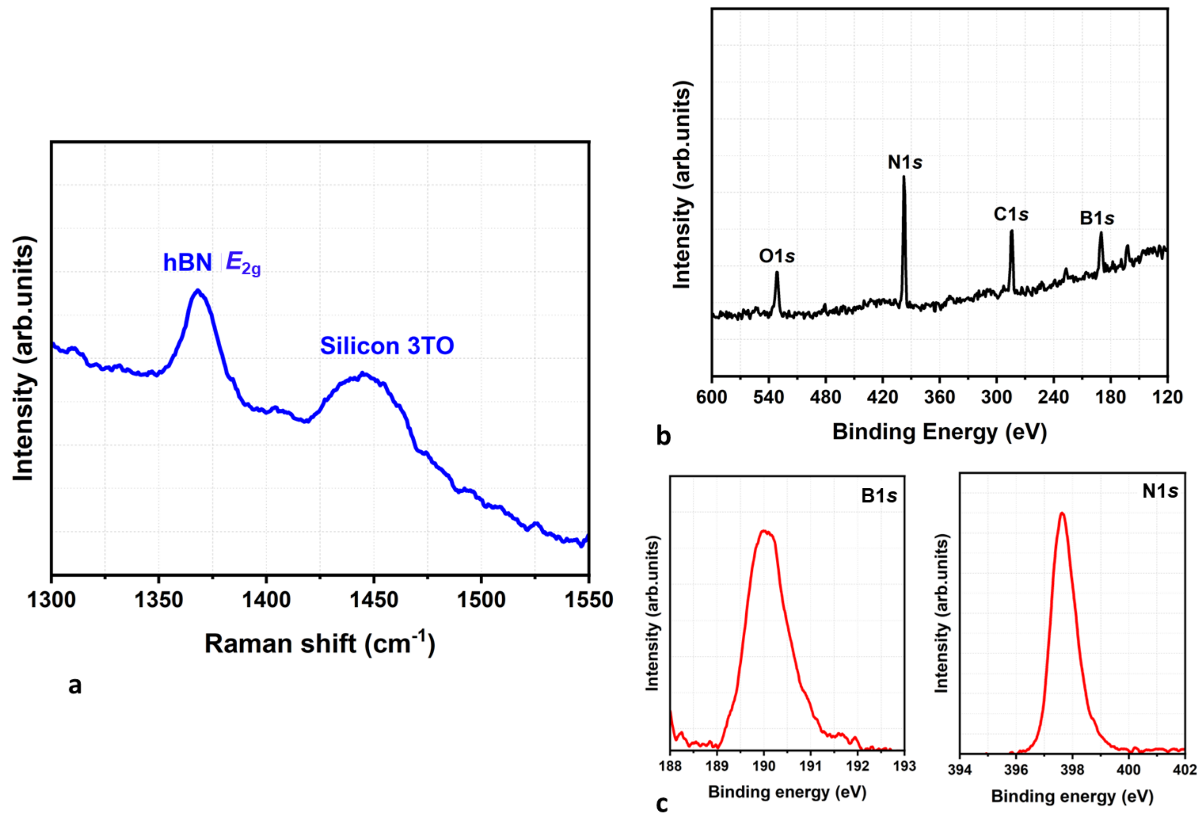



**Supplementary figure 2:** (a) Phase contrast TEM image of the memristor device cross-section showing the layered structure of hBN films. The titanium layer thickness matches with the crystal thickness monitor reading during e-beam evaporation (b) Annular Bright field scanning TEM image of the same FIB cross-section shows the layered structure, thereby confirming that the layers observed in phase contrast TEM image are not Fresnel fringes but originate from the hBN film (c) Annular Dark field scanning TEM (ADF-STEM) image of the same cross-section.

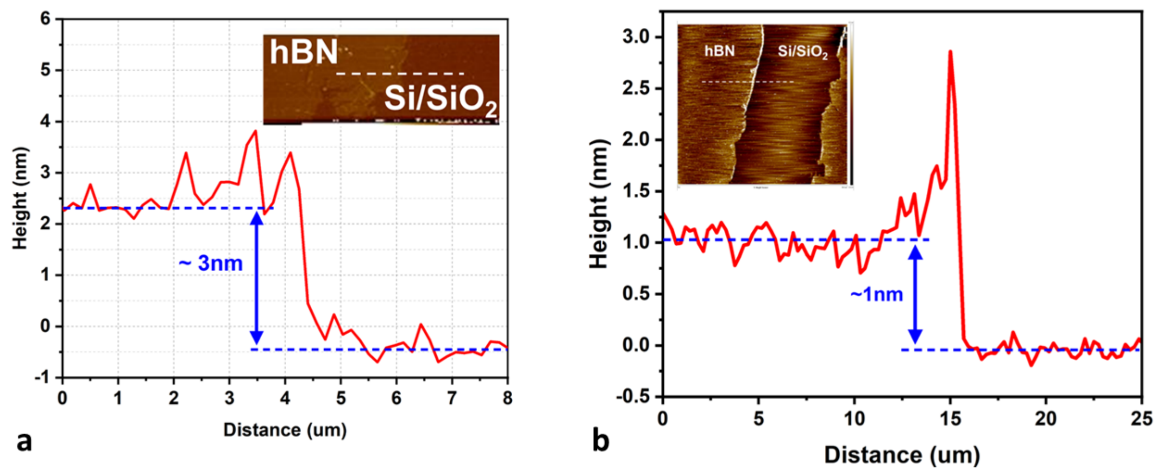



**Supplementary figure 3:** (a) Focused ion beam (FIB) cut cross-section of the sample highlighting two different locations A, B where the TEM images have been collected (b) Phase contrast TEM image from location A showing the layered structure (c) Grayscale pixel profile of the image across the marked yellow line shown in panel b. The grayscale profile shows 8 peaks corresponding to 8 hBN layers. The interlayer separation is around 0.33nm which closely matches reported values [S10-S12]. (d) Phase contrast TEM image from location B showing (e) Grayscale profile across the marked yellow line in panel d. The hBN thickness is around 7 layers.

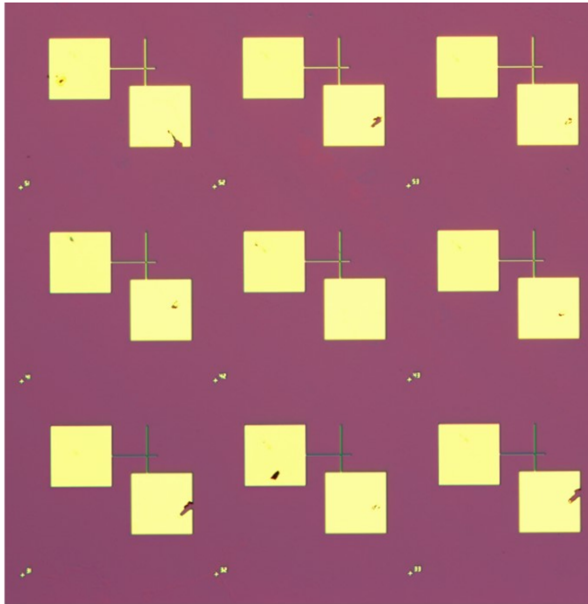
The layered structure observed at different locations shows excellent uniformity of the synthesized hBN films.




**Supplementary figure 4:** (a) Raman spectrum of the hBN film transferred onto $Si/SiO_2$ substrate. The $E_{2g}$ peak at 1368cm$^{-1}$ [S13-S14] confirms the good quality of the synthesized hBN films. (b) X-ray Photoelectron spectra of the transferred hBN film. The survey plot shows the elemental 1*s* core level peaks of B, C, N and O. (c) High-resolution XPS spectra collected around B 1*s* (190.2eV) and N 1s (397.7eV) [S15].




**Supplementary figure 5:** (a) Atomic force micrography (AFM) height profile of thick hBN (7-8 layers) across the line marked in the inset. The measured thickness of 3nm closely matches expected thickness of 8 layers hBN film (b) AFM height profile of the thin hBN (3-4 layers) across the line marked in the inset. The thin hBN films are synthesized under lower precursor vapor pressure conditions (P ~ 5mT) achieved by reducing the quantity of precursor added to the ampoule.



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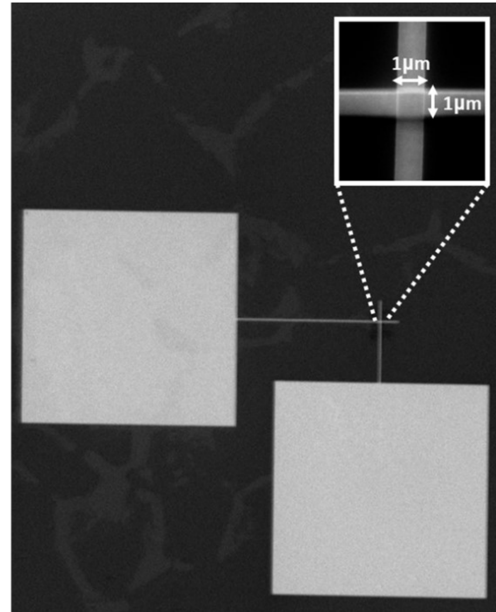


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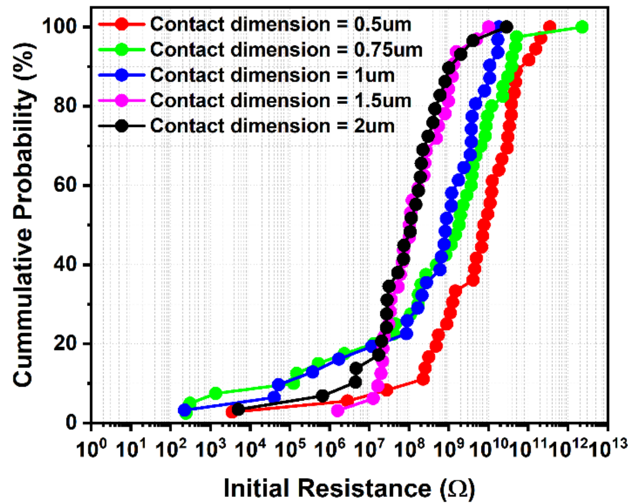
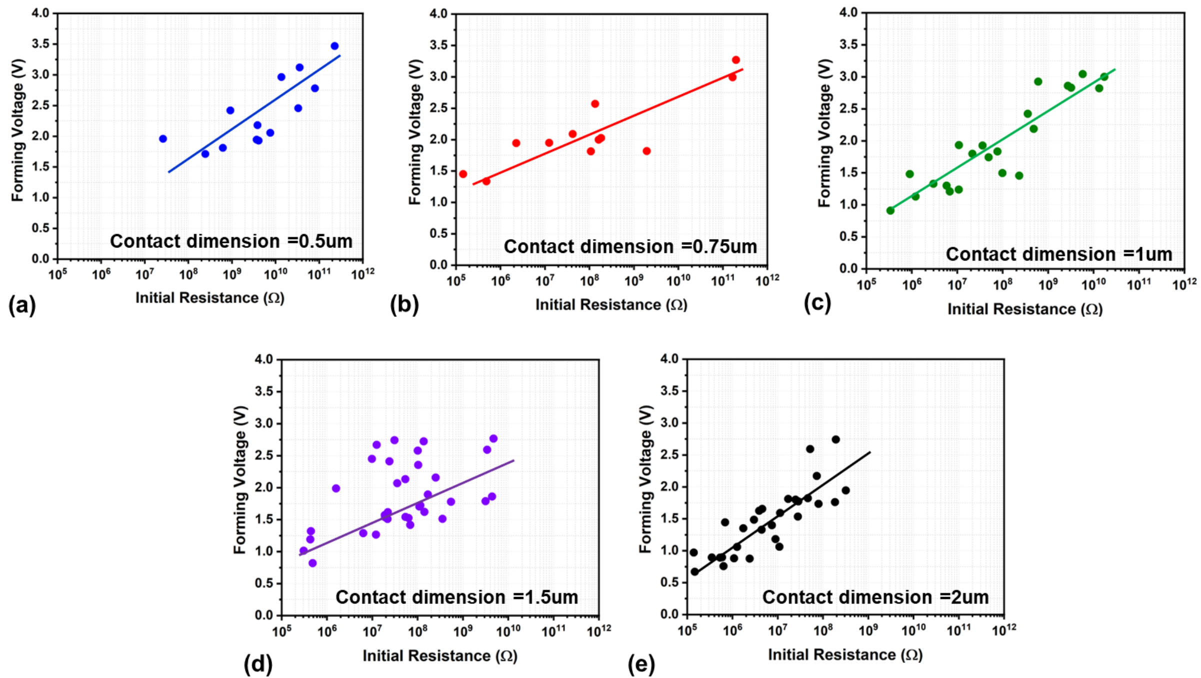
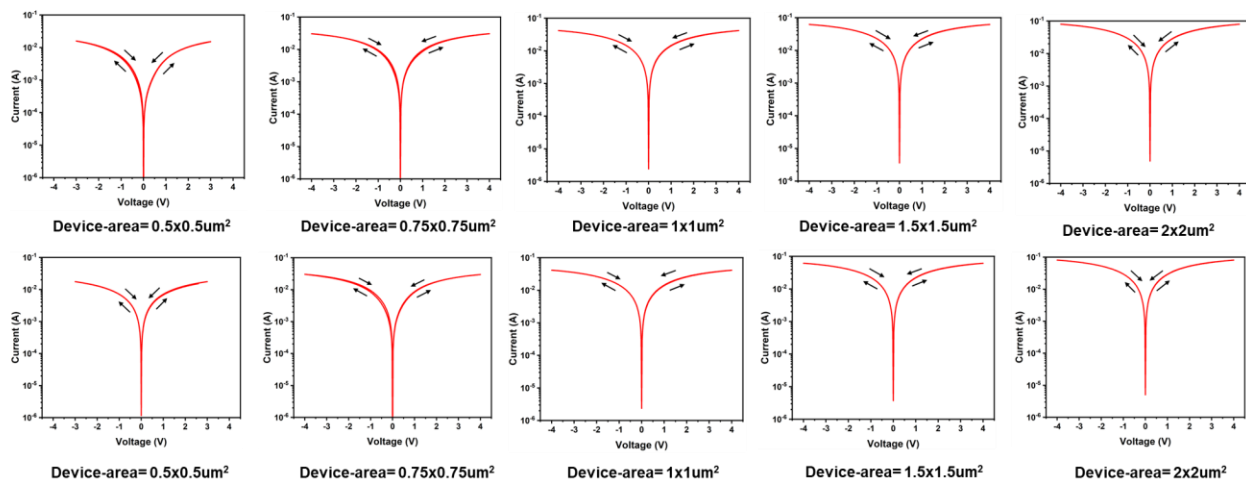
**Supplementary figure 6:** (a) Optical Microscope image of the devices with varying cross-sectional dimensions (500x500nm$^2$ to 2x2um$^2$) (b) Scanning Electron Microscope image of the memristor device cross over point (inset) where top and bottom electrodes overlap.



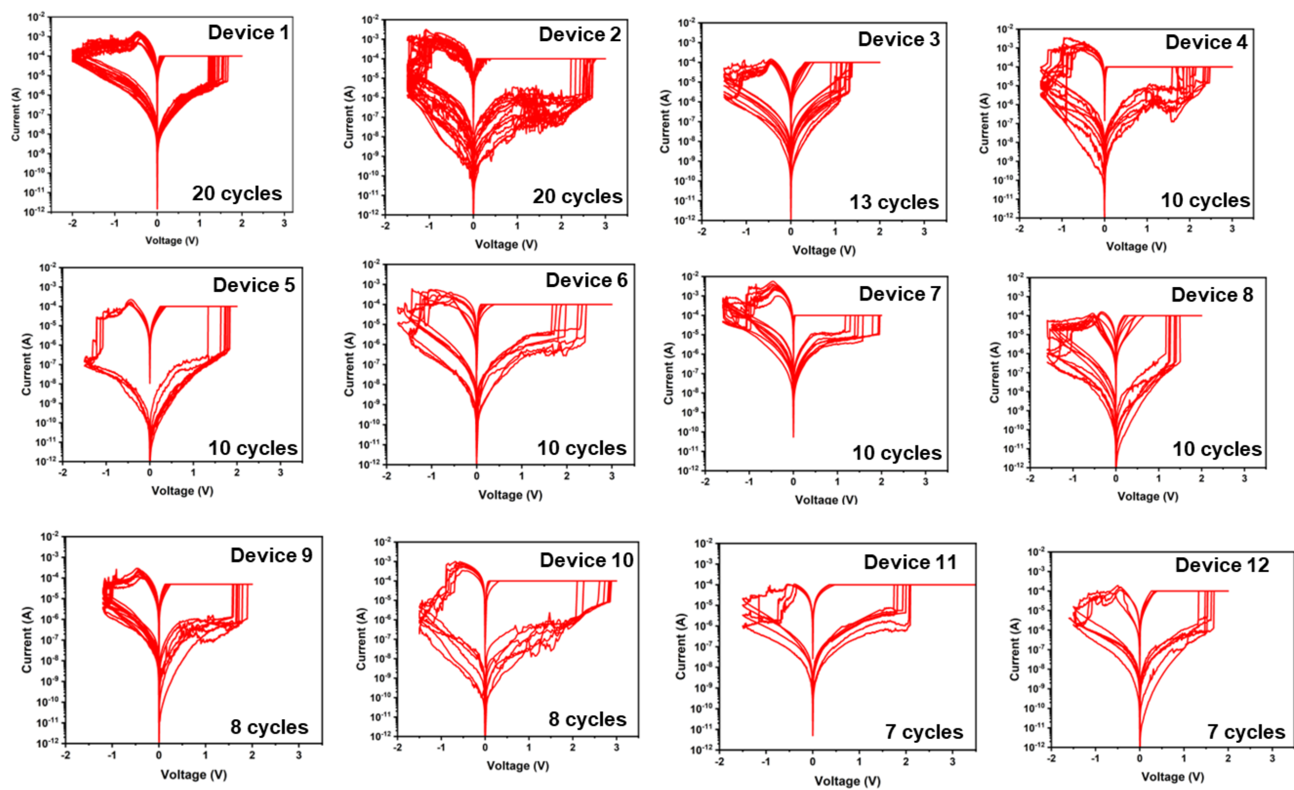

**Supplementary figure 7.1:** Cumulative distribution of Initial Resistance for devices with varying contact dimensions (0.5um shown in red, 0.75um shown in green, 1um shown in blue, 1.5um shown in pink, 2um shown in black). The initial resistance distribution shift to lower values as the device dimension increases.




**Supplementary figure 7.2:** Forming voltage vs Initial Resistance for devices with contact dimensions (a) 0.5um (b) 0.75um (c) 1um (d) 1.5um (e) 2um. Evidently, the forming voltage increases with initial resistance for all device dimensions. Therefore, a generic relationship can be established between initial resistance and forming voltage for the 2D hBN based memristor devices.



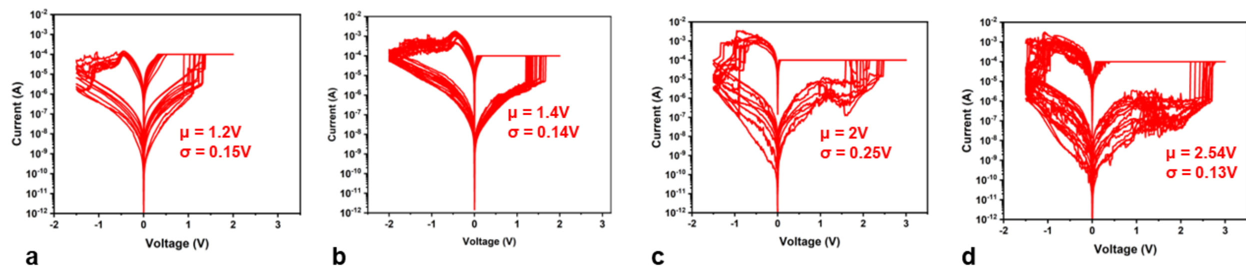

**Supplementary figure 8:** DC IV characteristics of Ti/Au devices (no hBN layer) with varying dimensions. All the devices exhibit ohmic conduction with no conceivable memory window. Moreover, the resistance of these devices is very low (50Ω -180Ω) compared to the devices with hBN (92% of devices with resistance > 1MΩ). Therefore, we can ascertain that the resistive switching observed in this study can be solely attributed to the hBN layer.




**Supplementary figure 9:** DC IV characteristics collected from 12 different devices with a current compliance limit of 100uA.

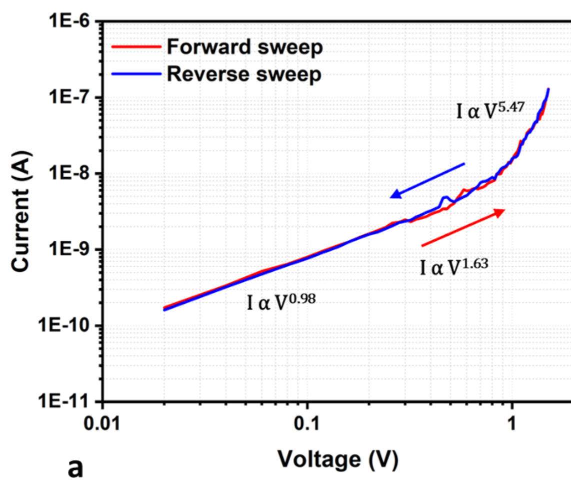
Variation in the device characteristics

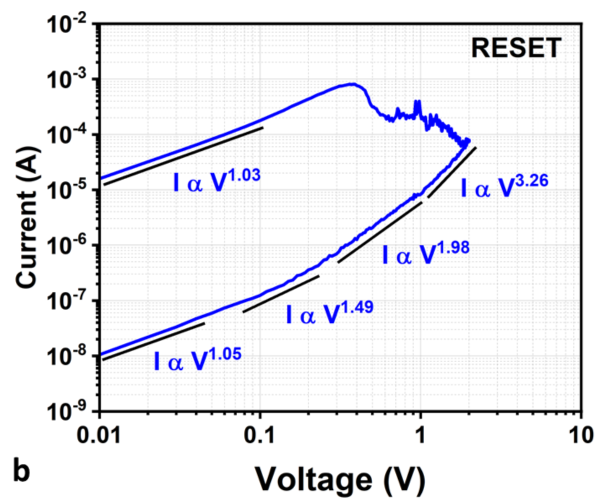
The voltage distribution presented in Fig.2c of the main text shows a larger variation for SET (1V to 3V) than RESET. To understand the source of this variation, we segregated the data to cycle-to-cycle and device-to-device components. From Supplementary figure.9, qualitatively, we observe that the cycle-to-cycle variation is lower than the device-to-device variation. To quantify this observation, we chose four devices and plotted their IV characteristics in Supplementary figure.10. Here, although the mean SET voltage varies considerably (between 1.2V and 2.54V), the distributions are relatively tightly bound around the mean value with a worst-case standard deviation of 0.25V. Whereas the standard deviation of the overall distribution (Fig.2c) is about 0.5V. This indicates that the device-to-device variation is the dominant cause of variation for these memristors.




**Supplementary figure 10:** (a-d) DC IV characteristics measured from four different memristor devices.

We speculate that the electrode surface roughness contributes to the higher device-to-device variation among these devices. Evaporated metal electrodes typically have a surface roughness of about 1-2nm [S16-S17]. The effect of this roughness on the switching characteristics should be lower in memristors with thicker switching layer (>5nm). However, as the switching layer thickness scales down, it is easier for filaments to propagate vertically and form around weak spots with bumps/hillocks. Therefore, the surface roughness of the electrodes will largely determine the location and voltage of the breakdown. These variations can be reduced with industry-standard tools that can achieve lower surface roughness, which is difficult to achieve with university equipment.

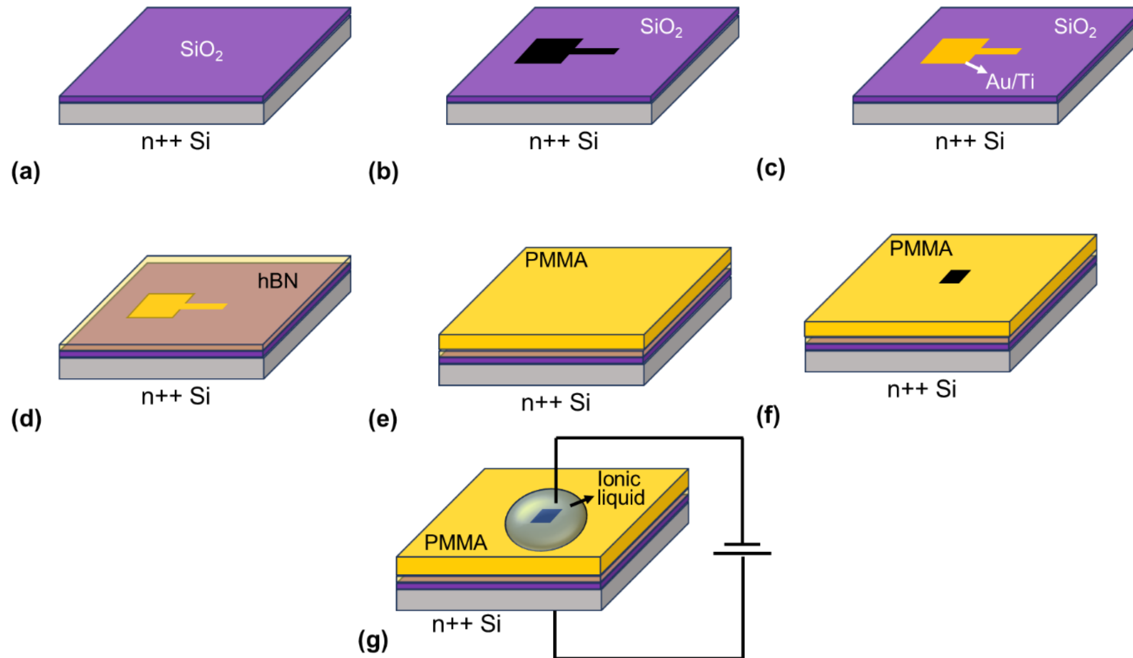



**Supplementary figure 11:** (a) DC current voltage sweep of a device in HRS. The reverse sweep (blue) traces the forward sweep (red) over the entire I-V range, indicating that the change in slope is caused by the transport mechanism inside the dielectric rather than the filament formation. (b) RESET I-V curve plotted on the log-log scale. The device exhibits linear conduction in the LRS and SCLC in the HRS.

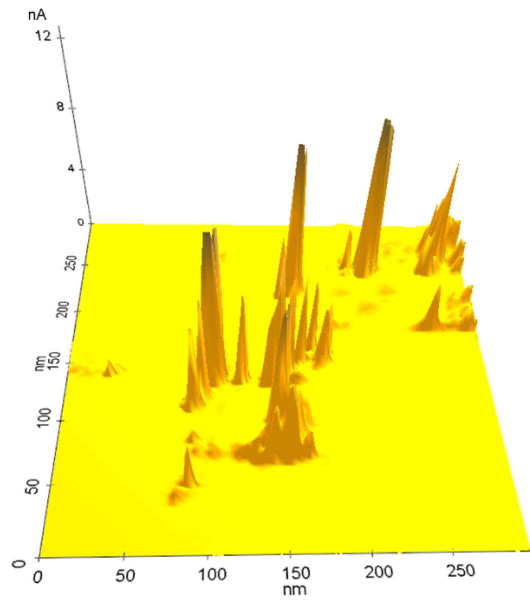
Conductive Atomic Force Microscopy

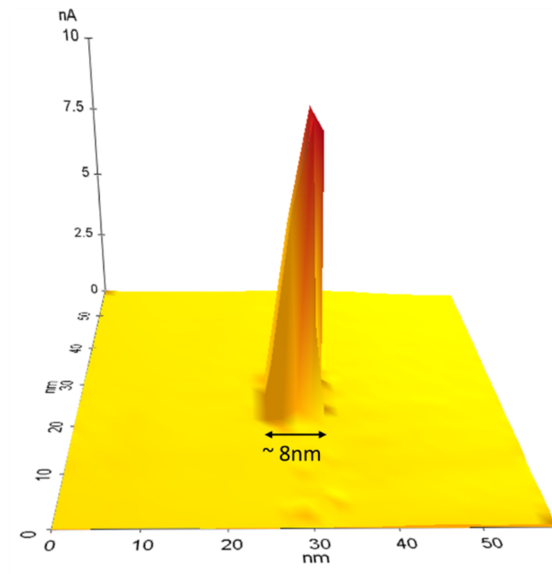
To confirm the proposed filamentary conduction mechanism, we performed Conductive AFM (CAFM) measurements on our devices. Sample preparation process flow and experimental setup are shown in the schematic below (Supplementary Figure 12.1). This approach of using ionic liquid for CAFM measurements was adopted from previous work [S18].



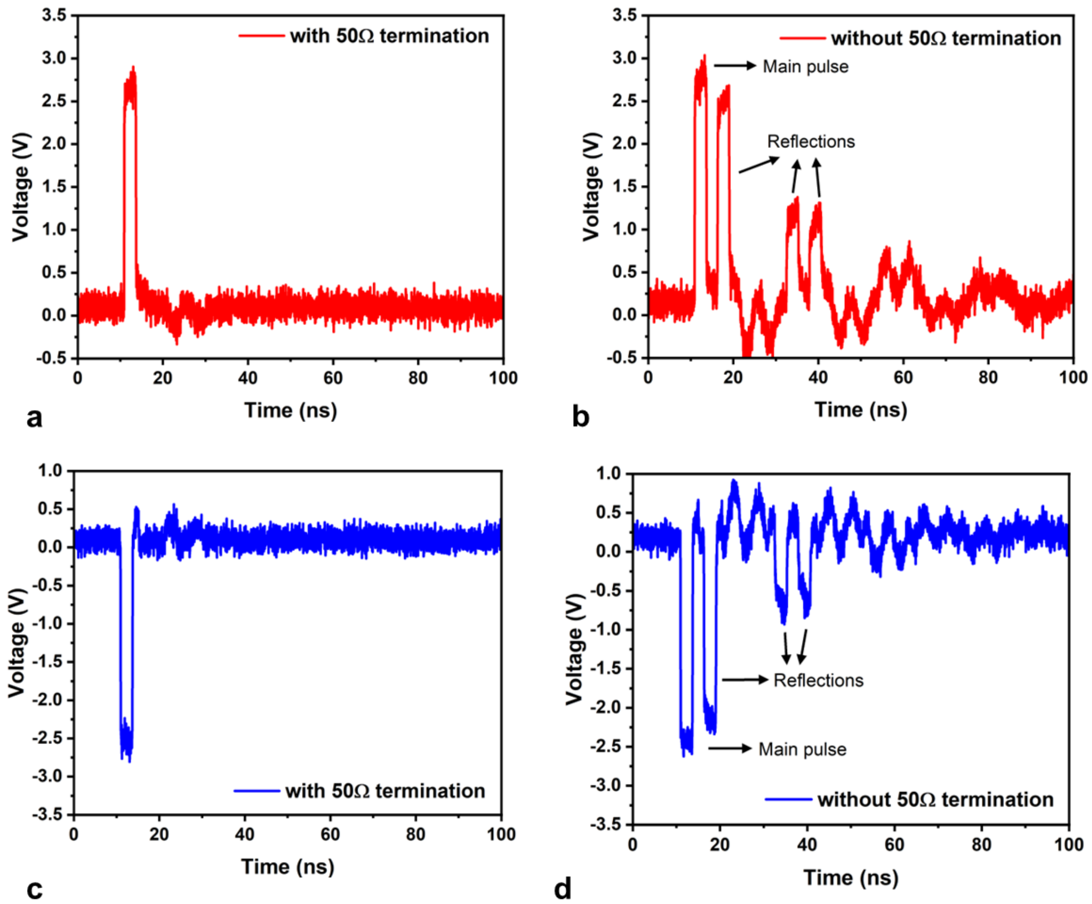

**Supplementary Figure 12.1:** Schematic showing the sample preparation process flow for Conductive AFM measurement. (a) Initial Si/$SiO_2$ substrate ($SiO_2$ thickness – 20nm) (b) Pattern and etch $SiO_2$ such that the Si surface is exposed (c) PVD deposition of Au followed by Ti (d) Transfer hBN film onto the bottom electrode (Ti comes in contact with hBN) (e) Spin coat PMMA layer (f) pattern and develop PMMA layer (small region 3x3um$^2$ exposed) (g) Drop ionic liquid (makes contact with hBN layer) and apply voltage bias.

The sample was prepared such that the titanium metal made contact with the hBN layer to emulate our device structure. Filaments were formed in the hBN layer by stressing the device as shown in Supplementary Figure 12.1(g) (positive voltage to the bottom electrode). After stressing the devices, the ionic liquid was washed away, PMMA was dissolved in acetone and then the samples were taken to CAFM for measurements. During the CAFM measurements, the AFM tip comes in contact with the hBN layer and the back-side silicon substrate is grounded. Large area scan (300nmx300nm) clearly shows the formation of conductive filaments (Supplementary Figure 12.2(a)) across the hBN layer. High resolution scan of a single conducting filament is presented in Supplementary Figure 12.2(b). Based on the CAFM and EELS measurements (Fig.2g, main text), we can conclude that the dominant switching mechanism in our devices originates from the formation/dissolution of Ti ion constituted conductive filaments.

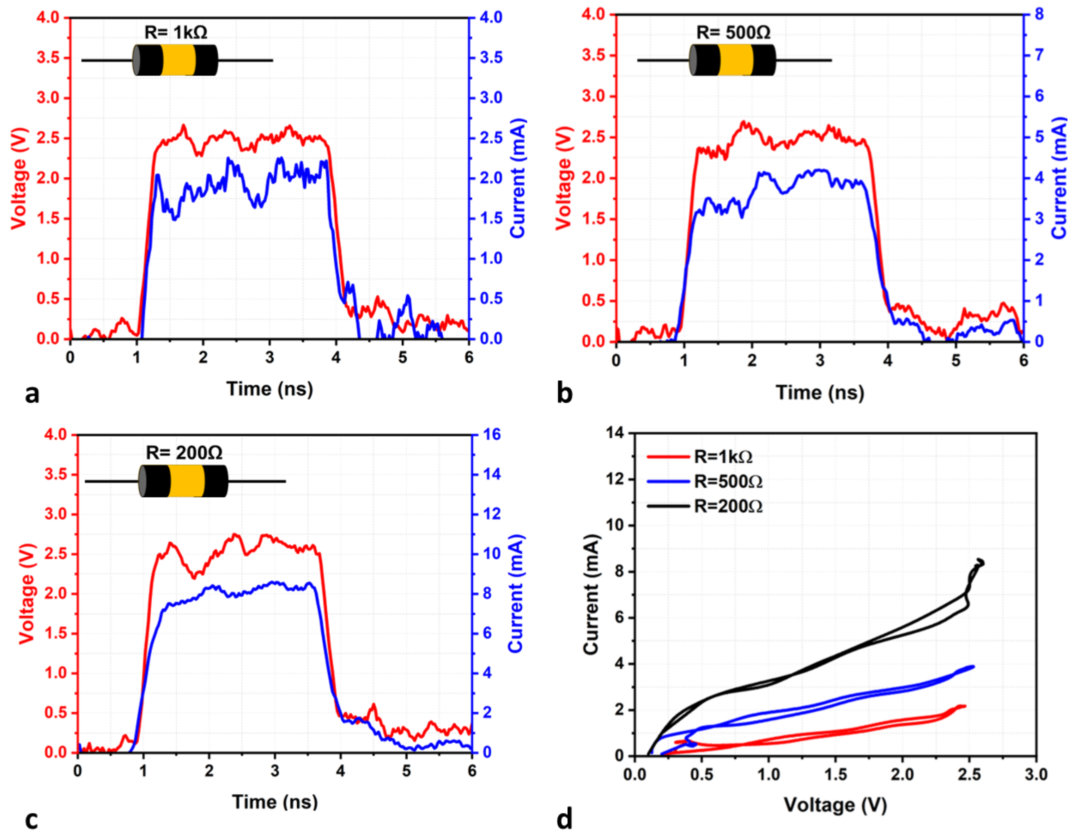


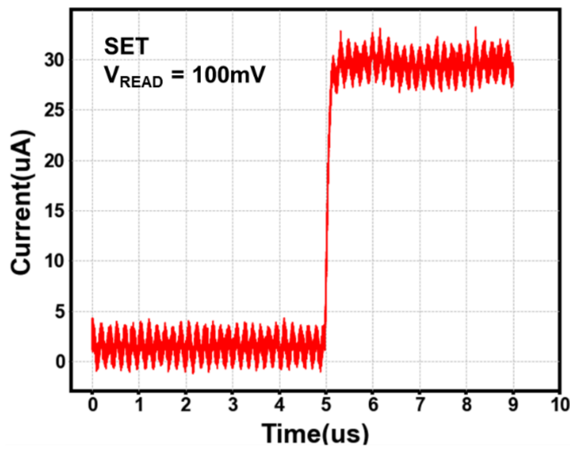

**Supplementary Figure 12.2:** (a) Large area CAFM current map showing multiple filaments (b) High resolution current map of a single filament.

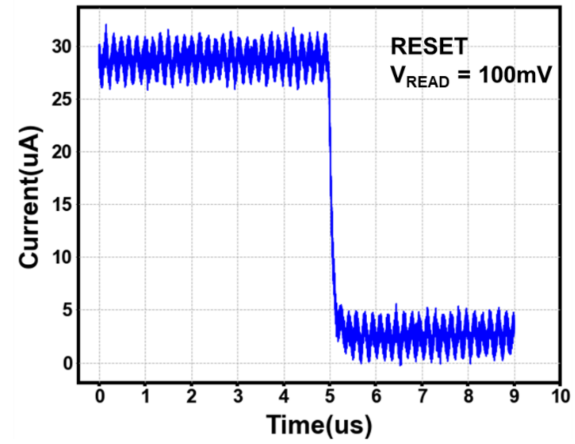



**Supplementary figure 13:** Transient waveform for SET pulse (a) with 50Ω termination (b) without 50Ω termination soldered onto the probe tips. RESET pulse (c) with 50Ω termination (d) without 50Ω termination soldered onto the probe tips. The 50Ω termination resistor effectively suppresses reflections and ensures maximum power transfer. Such reflections would result in random programming of the memristor. Therefore, all the experiments presented in this work were conducted with the 50Ω termination on the probe tips ensuring minimal reflected power.

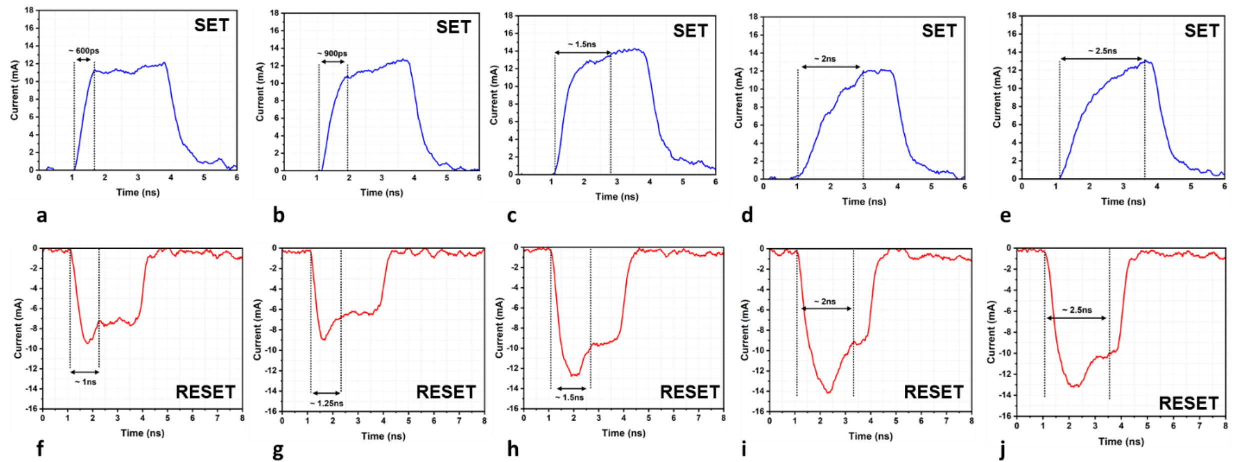



**Supplementary figure 14:** Applied voltage pulse (red trace) and measured current (blue trace) across a discrete surface mount resistor with the resistance (a) 1kΩ (red trace) (b) 500Ω (blue trace) (c) 200Ω (black trace). (d) I-V plots of the pulses are shown in (a),(b),(c). The graphs display no significant hysteretic window suggesting that the hysteresis in Fig. 3(c),(e) in the main text can be attributed to the resistive switching of the memristor rather than to setup parasitics.




**Supplementary Figure 15:** (a) Current signal measured on the DC path during a SET operation with a background DC offset of 100mV. Change in resistance is evident, confirming the resistive switching in the memristor device (b) Current signal measured during a RESET operation.




**Supplementary Figure 16:** SET current waveforms with intrinsic switching time (a) 600ps (b) 900ps (c) 1.5ns (d) 2ns (e) 2.5ns. The applied voltage signal is not included for clarity. RESET current waveforms with intrinsic switching time (f) 1ns (g) 1.25ns (h) 1.5ns (i) 2ns (j) 2.5ns.

Here the switching time is defined as the time taken for the current signal to settle to ~90% of its final magnitude. Most other studies do not include the rise time of the voltage pulse, and the switching time is usually reported as the time required to reach 50% of the final current magnitude. Though such characterization provides an attractive switching time estimate (results in $T_{SWITCH}$ < 1ns in our measurement), we believe that such an approach does not reflect a realistic scenario. Therefore, the switching time data provided in this study should be taken as a realistic estimate. Data extracted from 200 different traces have been used for further analysis in Figure 4,5 in the main text.

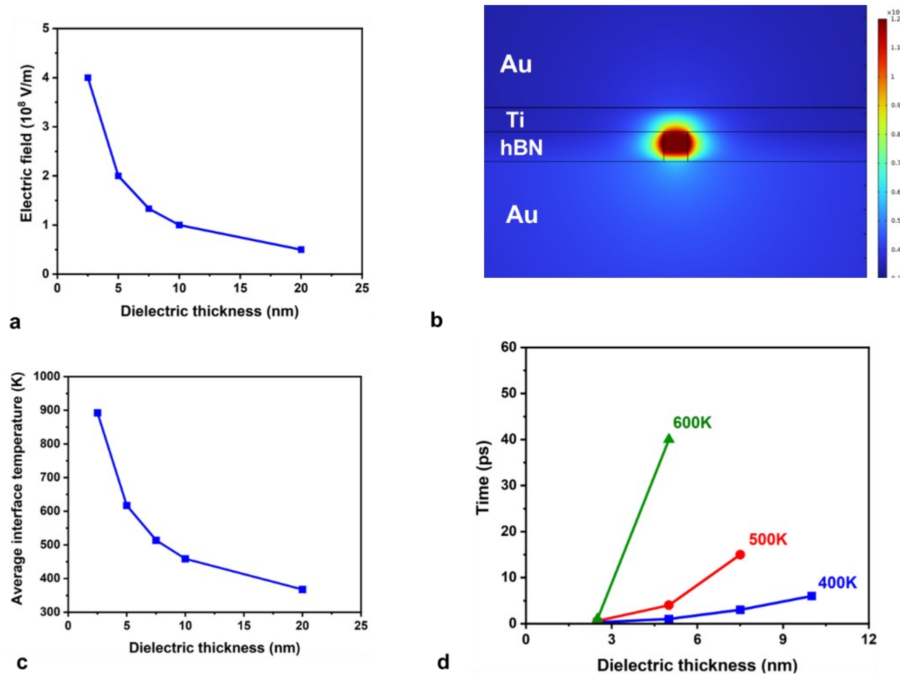
Ultra-fast switching in 2D memristors

The switching mechanism in our devices is based on metal ion diffusion into the switching layer. The applied electric field facilitates the vertical propagation of the filament around weak spots in the dielectric. This initially formed narrow filament connects the electrodes and lowers the resistance of the memristor. The current flowing through this filament generates temperature through the Joule heating phenomenon. The temperature generated in the filament lowers the energy barrier for ion release from the electrode and further propels the filament growth. To understand the fundamental reason for the ultra-fast switching in our devices, we perform transient thermal analysis using finite element based physics solvers (COMSOL). To summarize the results, the characteristic properties aiding the ultra-fast switching in 2D hBN memristors are:

1. Ultra-thin switching layer
2. High thermal conductivity of 2D hBN layers

Ultra-thin switching layer

Oxide memristors (commercial or university demonstrations) typically have a thicker switching layer (5nm-20nm) in comparison to the memristors in this study (< 2.4nm). The thinner switching layer significantly increases the local electric field across the dielectric, which promotes faster resistance switching. Supplementary Fig.17.1a shows the electric field increases inside the switching layer as the dielectric thickness reduces.



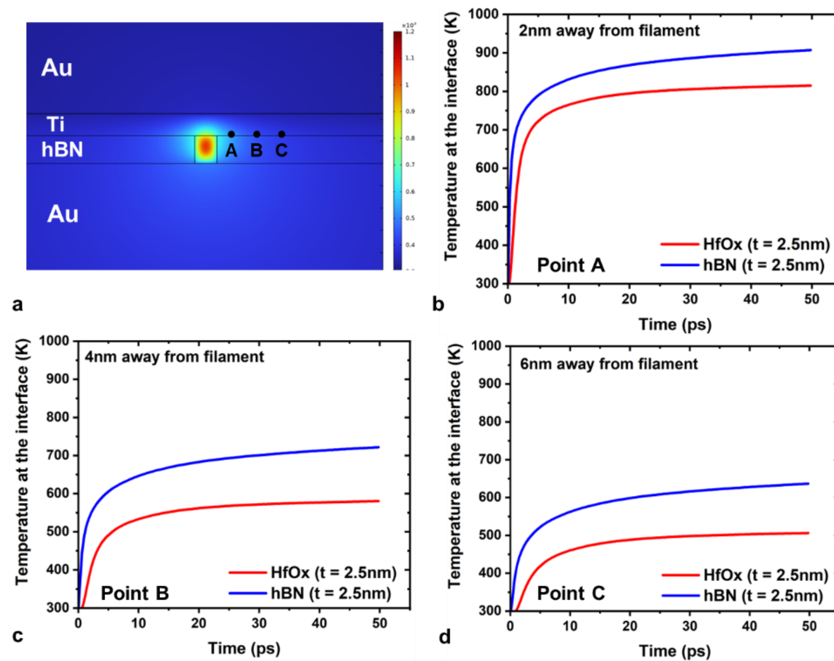

**Supplementary Figure 17.1:** (a) Electric field vs dielectric thickness for V=1V. (b) Snapshot of the COMSOL model showing the metallic filament and electrodes. The temperature profile shows the highest temperature at the center of the filament. (c) Temperature reaching the interface vs dielectric thickness (d) time taken for the interface to reach 400K (blue curve), 500K (red curve), 600K (green curve) as a function of dielectric thickness.

From the Arrhenius model [S19-S21], the filament growth dynamics depend on the temperature in addition to the applied voltage. The critical physical process that determines the switching speed of the device is the metal ion release [S19] which is determined by the Ti/hBN interface temperature ($T_{INT}$). Note that this temperature is different from the filament temperature ($T_{CF}$). The current passing through the device generates temperature in the filament ($T_{CF}$) through joule heating. This temperature is highest at the center of the filament (vertically) and lowers towards the electrodes, as seen in Supplementary Fig.17.1b. This type of temperature profile has been reported in several previous studies [S20-S22]. Most studies approximate $T_{CF} \sim T_{INT}$ for simplicity in analytical modeling.

Using the COMSOL model, we study the $T_{INT}$ dependence on dielectric thickness, as shown in Supplementary Fig.17.1c. It is evident that as the dielectric thickness reduces, steady-state $T_{INT}$ increases. In addition, Supplementary Fig.17.1d plots the time taken for temperature build-up at the interface as a function of dielectric thickness. We plot the time taken to reach 400K, 500K, and 600K for comparison. The $T_{INIT}$ for thinner dielectric (such as the devices in this study) reaches 600K in less than 1ps, whereas thicker dielectric ~5nm takes about 40ps. The faster temperature build-up at the interface promotes faster metal ion release, which creates a positive feedback loop: higher $T_{INT}$ → lower R → higher $T_{INT}$. This positive feedback loop promotes faster switching in devices with a thinner dielectric layer.

<u>High thermal conductivity of 2D hBN</u>

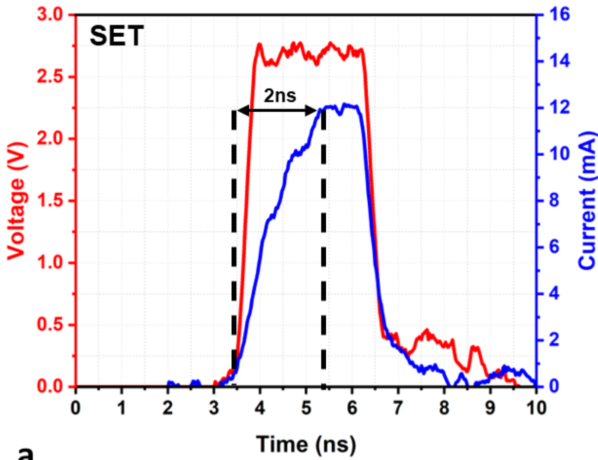
Based on the previous discussion, the obvious subsequent question would be - "Will the oxide RRAMs with thinner switching layer switch as fast as the 2D memristors?" To answer this question, we simulated two devices – one with an $HfO_x$ layer and the other with 2D hBN, with identical switching layer thicknesses (2.5nm).




**Supplementary Fig.17.2:** (a) Snapshot of COMSOL model showing three points of interest A,B,C. Transient interface temperature at (b) point A (c) point B (d) point C for HfOx (red curve) and hBN (blue curve).

In addition to thickness, another physical property that determines the switching speed of the devices is the thermal conductivity of the switching layer. The in-plane thermal conductivity of hBN (k ~ 100-200 W/mK) [S23-S25] is significantly higher than oxides (k ~ 0.5-2 W/mK) typically used for memristors ($HfO_2$, $Al_2O_3$, $TaO_x$) [S26-S28]. On the other hand, the out-of-plane thermal conductivity is comparable (~5 mW/K) to the oxides. The high thermal conductivity quickly spreads the heat from the filament to the surroundings, which heats a larger cross-section of the interface. Supplementary Fig.17.2a shows three points on the interface at 2nm,4nm, and 6nm away from the filament. Temperature transients at these points (Supplementary Fig.17.2 b,c,d) highlight this effect. Evidently, $T_{INT}$ increases rapidly for hBN compared to $HfO_x$. This effect is especially more pronounced as we move away from the filament (points B, C). Since a larger cross-section of the interface is heated, the probability of ion release increases, which results in faster filament expansion. Therefore, 2D materials that typically have higher thermal conductivity promote faster switching compared to oxide RRAMs with identical layer thickness.

Overall, the 2D memristors benefit from having an ultra-thin switching layer as well as high thermal conductivity compared to TMO memristors. Fig.4d (main text) shows the $T_{INT}$ for hBN devices with 2.5nm thickness and HfOx devices with 5nm thickness (typical thickness for TMO memristors). Clearly, the temperature rises rapidly for the hBN devices, resulting in ultra-fast switching.



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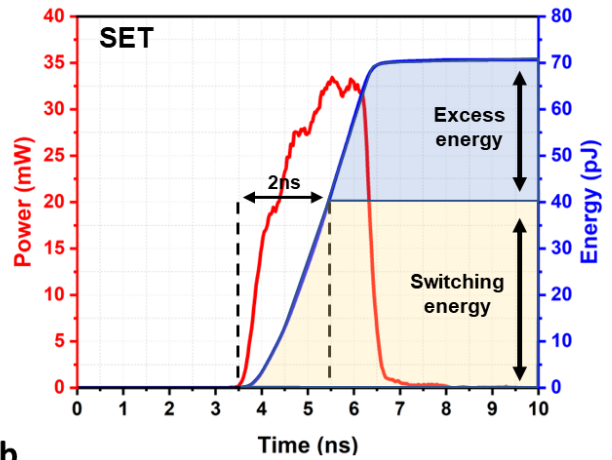

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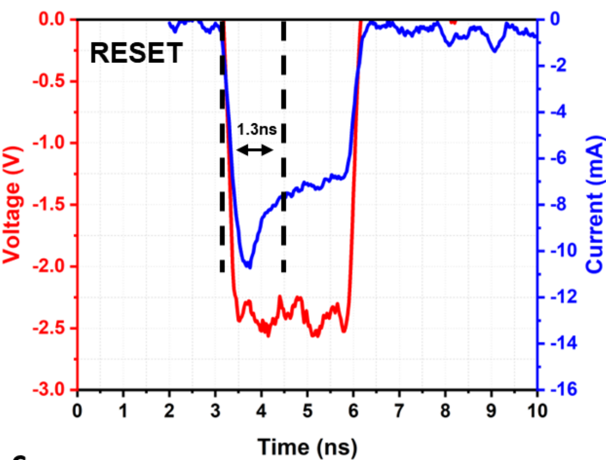

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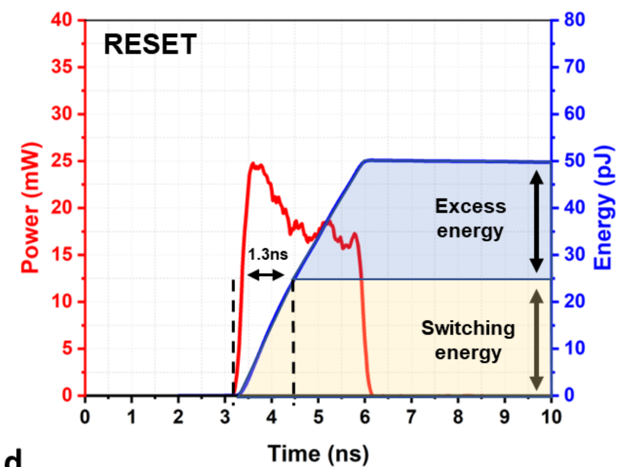
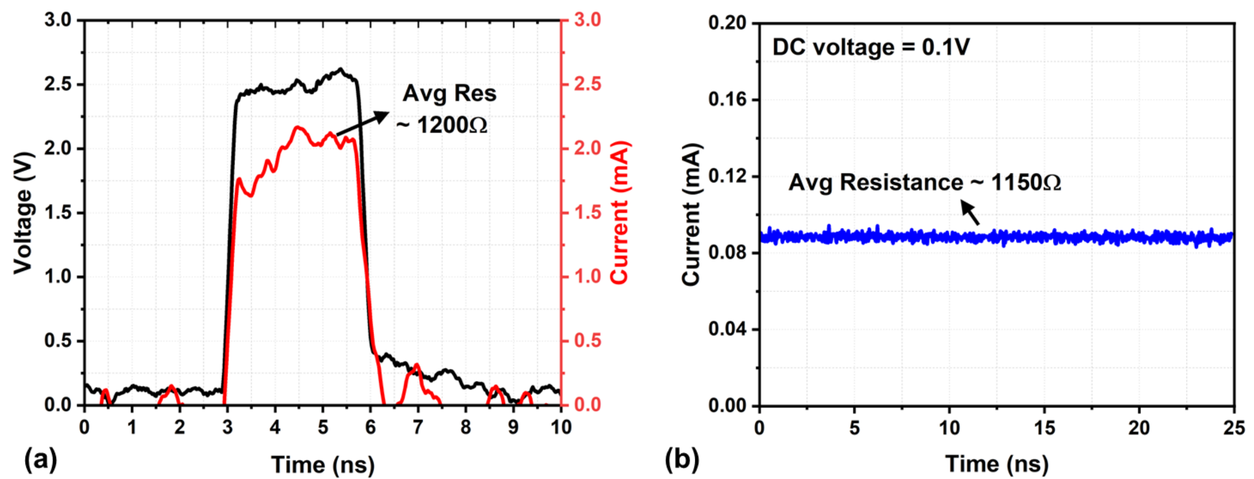


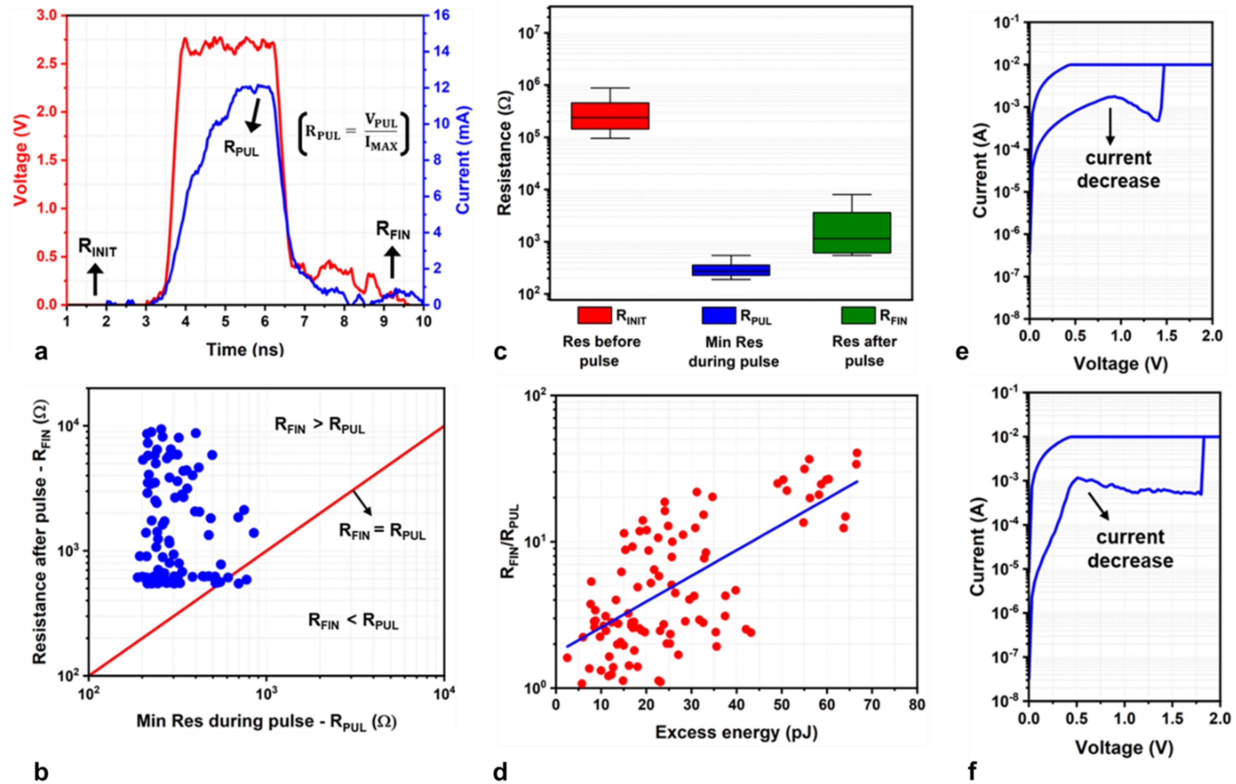
d

**Supplementary figure 18:** (a) Applied voltage pulse (red trace) and measured current (blue trace) in a SET transition. The device takes about 2ns to complete the transition to the final state (b) Power ($P = V * I$) consumed during the SET transition (red trace). The total energy obtained by integrating power over time ($E = \int P\, dt$) is shown in the blue trace. The total energy is partitioned into switching energy (energy contributed to switching) and excess energy (energy spent after the switching is complete), as discussed in the main text. (c) Applied voltage pulse (red trace) and measured current pulse (blue trace) for a RESET transition (d) Power and energy plots during the RESET transition.




**Supplementary figure 19:** (a) Transient voltage (black trace) and current waveforms (red trace) applied to a discrete resistor (b) DC current measured before and after the pulse for the discrete resistor.

As explained in the methods section, the resistance during the pulse is directly measured by the oscilloscope, whereas the resistance before/after the pulse is measured through a current amplifier in the branched DC path. Therefore, any additional resistance in the DC path can increase the resistance after the pulse. Supplementary Fig.19 shows that the resistance during and after the pulse measured close to 1.2kΩ. Therefore, the resistance increase observed after the pulse in Fig.5c (main text) is indeed a characteristic feature of the memristors associated with Joule heating.




**Supplementary Figure 20:** (a) Voltage (red trace) and current pulse (blue trace) waveforms during a SET operation. The resistance value is calculated at the maximum current magnitude during the pulse ($R_{PUL}$ - blue boxplot) and immediately before ($R_{INIT}$ – red boxplot) and after ($R_{FIN}$ – green boxplot) the pulse via applying small DC bias V=100mV (b) $R_{FIN}$ vs. $R_{PUL}$ collected from 100 transient traces in (a): The post-switching resistance $R_{FIN} > R_{PUL}$ in ~97% of the collected data points (c) Resistance distribution of $R_{INIT}$, $R_{PUL}$, $R_{FIN}$. The distribution clearly indicates the filament resistance increases after the pulse voltage is scaled down. This resistance increase should not be confused with the resistance relaxation observed in volatile resistive switching devices since the currents in this study (~6mA-12mA) are higher than the volatile switching devices current limits (<100uA) [S18,S29]. Therefore, the data suggest that the filament cross-section is reduced. (d) The post-switching resistance increase ($R_{FIN}/R_{PUL}$) correlates (weakly) to a higher excess switching energy, implying that high temperature may induce random ions migration away from the filament, which suppresses the filament conductivity (e), (f) DC I-V sweep showing current decrease during a SET pulse. These rare instances of current decrease occur when RESET does not sufficiently dissolve the filament, and a large current promotes its further thermal dissolution that is consistent with the suggestion in (d). Such Joule heating induced resistance increase in 2D hBN memristors has been previously reported [S30].

**Supplementary figure 21: Filament growth model**

The switching mechanism in our devices is based on titanium ion migration into the hBN layer that form filaments. The filament growth model based on Arrhenius relationship is a universally accepted phenomenological model that satisfactorily captures the growth dynamics in TMO memristors and CBRAMs (conductive bridge RAM) [S19, S31-S33]. Therefore, in this study, we employ the same model with modifications to capture the behavior of our 2D memristors under ultra-fast voltage pulse stresses. Based on this model, the time dependency of the filament growth can be described by,

$$\frac{d\Phi}{dt} = A_1\, e^{(-\frac{Ea0-\alpha qV}{kT_{CF}})} \qquad \text{---------- (1)}$$

where $\Phi$ → filament diameter

$A_1$ → pre-exponent factor

$E_{a0}$ → Activation energy for bond breaking and ion hopping

$\alpha$ → barrier lowering coefficient

$q$ → charge of electron

$V$ → voltage across the device

$k$ → Boltzmann's constant

$T_{CF}$ → conductive filament temperature

According to Eq.(1), the filament growth rate depends on the applied voltage as well as the temperature of the memristor device. Based on the equations presented in [S32], the thermal time constant of the filament can be calculated to be 0.226ps for our devices. As the thermal time constant is ~500x smaller than the input pulses ($T_{PULSE}$ ~ 120ps-3ns), any transient effects can be safely neglected. Therefore, the conductive filament temperature can be obtained by solving the steady-state Fourier heat equation.

The ramping voltage pulse facilitates the vertical propagation of the filament around weak spots in the dielectric. This initially formed narrow filament connects the electrodes and lowers the resistance, which increases the current in the memristor. The local temperature ($T_{CF}$), determined by Joule heating of the filament ($T_{CF} \propto V*I$), in turn, increases with current that further propels the filament growth. This self-accelerating process – larger $\Phi$ → larger I → larger T → larger $\Phi$ proceeds until the device enters a high current regime where secondary effects begin to manifest. In the high current regime (I>5mA), the external resistance $R_C$ (arising from contact leads) results in a voltage drop, thereby lowering the effective voltage across the device ($V_{DEV}$). In addition, $T_{CF}$ increases significantly in the high current regime, which increases the out-diffusion of ions from the filament, thus promoting the dissolution of the filament. The out-diffusion of ions from the filament can be modeled by,

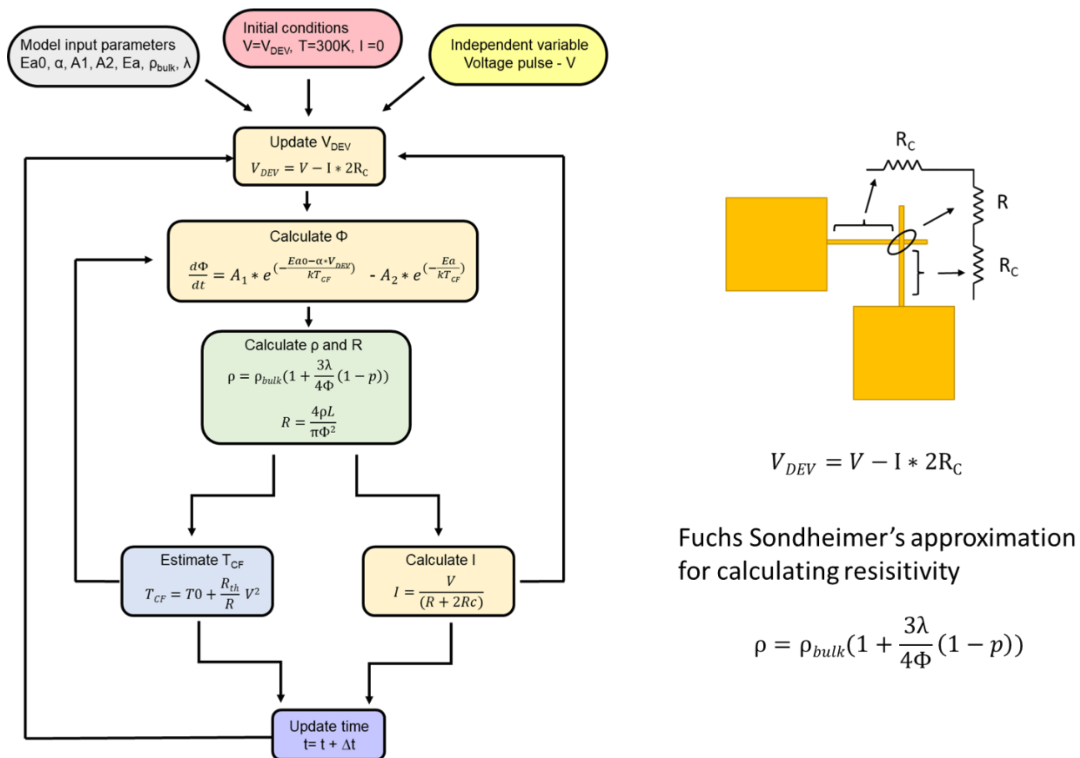
$$\frac{d\Phi}{dt} = -A_2 e^{(-\frac{Ea}{kT_{CF}})} \qquad \text{---------- (2)}$$

where Ea is an activation energy for out-diffusion of ions from the filament. The overall filament growth rate can be modeled by combining Eq.(1) and Eq.(2),

$$\frac{d\Phi}{dt} = A_1 e^{\left(-\frac{Ea0-\alpha qV}{kT_{CF}}\right)} - A_2 e^{\left(-\frac{Ea}{kT_{CF}}\right)} \qquad \text{--------- (3)}$$

The first term in Eq.(3) represents the filament growth due to ion diffusion from the Ti electrode and the second term describes the filament dissolution due to ion out-diffusion from the filament. During the switching energy phase, when the Joule heating is insignificant (low current in the memristor), the filament growth rate dominates, resulting in filament expansion. On the other hand, during the excess energy phase, when Joule heating is significant (high current in the memristor), the filament dissolution rate increases. Here, a stable equilibrium is established between filament growth and dissolution processes. The system restores back to the equilibrium state when disturbed. For example, let us assume that the second term in Eq.(3) begins to dominate, then the following events occur: $\Phi$ decreases → R increases → $T_{CF}$ decreases → $\Phi$ increases. This negative feedback loop ensures that the filament diameter and the corresponding current through the device saturate after reaching a certain maximum, as evident from Fig.3b in the main text. Finally, during the voltage pulse falling transition, the filament growth rate (determined by V, $T_{CF}$) recedes faster than the filament dissolution rate (determined only by $T_{CF}$), thereby resulting in the narrowing of the filament.

The time evolution of the filament can be calculated by self-consistently solving for conductive filament diameter ($\Phi$) and temperature ($T_{CF}$) as shown by the flowchart in Supplementary Fig.21.1,

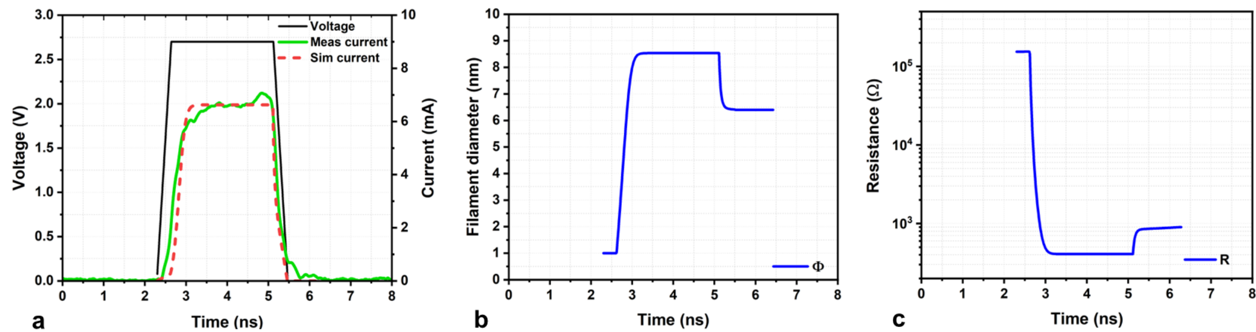



**Supplementary Figure 21.1:** Flowchart highlighting the sequence of equations providing the self-consistent solution.

The input parameters included in the model are listed in the table below. The transient voltage pulse is an independent variable to the model. The model iterates over time while calculating and updating Φ, R, $T_{CF}$, $V_{DEV}$ over each iteration using the following equations,

- Eq.3 for calculating Φ
- Fuchs-Sondheimer's approximation [S34] for calculating dimension dependent resistivity and corresponding resistance
- Fourier's steady-state equation for calculating $T_{CF}$
- Ohm's law to update $V_{DEV}$

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $E_{a0}$ | 1.2eV [S32] | $\rho_{bulk}$ | 42e-8 Ωm [S34] |
| α | 0.4 [S32] | λ | 28nm [S35] |
| $A_1$ | 1nm/s-10nm/s [S32] | p | 0.5 [S35] |
| $E_a$ | 0.3eV | $T_0$ | 300K |
| $A_2$ | 1nm/s – 10nm/s[S19] | $R_C$ | 20Ω-80Ω |



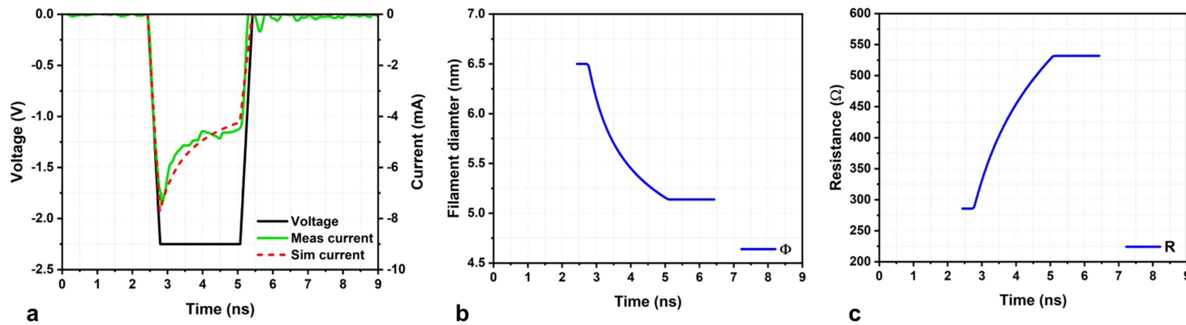

**Supplementary Figure S21.2:** SET Calculated time evolution of (a) I (b) Φ (c) R for a device with $T_{SWITCH}$=700ps (fig.3b in the main text). The model current (red trace) closely fits the measured current waveform (green trace) for an applied voltage pulse (black trace).

The self-consistent electro-thermal solver using the proposed model (red dotted trace) closely fits the measured data (green solid trace) (Supplementary Fig.21.2). In addition, the model also captures the filament narrowing. The filament expands to ~9nm in diameter and narrows to ~6.5nm after pulse termination. The memristor resistance change closely matches the resistance values observed in Fig.5c main text and Supplementary Fig.20. We believe that this joule heating driven filament narrowing will be observed in other 2D memristors as well, and therefore the proposed equations can be used to model them.

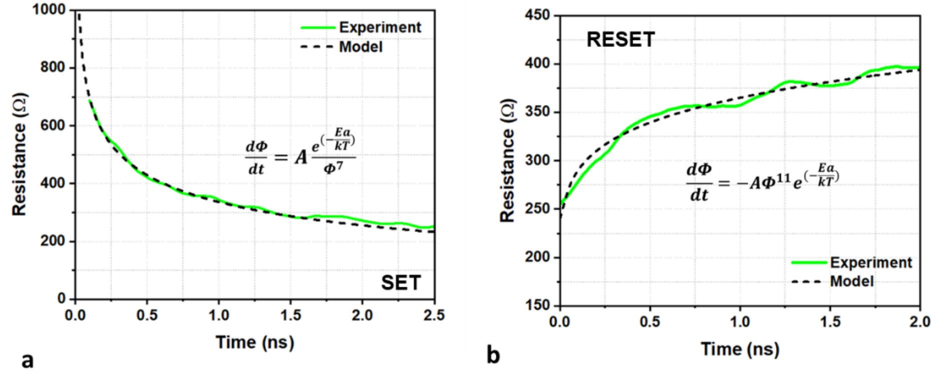
Similarly, the filament dynamics during RESET can be captured using Eq.4,

$$\frac{d\Phi}{dt} = -A_1 e^{\left(-\frac{Ea0-\alpha qV}{kT_{CF}}\right)} - A_2 e^{\left(-\frac{Ea}{kT_{CF}}\right)} \qquad \text{---------} \ (4)$$

Here, the term associated with Joule heating accelerates filament dissolution and aids the RESET process. The electro-thermal solver using the above equation closely models the measured RESET current signature as seen from Fig.S20.3a.




**Supplementary Figure S21.3:** RESET Calculated time evolution of (a) I (b) Φ (c) R for a device with $T_{SWITCH}$=1ns (fig.3d in main text). The model current (red trace) closely fits the measured current waveform (green trace) for an applied voltage pulse (black trace).




**Supplementary Figure 22:** (a) Resistance time dependency during SET operation (b) Resistance time dependency during RESET operation. The model (black dotted line) closely fits the experimental data (green solid line).

SET operation – Empirical model

The filament growth is modeled using the Arrhenius equation modified by including filament enlargement factor ($\Phi^n$) to account for growth rate deceleration process. This simple empirical model of resistance evolution over time assumes a constant temperature and, therefore, significantly reduces the computational time. Such models can be employed to study large array level performance metrics using SPICE circuit simulations. Supplementary Fig.22a shows the measured data (solid green trace) and simulations (black dotted trace) for the resistance time dependency: the growth rate of the filament diameter is accurately reproduced. The following equations are used in this model:

$$\frac{d\Phi}{dt} = \frac{A * exp\left(-\frac{Ea}{kT}\right)}{\Phi^n}$$

$$\Phi = (n+1)\left(A * \exp\left(-\frac{Ea}{kT}\right) * t\right)^{1/(n+1)}$$

$$R = \frac{4 * \rho * L}{\pi(n+1)^2 \left( A * \exp\left(-\frac{Ea}{kT}\right) * t\right)^{2/(n+1)}}$$

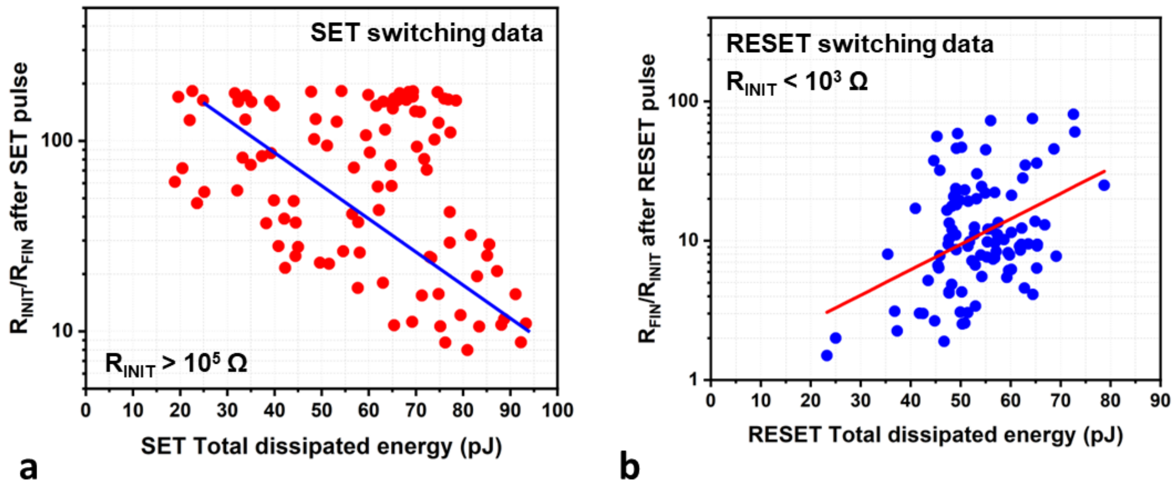
RESET operation – Empirical model

Like SET, the RESET operation also displays filament diameter dependent dissolution rate: the R(t) slope decreases as the filament dissolves. Supplementary Fig.22b shows the measured data (solid green trace) and simulations (black dotted trace) for the resistance time dependency: the model closely matches the measured data. The following equation are used in the model,

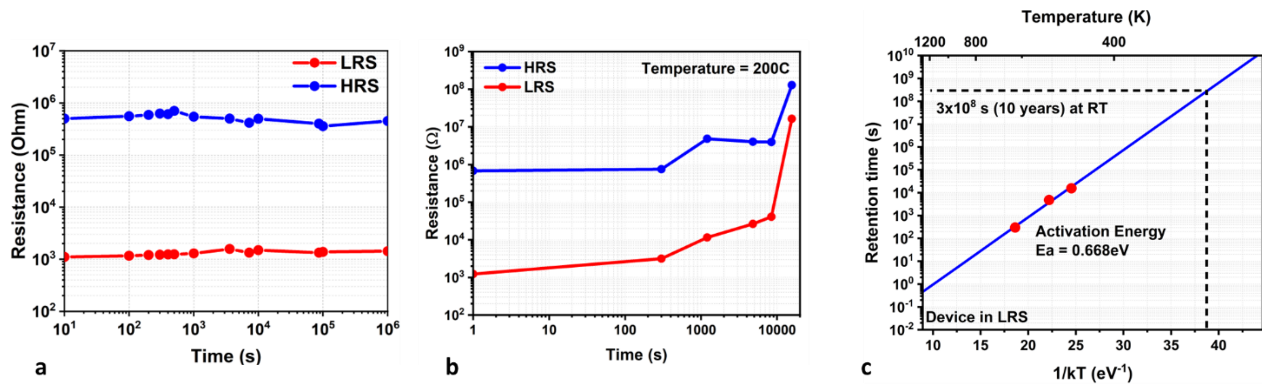
$$\frac{d\Phi}{dt} = -\Phi^n * A * exp(-\frac{Ea}{kT})$$

$$\Phi = \frac{1}{(n-1) * A * exp\left(-\frac{Ea}{kT}\right) * t + ((n-1) * \Phi_0)^{1-n}}$$

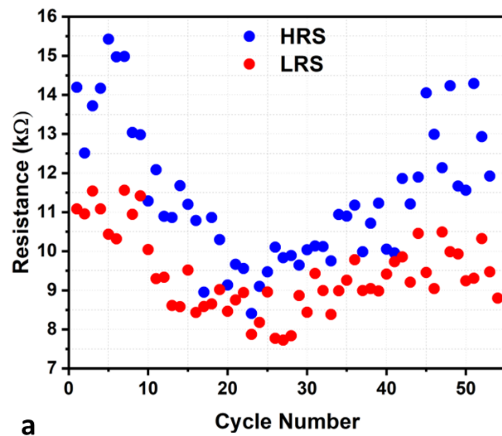
$$R = \frac{4 * \rho * L}{\pi}((n-1) * A * exp\left(-\frac{Ea}{kT}\right) * t + ((n-1) * \Phi_0)^{1-n})^{2/(n-1)} *$$

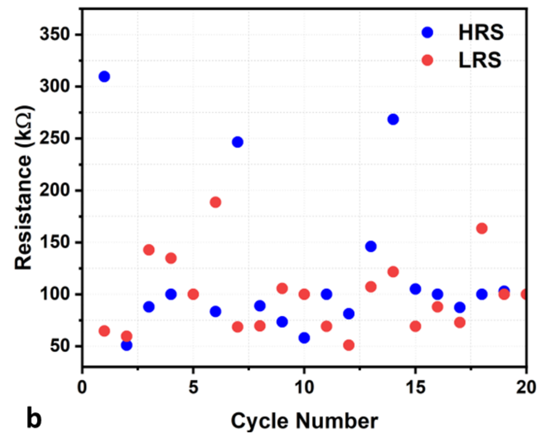



**Supplementary Figure 23:** (a) Relative resistance decrease after SET, ($R_{INIT}/R_{FIN}$) vs total energy (switching energy + excess energy). A downward trend indicates that the greater total energy results in smaller resistance decrease induced by a SET pulse. Higher energy dissipation (higher Joule heating) can suppress the filament by assisting with post-switching out-diffusion of metal ions, as discussed in Supplementary Fig. 20 (b) Relative resistance increase after the RESET pulse ($R_{FIN}/R_{INIT}$) vs total energy (switching energy + excess energy). An upward trend indicates that higher dissipation aids the RESET process resulting in larger resistance increase.

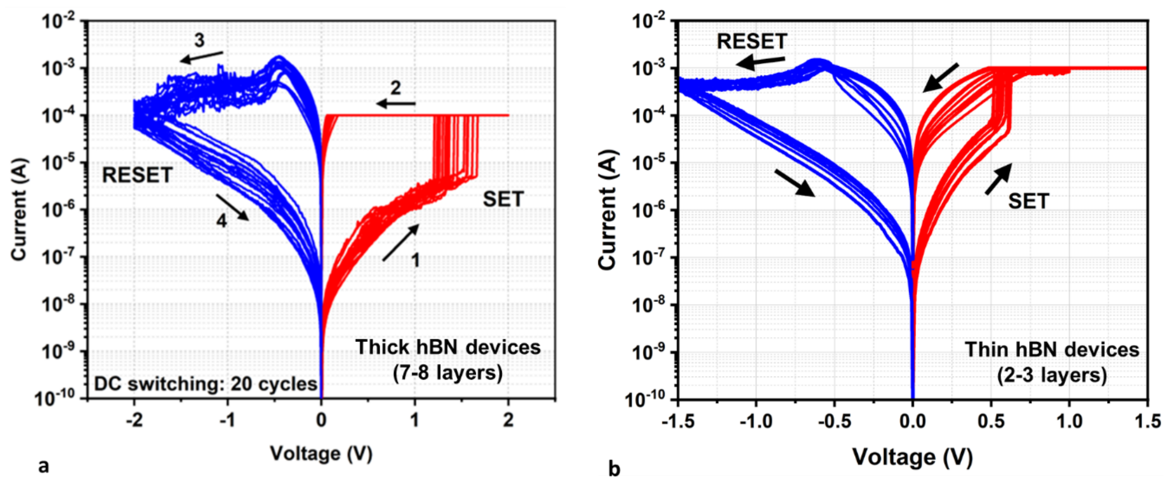



**Supplementary Figure 24:** (a) Retention measurement at room temperature. Devices retain their state with minimal drift in characteristics up to $10^6$ seconds (11 days). The measurement was discontinued after 11 days. (b) Memristor retention at 200C. Resistance increases over time (both in LRS (red curve) and HRS (blue curve)) confirming the role of heat in filament dissolution (c) LRS retention time at different operating temperatures. The LRS retention time shows an exponential dependence on the temperature, characterized by an activation energy of 0.668eV. Extrapolation shows that the device could retain the state for 10 years at room temperature.




**Supplementary Figure 25:** (a)(b) Endurance cycling with ultra-short pulses ($T_{PULSE}$ ~ 120ps) for thick hBN film (~ 7-8 layers). HRS data points shown in blue and LRS data points shown in red. Switching is inconsistent, no clear memory window is observed contrary to thin hBN film devices (Fig. 6c in main text).




**Supplementary Figure 26:** (a) Representative DC I-V characteristics of a thick hBN device (7-8 layers) and (b) a thin hBN device (3-4 layers). SET curves shown in red and RESET curves shown in blue. Thin hBN devices do not require a forming process to establish the initial conductive filament and have a smaller memory window compared to thick devices.

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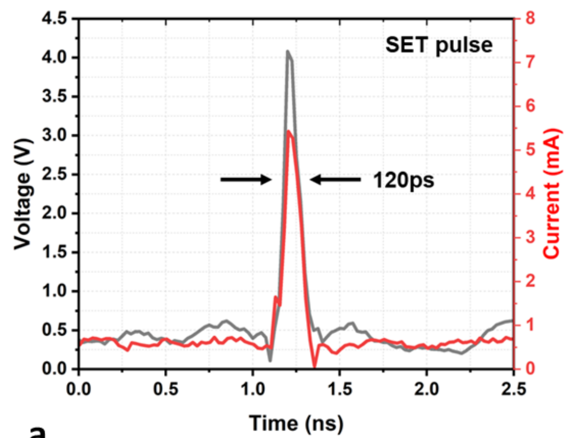


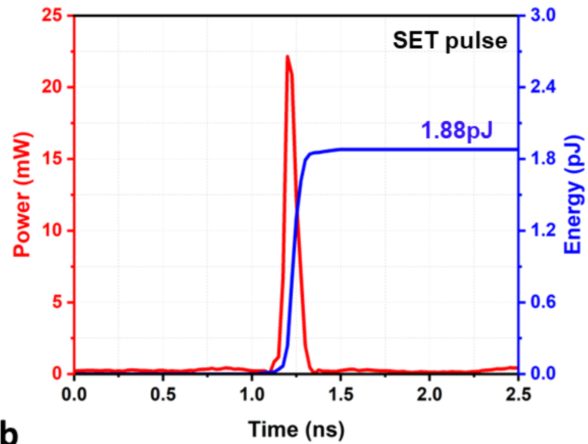


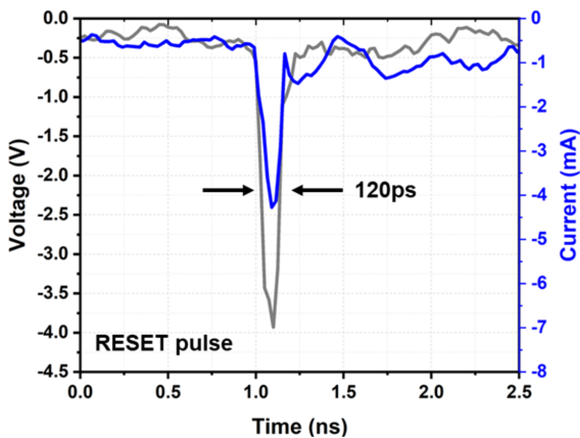


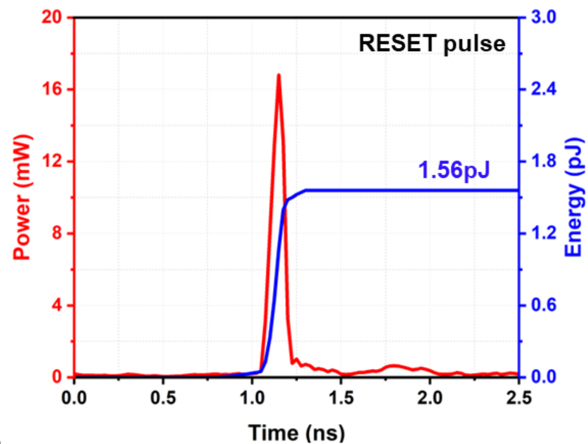


**Supplementary Figure 27:** (a) Ultra-short voltage pulse (grey trace) and measured current (red trace) during SET transition. The resolution of the measurement setup (~25ps) allows only up to 4-5 data-points to be captured during the pulse stress that limits our ability to identify transient current features (similar to nanosecond pulses in Figures 3,4,5 in the main text). The switching is confirmed by the DC read operation after the pulse (b) Instantaneous Power (red trace) and energy dissipated (blue trace) during SET transition. The energy of < 2pJ is among the lowest reported switching energy in 2D material memristors (c) Ultra-short voltage pulse (grey trace) and measured current (blue trace) during the RESET transition (d) Power and energy dissipated during the RESET transition.

|  |  | Material | Switching time | Number of cycles presented | Reference |
|---|---|---|---|---|---|
| 1 | Transition Metal Oxide | Yitrium Iron Garnet | 540ps | 20 | S36 |
| 2 |  | $HfO_x$ | 400ps | 1 | S37 |
| 3 |  | $HfO_2$ | 100ps | 1 | S38 |
| 4 |  | AlN | 85ps | 1 | S39 |
| 5 |  | HfOx | 300ps | 1 | S40 |
| 6 |  | $SiO_2$ | 105ps | 10 | S41 |
| 7 |  | $TaO_x$ | 100ps | 1 | S42 |
|  |  | $TaO_x$ | 250ps | 1 | S43 |
| 8 | 2D Material | $MoTe_2$ | 5ns | 1 | S44 |
| 9 |  | $MoS_2$ | 15ns | 1 | S45 |
| 10 |  | $MoS_2$ | 700ps | 1 | S46 |
| 11 |  | $MoS_2$ | 15ns | 1 | S47 |
| 12 |  | $MoTe_2$ | 100ns | 1 | S48 |
|  |  | hBN (this work) | 1.43ns | 600 | - |
| 13 |  | hBN (this work) | 120ps | 100 | - |

**Supplementary Table1 –** Comparison of switching times with previously published reports. The table includes fastest reported switching data from well-studied TMO memristors as well as emerging 2D memristors. The devices reported in this study outperform 2D memristors in terms of both speed and endurance.

Although a few studies report higher endurance at 100ps switching speed [S49-S50], they employ program-verify scheme during endurance cycling. In this approach, the device is subjected to repeating pulses until the desired transition (SET and RESET) is completed and several cycles may involve multiple pulses for successful operation. For the evaluation consistency, such studies have been omitted from this analysis. Moreover, if the device requires multiple pulses (even on a few instances), the switching speed cannot be reliably characterized.

Endurance in 2D memristors

The endurance in 2D memristors has been a concern, mainly attributed to the ultra-thin switching layer. Transition metal oxide (TMO) based memristors typically have a switching layer thickness ranging between 5nm-20nm [S51-S53]. On the contrary, 2D memristors typically have ultra-thin switching layers, sometimes even scaled down to monolayer thickness. The reduced vertical separation between metal electrodes enhances the electric field, which results in weaker control over the metal ion migration into the switching layer and subsequent filament formation. Moreover, as the thickness of the switching layer reduces, the impact of bottom/top electrode roughness plays a significant role in determining the overall device performance. In the following table, we have listed the reported endurance in 2D memristors along with the thickness of the switching layer.

| | Switching layer stack | Thickness (nm) | Cycles endurance |
|---|---|---|---|
| [S54] | Au/hBN/Au | 0.33 | 50 |
| [S55] | Au/$MoS_2$/Au | 0.65 | 20 |
| [S56] | Au/$MoS_2$/Au | 0.65 | 150 |
| [S57] | Ag/$hBNO_x$/Gr | 0.9 | 100 |
| [S58] | Au/$ReSe_2$/Au | 1 | 200 |
| [S59] | Cu/$MoS_2$/Au | 1.4 | 20 |
| [S60] | Ti/hBN/Au | 2.4 | 100 |
| [S61] | Ti/hBN/Au | 2.4 | 100 |
| [S62] | Ti/hBN/Ni | 3.96 | 100 |
| [S63] | Ti/hBN/Au | 4.3 | 50 |
| [S64] | Ti/hBN/Au | 4.95 | 250 |
| [S65] | Ti/hBN/Gr | 5 | 1000 |
| [S66] | Au/$MoS_2$/Au | 5 | 120 |
| [S67] | Au/hBN/Au | 6 | 50 |
| [S68] | Pd/$WS_2$/Pt | 6.45 | 15 |
| [S69] | Ti/hBN/Au | 6.6 | 1200 |
| [S44] | Ti/$MoTe_2$/Au | 7 | 600 |
| This work | Ti/hBN/Au | 2.5 | 600 |
| This work | Ti/hBN/Au | 1.32 | 100 |

**Supplementary Table 2 –** Comparison of reported endurance in 2D memristors.

From the table, we see that the 2D memristors with switching layer thickness <5nm, typically exhibit <250 cycles endurance. Some memristors [S65,S69] exhibit about 1000 cycle endurance with >5nm switching layer thickness. Our devices exhibit on-par performance with 600 cycles for thicker ($T_{hBN}$~ 2.5nm) memristors and 100 cycles for thinner ($T_{hBN}$~ 1.32nm) memristors.

On the other hand, only two research studies report high endurance (~$10^7$) using thicker 2D memristors [S70-S71]. Many studies report low endurance even with thicker 2D memristors [S72-S74].

Role of Current Compliance (CC)

A recent study [S75] reported high endurance of ~$10^6$ cycles in the 1T1M (1transistor-1memristor) bitcell with just ~6.6nm thick switching layer. In that study, the standalone devices without CMOS transistors exhibited only 100 cycles, whereas devices with transistors exhibited a million cycles. This promising result suggests that the adjoining selector device can improve endurance in 2D memristor devices.

The characterization setup utilized in this study cannot support external current compliance (CC) for high-frequency pulse testing. For the frequency range studied in this article, the external CC device (resistor, diode or transistor) must be located within <1cm distance from the DUT (device under test) to avoid refelctions. Therefore, the only possible option is to have a CC device fabricated monolithically, like in [S75]. Without current compliance, most of our devices get shorted during testing, which cannot be recovered. We expect that having a 1T1M configuration would improve the endurance of our devices as well.

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