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Scalable algorithm simplification using quantum AND logic

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Supplementary Information for "Scalable algorithm simplification using quantum AND logic"

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CONTENTS

I. LOGIC CIRCUIT CONSTRUCTION USING QUAND

In the main text, we have shown the efficient decomposition for multi-qubit controlled-Z (n-CZ) using the QuAND gate, which extends the classical AND logic to qubits. Basically, any multi-qubit controlled-unitary (CU) gates can be implemented efficiently in a same three-step procedure: embedding, controlled-unitary, and recovery (Fig. S1a). Figure S1b and S1c also show alternative way to synthesize generalized Toffoli and Fredkin gate (controlled-SWAP), which are important quantum logics.

Since our QuAND gate is a quantum implementation of AND logic leveraging ancilla level and since NAND gate is universal in classical circuit, all classical logic circuits can be efficiently constructed by adapting classical circuit optimization techniques with single-qubit, two-qubit CZ and QuAND gates. In fact, compared to the traditional Toffoli decomposition scheme, our scheme requires fewer ancilla qubits and gate operations. The QuAND gate is readily applicable to a large category of circuits and useful in simplifying circuit synthesis. Here we show three examples of leveraging QuAND gates for efficient synthesis of basic arithmetic circuits.

Figure S2 shows an efficient decomposition for incrementer using QuAND. The first half of the circuit – a sequence of QuAND gates – computes the carry information. The second half – a sequence of CNOT and reverse QuAND gates – recovers the original binary encoding and completes the incrementation. Figure S3 shows an efficient decomposition for constant adder using QuAND. The first half of the circuit – a sequence of G_0 or G_1 (constructed by QuAND and single-qubit X gates) gate depending on the corresponding bit value of b – computes the carry information. The second half of the circuit – a sequence of reverse G_0 or reverse G_1, and CNOT gates – recovers the original binary encoding and completes the addition operation. Figure S4 shows an efficient decomposition for adder using QuAND, as inspired by [1]. The M gate – constructed by QuAND and CNOT gates – computes the majority function and the carry information. The U gates undo the M gates and complete the addition of the two integers.

Depth of these circuits may be further reduced on topology with higher connectivity by the carry-lookahead technique. Other arithmetic and boolean logic circuits can be constructed in a similar way that replaces AND gates in classical circuits with QuAND gates.

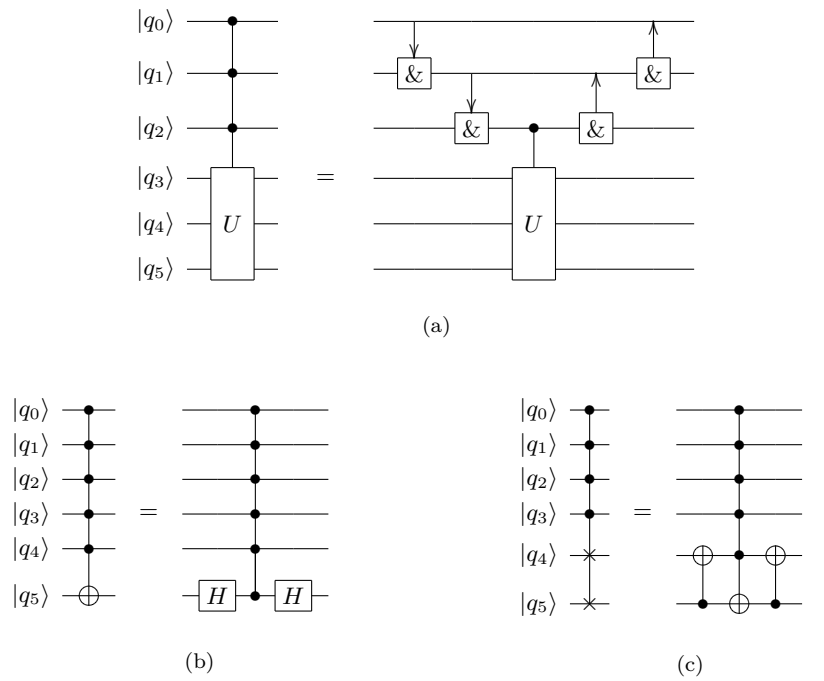


FIG. S1. **Circuit decomposition of generalized Fredkin gate. (a)** A circuit decomposition of multi-qubit controlled-U gate (left) using using QuAND, reversal QuAND and controlled-U gates (right).**(b)** A circuit decomposition of multi-qubit Toffoli gate (left) using n-qubit CZ and Hadamard gates (right).**(c)** A circuit decomposition of generalized Fredkin gate (left) using n-qubit Toffoli and CNOT gates.

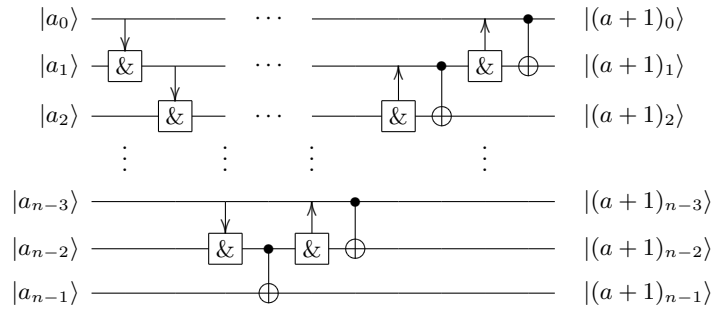


FIG. S2. **A circuit decomposition of incrementer using QuAND.** The n-qubit binary input $|a\rangle = |a_{n-1}\dots a_1 a_0\rangle$ is incremented to $|a+1\rangle$ at the output. The subscript indicates the index of the binary digit.

II. MULTI-QUBIT TOFFOLI DECOMPOSITION

To compare different schemes for synthesizing n-qubit Toffoli gate, we list relevant references and their main properties in Table.S1 for all-to-all connection and in Table. S2 for 1-D chain topology.

In prior works, multi-qubit Toffoli gate can be decomposed to qubit-only circuit with linear circuit depth and size by using ancilla qubits. The textbook approach [2] reduces a big Toffoli to standard (3-qubit) Toffoli and costs $n-2$ ancilla qubits for concatenating the AND results. He et.al.[3] provides a way to trade off between the number of ancilla qubits and circuit depth, but requires additional cost for feedback control or large constant factor. A similar approach from Barenco et.al.[4] uses the last control qubit as ancilla, saving ancilla qubit at the cost of circuit depth. Other works have focused on simplifying n-qubit Toffoli by ancilla levels. Ralph et.al.[5] and Lanyon et.al.[6] utilizes n-level qudit system to achieve $2n$ circuit depth and size by swapping the target state out of qubit space when the control qubits are not $|1\rangle$. Gokhale et.al.[7] and Inada et.al.[8] proposes leveraging qutrit control to achieve at most $2n$ circuit depth and size. In particular, Gokhale et.al. [7] proposes a novel approach which utilizes $|2\rangle$ state for storing the AND result of control qubits and propagate the results with Toffoli-like gate conditioned on $|2\rangle$ state, achieving logarithmic depth.

In our scheme, the circuit depth and size are both in line with the best value from previous works. However, it

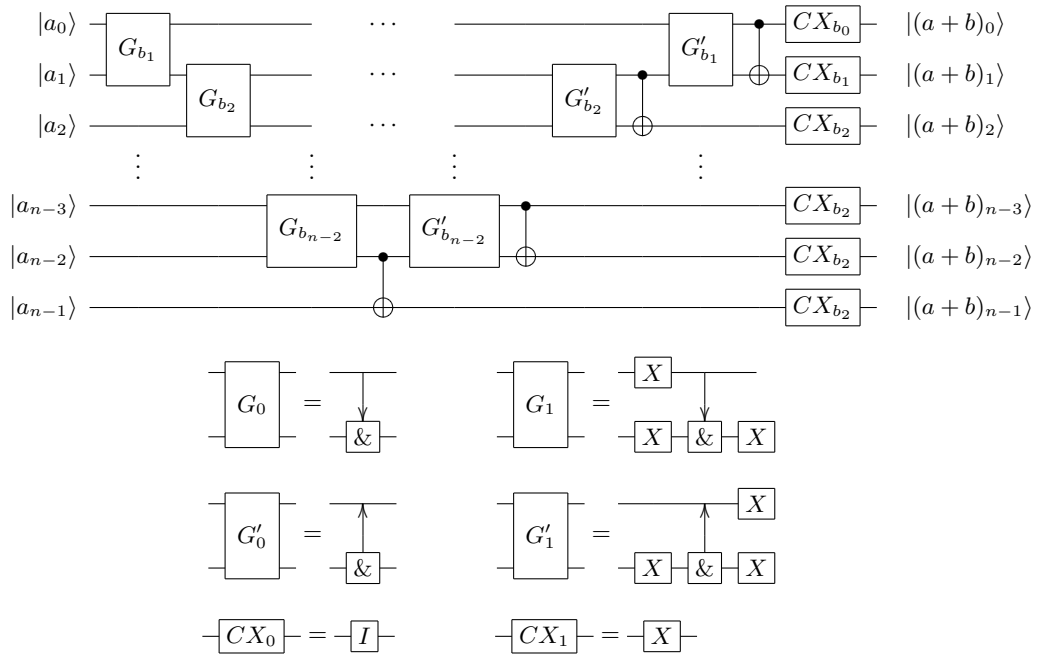


FIG. S3. **A circuit decomposition of constant adder using QuAND.** The n-qubit binary input $|a\rangle = |a_{n-1}\dots a_1 a_0\rangle$ is added by a known constant integer $b = b_{n-1}\dots b_1 b_0$ ($b_0 = 1$) at the output.

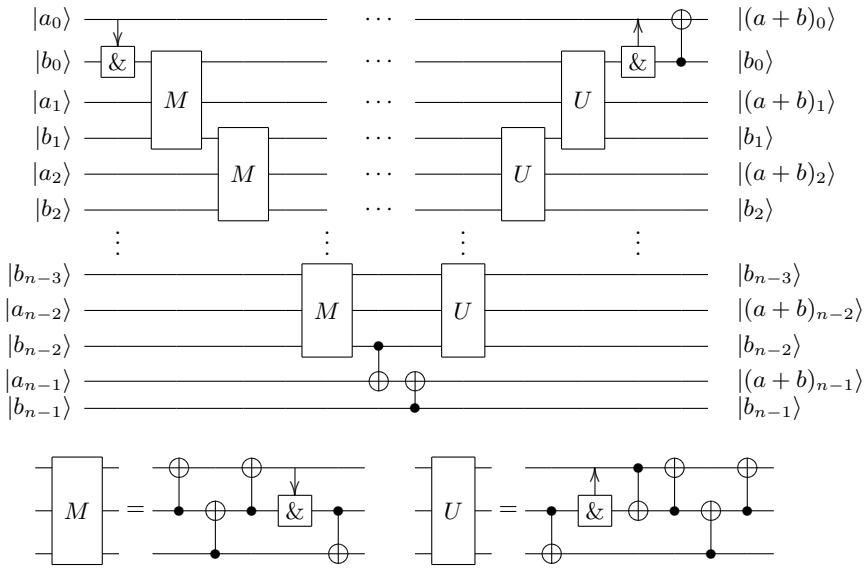


FIG. S4. **A circuit decomposition of adder using QuAND.** Two n-qubit binary inputs, $|a\rangle = |a_{n-1}\dots a_1 a_0\rangle$ and $|b\rangle = |b_{n-1}\dots b_1 b_0\rangle$, are summed up at the output.

requires only one additional operation with the ancilla level, i.e. the $|11\rangle\langle 20| + |20\rangle\langle 11|$ SWAP gate, which is naturally available in state-of-the-art hardware. The scheme features resource-efficient implementation in the sense that it is low-depth, free from ancilla qubits, and simple in control. These advantages plus compatibility with state-of-the-art hardware are the key to our successful realization of the large-scale multi-qubit Toffoli gate and Grover's search algorithm.

Our scheme shows better scalability on qubit arrays with higher connectivity. The circuit depth can be reduced to $2\sqrt{n}$ on a 2-D square array and to $2\log_2 n$ on a binary tree, as shown in Fig. S5.

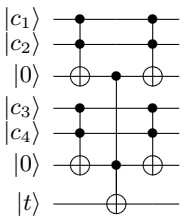
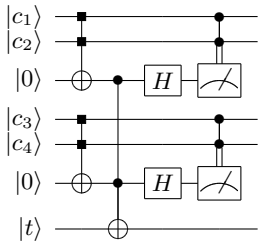
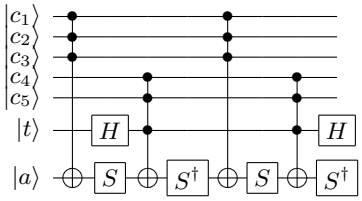
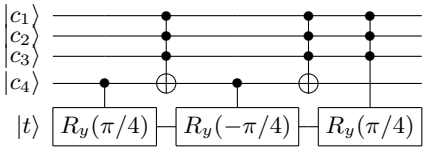
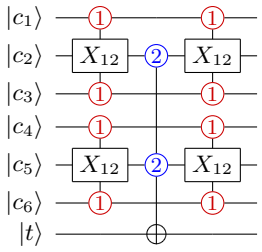
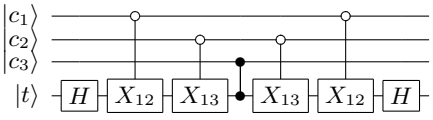
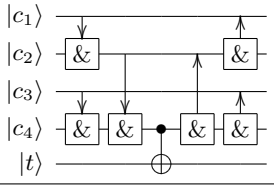
	Depth	Size	Constant	Ancilla qubits	Control Requirement	Intuition
Nielson and Chuang [2]	$\log_2 n$	n	12	$n-2$	Qubits	
He et.al. [3]	$\log_2 n$	n	4	$n-2$	Qubits	
He et.al. [3]	n	n	24	1	Qubits	
Barenco et.al. [4]	n^2	n^2	48	0	Qubits	
Gokhale et.al. [7]	$\log_3 n$	n	2	0	Three-Qutrit control	
Ralph et.al. [5, 6]	n	n	2	0	n-level Qudit control	
This work	$\log_2 n$	n	2	0	$\|11\rangle\langle 20\| + \|20\rangle\langle 11\|$	

TABLE S1. **Comparison of multi-qubit Toffoli gate decomposition assuming all-to-all connectivity.**

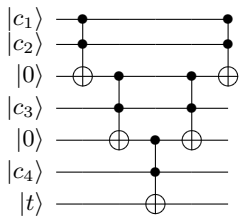
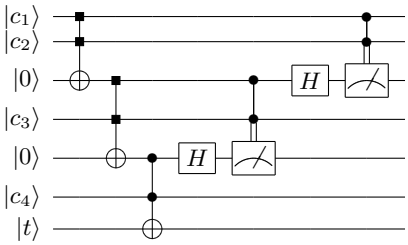
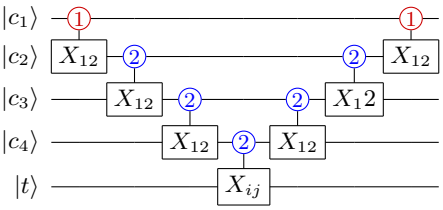
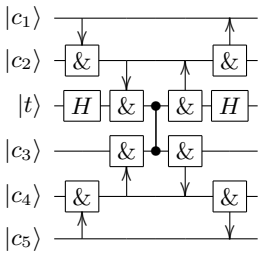
	Depth	Size	Constant	Ancilla qubits	Control Requirement	Intuition
Nielson and Chuang [2]	n	n	> 12	$n-2$	Qubits	
He et.al. [3]	n	n	> 4	$n-2$	Qubits	
Inada et.al. [8]	n	n	2	0	Qutrit control	
This work	n	n	2	0	$\|11\rangle\langle 20\| + \|20\rangle\langle 11\|$	

TABLE S2. **Comparison of multi-qubit Toffoli gate decomposition assuming a 1-D chain.**

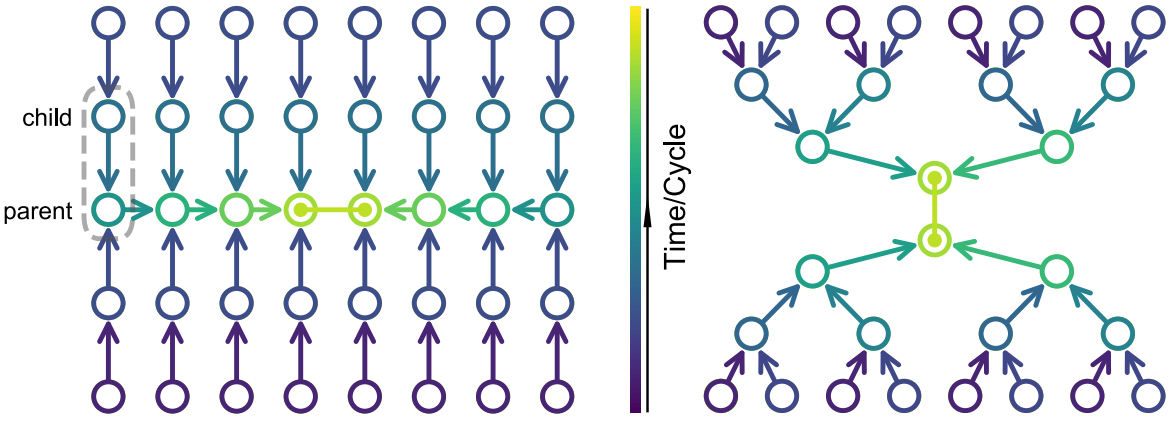


FIG. S5. **Schematics of synthesizing multi-qubit CZ gates on 2-D square array (left) and a binary tree (right).** Circles indicate qubits and arrows indicate QuAND gates, pointing from child to parent. Color gradient indicates the temporal order. The reverse QuAND sequence is omitted.

III. DEVICE AND EXPERIMENTAL SETUP

A. Wiring

The processor is made of aluminum on sapphire following a similar recipe as described in Ref. [9]. It is mounted inside a dilution refrigerator at a base temperature of 10 mK. We magnetically shield the processor with two Cryoperm cylinders. Inside the refrigerator, we use a total of 10 coaxial lines for the qubit/coupler control, 1 input and 1 output line for qubit readout. Attenuators and filters are installed at different temperature stages for thermalization and noise attenuation. At the lowest-temperature stage, we use customized low-pass IR filters on all the control lines for attenuating (20-30 dB) signal at qubit frequency while passing DC and low-frequency signal. The output signals are amplified by a high electron mobility transistor (HEMT) amplifier (40 dB gain) at the 4K stage and another low-noise amplifier (50 dB gain) at room temperature. Circulators and filters are placed on the output line to block noises from higher temperature stages. The output signals are finally down-converted to intermediate frequency and demodulated by two analog-to-digital converters (ADCs).

Microwave signals for single-qubit XY control and dispersive readout are up-converted from carriers generated by a microwave source using IQ mixing. We use diplexers to combine the XY and the Z signals at room temperature. For better impedance matching, an isolator is added to the XY port.

B. Device parameters

We summarize the measured device parameters in Table.III. Over time, we observe coherence fluctuations for some qubits, likely due to coupling to spurious two-level systems (TLSs).

We observe significant dephasing (Ramsey decay time <200 ns) from flux noise when performing two-qubit operations by adjusting the coupler frequency close to the qubit frequency. We fit the dephasing time to the slope of corresponding energy spectrum in order to extract the flux noise amplitude $\sigma_{\Phi_e} = 116\mu\Phi_0$ according to the relation $\Gamma_\phi^s(\Phi_e) = \frac{1}{\sqrt{2}}\frac{\partial\widetilde{\omega}_s}{\partial\Phi_e}\sigma_{\Phi_e}$. The relaxation time of the couplers are measured by swapping excitation from a neighboring qubit to the coupler, delaying for a varying amount of time, and swapping the remaining excitation back to the qubit. The strong flux noise and shorter relaxation time of the couplers explain majority of the two-qubit gate error.

Since the second excited state of the (child) qubits are used for temporary storage, their coherence will affect the performance of Toffoli gate. In the transmon design, the second excited state is subject to larger charge dispersion, making it more sensitive to charge noise. The average relaxation time of $|2\rangle$ is measured to be 8.8 μs, about half the relaxation time of $|1\rangle$ (15.5 μs), which is consistent with the relation $|\langle 2|\hat{n}|1\rangle|^2 = 2|\langle 1|\hat{n}|0\rangle|^2$. With our design parameters, the charge dispersion on the $|2\rangle$ state is estimated on the order of $0.03 \sim 5$ kHz, leading to negligible dephasing. The measured average T_2 of the $|2\rangle$ state (relative to $|0\rangle$) is 9.5 μs, shorter than that of the $|1\rangle$ state (16.6 μs), mainly due to the shorter relaxation time.

We use randomized benchmarking (RB) to characterize gate errors. For single qubit gates, the gate fidelity in both isolated and simultaneous benchmarking is near the coherence limit. For two-qubit gates, we observe worse error rate – typically 2-3 times – when performing simultaneous two-qubit RB experiments on all eight qubits. We suspect the cause to be the spectator effect in the presence of unwanted stray coupling present as discussed in Ref. [10].

C. Crosstalk

Crosstalk is a major technical challenge for building large-scale processors. In Fig. S7, we show the measured microwave (XY) crosstalk, flux (Z) crosstalk and residual ZZ interaction. The effect from microwave (XY) crosstalk between neighboring qubits (not shown) are negligible in this device due to large detuning between red-band and blue-band qubits. In the experiment, we calibrate microwave crosstalk for qubits in the same frequency band using the method presented in Ref. [11]. After the calibration, there is negligible XY crosstalk effect on gate performance as evident by the isolated and simultaneous single-qubit gate RB results (Table S3). The Z crosstalk is strongest between neighboring qubits (average: 0.23%, standard deviation: 0.16%), and is calibrated using Ramsey-type experiments. The ZZ crosstalk is also strongest between neighboring qubits (average: 52 kHz, standard deviation: 26 kHz). The low-level residual ZZ interaction has a negligible contribution to gate errors.

Qubit[a]	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Frequency (GHz)	6.257	7.015	6.359	7.152	6.424	7.142	6.504	7.184
Anharmonicity (GHz)	-0.255	-0.236	-0.252	-0.239	-0.252	-0.238	-0.250	-0.239
Readout resonator frequency (GHz)	4.973	4.979	5.018	5.023	5.064	5.071	5.112	5.120
Readout resonator linewidth (MHz)	0.7	0.8	0.7	0.8	0.8	0.8	0.8	0.8
Dispersive shift of $\|1\rangle$ (MHz)	-0.55	-0.22	-0.50	-0.22	-0.47	-1.20	-0.50	-0.28
Dispersive shift of $\|2\rangle$ (MHz)	-1.65	-0.75	-1.85	-0.67	-1.75	-0.60	-1.40	-0.80
Readout error of $\|0\rangle$ (%)	3.3	1.4	1.3	1.1	1.1	3.9	4.0	1.2
Readout error of $\|1\rangle$ (%)	10.1	14.4	8.9	10.3	7.3	22.3	14.2	8.8
Readout (three state) error of $\|0\rangle$ (%)	3.8	1.3	0.9	0.9	1.5	4.8	8.8	0.9
Readout (three state) error of $\|1\rangle$ (%)	23.4	19.6	15.1	15.3	9.9	23.0	19.5	9.7
Readout (three state) error of $\|2\rangle$ (%)	16.6	20.4	20.3	16.1	16.8	20.7	30.9	24.6
Relaxation time of $\|1\rangle$ (μs)	21	10	15	19	22	7.3	12	18
Relaxation time of $\|2\rangle$ (μs)	14	6.1	8.0	10	12	4.6	7.1	8.9
Ramsey decay time of $\|1\rangle$ (μs)	25	11	19	13	26	12	18	9.0
Ramsey decay time of $\|2\rangle$ (μs) [d]	8.0	3.6	7.7	12.0	12.7	\	10.2	12.1
Spin echo decay time of $\|1\rangle$ (μs)	32	15	23	32	36	11	21	30
1-Q gate error[c] (isol.)(%)	0.07	0.16	0.11	0.11	0.06	0.19	0.11	0.14
1-Q gate error[c] (simul.)(%)	0.10	0.17	0.12	0.13	0.07	0.23	0.14	0.13
Coupler	C_{01}	C_{12}	C_{23}	C_{34}	C_{45}	C_{56}	C_{67}	C_{70}
Frequency (sweet spot) (GHz)	8.08	8.13	8.04	8.28	8.38	8.27	8.40	8.32
Relaxation time (μs)	4.6	4.9	7.5	6.7	4.5	7.1	3.1	3.3
Flux noise strength ($\mu\Phi_0$)	118	120	116	117	97	108	144	110
Coupling coefficient[b] $r_{\rm qc}$ (left qubit)	0.0186	0.0189	0.0185	0.0070	0.0184	0.0185	0.0186	0.0061
Coupling coefficient[b] $r_{\rm qc}$ (right qubit)	0.0155	0.0175	0.0177	0.0098	0.0175	0.0176	0.0178	0.0076
CZ gate error[c] (isol.)(%)	0.92	0.97	1.20	3.50	1.40	1.50	1.2	3.0
CZ gate error[c] (simul.)(%)	2.5	5.0	3.4	7.5	3.0	5.1	2.4	6.0

[a] The qubit parameters are measured with the coupler idly biased at the sweet spot.
[b] The coupling strength between the qubits and the coupler is frequency dependent, as $g_{\rm qc} = r_{\rm qc}\sqrt{\omega_{\rm q}\omega_{\rm c}}$. We extract the coupling coefficient by fitting the measured level spectra versus the flux bias on the coupler.
[c] The gate errors are measured using single(two)-qubit randomized benchmarking (RB). For two-qubit RB, we extract CZ gate errors by subtracting single qubit errors from the average errors of two-qubit Cliffords. The simultaneous two-qubit RB is performed in group of (Q_0-Q_1,Q_2-Q_3,Q_4-Q_5,Q_6-Q_7) and (Q_1-Q_2,Q_3-Q_4,Q_5-Q_6,Q_7-Q_0).
[d] Measured in a different cooling down. There is a stronger TLS that fluctuates Q_5, causing unclear T_2 result.

TABLE S3. **Device parameters**.

D. Readout correction

To correct state preparation and measurement (SPAM) error, we first find the transfer matrix $\mathcal{R}$ by preparing all computational states of the joint system and measured the final probability distribution, as shown in Fig. S8. Given the relatively small single-qubit gate error (0.14%), we have ignored the error of $\mathcal{R}$ itself. We then use $\mathcal{R}$ to correct readout results in subsequent experiments according to

$$|\varphi_{\rm corrected}\rangle = \mathcal{R}^{-1}|\varphi_{\rm raw}\rangle. \tag{1}$$

IV. COUPLER-ASSISTED iSWAP GATE BETWEEN FIXED-FREQUENCY QUBITS

In the rest of this supplementary material, unless specified otherwise, by iSWAP we mean the coherent swapping operation between $|11\rangle$ and $|20\rangle$, but not the usual definition which is between $|01\rangle$ and $|10\rangle$. For optimal state transfer during the iSWAP gate, the following four factors need to be considered when choosing the operation point: (1) short gate time considering the limited coherence time; (2) avoiding unwanted transitions during pulse rise and fall; (3) smaller parametric modulation amplitude to avoid high-order interaction; (4) avoiding spurious transitions during the parametric modulation.

Short gate time can be realized by shortening either the adiabatic rising/falling edges or the parametric pulse length. To loosen the adiabatic condition and ease the pulse shaping efforts, operation points closer to the idling bias (towards the left in the Fig. S9a and d) are preferred. It's worth noting that there is generally a small avoided level crossing ($\Delta_{\rm gap} \approx 2$ MHz) between $|110\rangle$ and $|002\rangle$, which we want to pass as fast as possible to avoid transition to $|110\rangle$

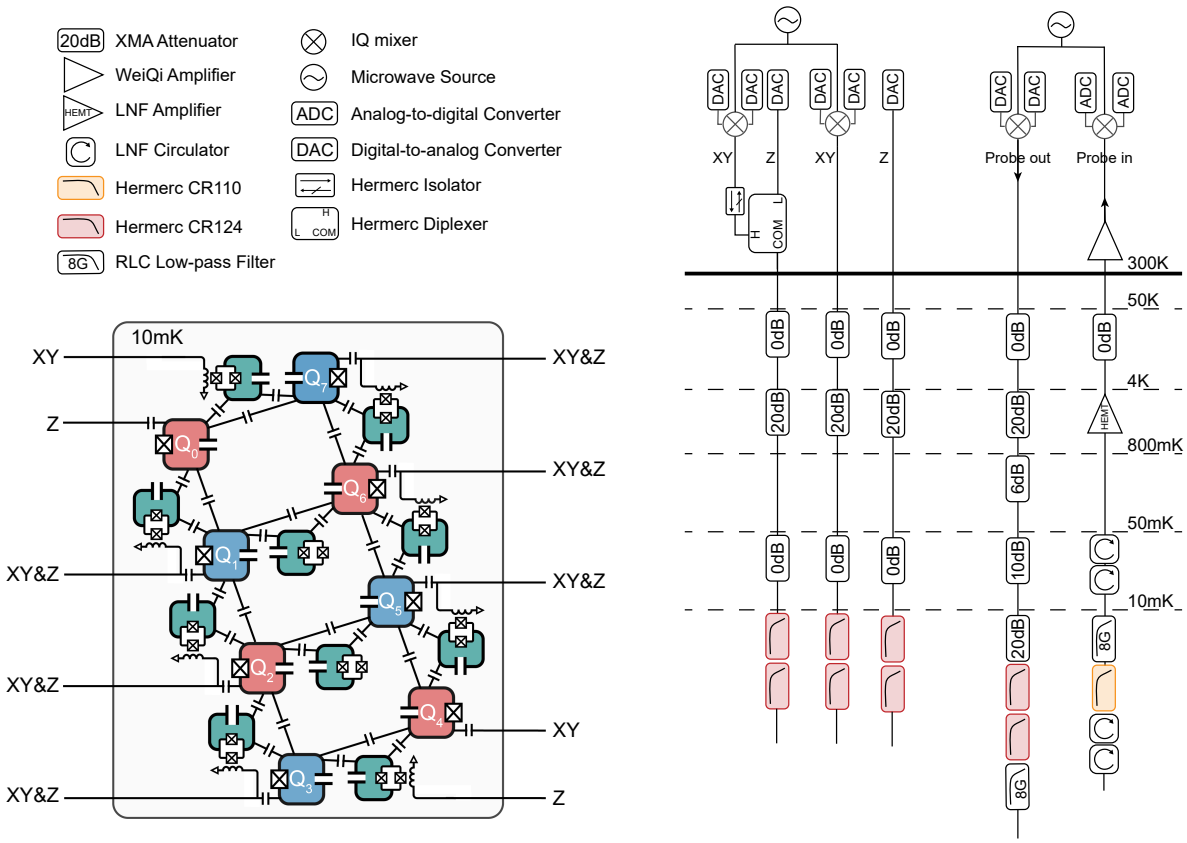


FIG. S6. **Schematic diagram of the experimental setup**. (Left) Schematic diagram of the 8-qubit quantum processor and 10 control lines (the readout line and the resonators are not shown). Adjacent qubits and couplers are capacitively coupled. The shared control lines are inductively coupled to qubits for XY drive and to coupler SQUID for frequency modulation. (Right) The schematic diagram of control electronics and wiring.

during the adiabatic falling edge. Shortening the parametric pulse requires stronger parametric modulation amplitude and/or a larger transition matrix element $|\langle s|a_c^\dagger a_c|101\rangle|$ (s=200 or 002). Too strong a parametric modulation results in high-order interaction term that cannot be ignored in the Jacobi-Anger expansion. For small modulation amplitude and short length, the working point towards lower coupler frequency is preferred as the transition matrix element becomes significantly stronger due to wavefunction hybridization.

To avoid spurious transitions to other states, we compare their impact on the target transition across the bias range. Figure S9b and e show the calculated AC Stark shift $\delta = (\sqrt{\Delta^2 + (r\ \Omega_0)^2} - |\Delta|)$, a metric to quantify the spurious effect by taking into consideration both detuning from targeted to unwanted transition Δ and drive strength $r * \Omega_0$, where Ω_0 is the Rabi frequency of the targeted transition given a certain drive amplitude, and r is the relative strength of the unwanted transition. In the experiments, we choose the extremum (black dot) as our operation point, balancing both the spurious effect and adiabatic constraint. The working points can be roughly identified from the transition spectroscopy experiment by comparing theory and experimental result, as shown in Fig. S9b and S9e.

At the selected operation points, we identify $|101\rangle \leftrightarrow |200\rangle$ transition through a swap-spectroscopy experiment (Fig. S10a). The targeted transition is well-separated from other spurious transitions. Finding the parametric frequency, we calibrate the iSWAP gate (pulse width: 30 ns) by sweeping the pulse amplitude, as shown in Fig. S10b. We check the integrity of the selected transition by counting the probability at each computational state, and repeat it for four different input states. Residual transition errors (2.7% on average) are mainly caused by energy relaxation during the pulse.

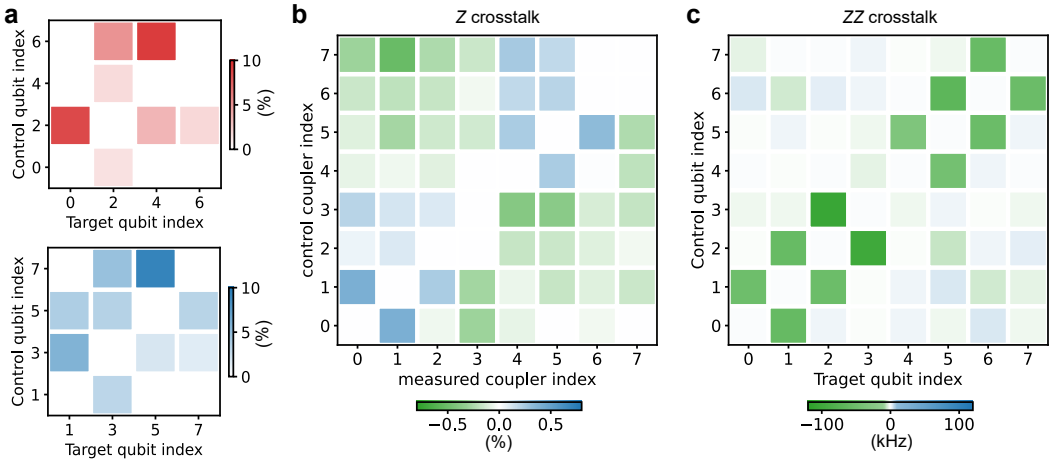


FIG. S7. **System crosstalk**. **a**, XY crosstalk coefficient between red-band qubits (top) and blue-band qubits (bottom). **b**, Z crosstalk coefficient between couplers. **c**, ZZ interaction strength between qubits. The ZZ interaction strength is measured with all the couplers biased at the sweet spot.

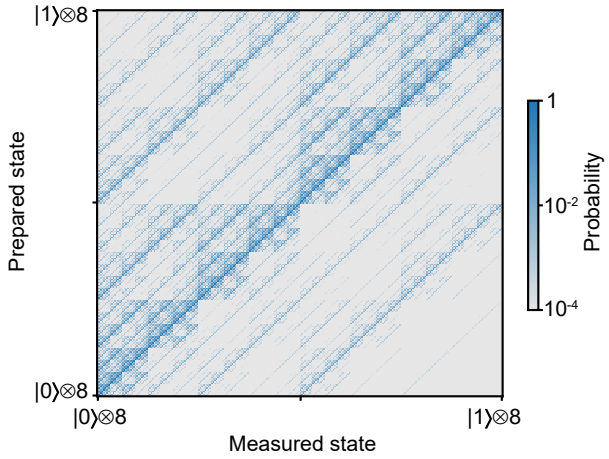


FIG. S8. **Multi-qubit readout correction matrix**. Readout matrix for 8-qubit system $|Q_0Q_1Q_2Q_3Q_4Q_5Q_6Q_7\rangle$.The readout matrix is measured by traversing $2^8 = 256$ eigenstates of the system (lowest two states for each qubit). For each prepared state, we repeat multiplexed state measurement for 50000 times.

V. IMPLEMENTATION OF n-QUBIT CZ GATES

A. Gate decomposition

The $n-$CZ gate scheme can be decomposed into iSWAP gates calibrated for connected qubit pairs on the 8-qubit ring and single-qubit X gates. The circuit for implementing the $n-$CZ gate with $n = 4, 6, 8$ are illustrated in Fig. S11a. There are two considerations when selecting the qubits in each case. First, the qubit pairs at both ends of the ladder, Q_0–Q_7 and Q_3–Q_4, have a relatively weak qubit–coupler interaction strength ($g/2\pi \approx 40$ MHz), leading to a tighter adiabatic condition and an inferior gate performance. Second, the frequency of Q_3 is unstable, showing random telegraph behavior, possibly as a result of spurious two-level systems. The waveforms for qubit-XY and coupler-Z control in the 8-CZ case is shown in Fig. S11b. To suppress the correlated flux noises, we idle all couplers at their respective sweet spot and use two-pole flux modulation in the flux pulses of the QuAND and reverse QuAND gates.

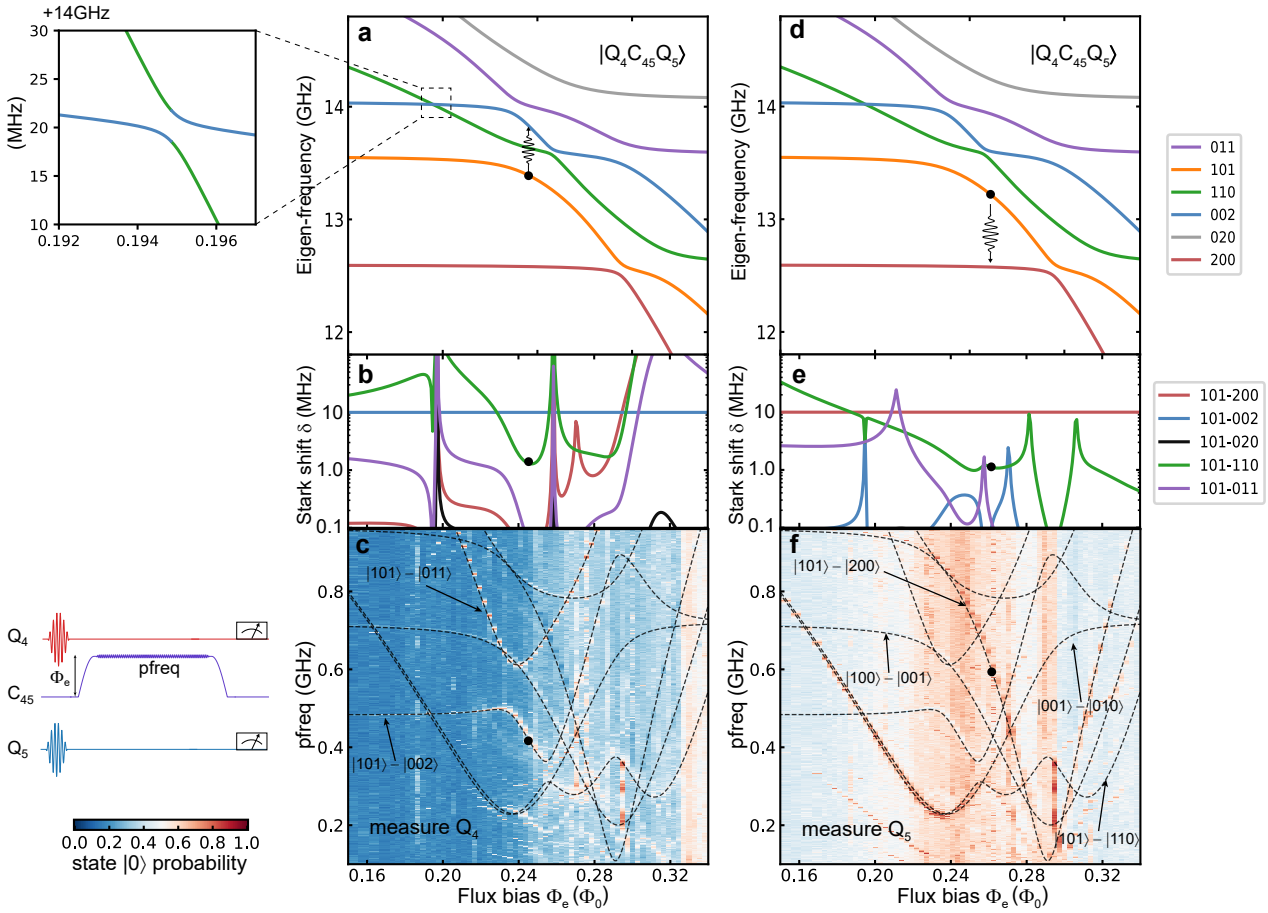


FIG. S9. **Optimizing the operation point for the iSWAP gate**. **a**, Energy level spectra of the qubit(Q_4)-coupler-qubit(Q_5) system versus the coupler flux bias Φ_e (solid lines). The inset shows the small avoided level crossing between $|002\rangle$ and $|110\rangle$. **b**, AC Stark shift induced by spurious transitions from the parametric drive versus flux bias. At each bias, we assume a drive amplitude that corresponds to 10 MHz $|101\rangle$-$|002\rangle$ swapping rate, i.e. Ω =10 MHz. Several prominent transitions are identified. **c**, Transition spectroscopy (initial state: $|101\rangle$, measured qubit: Q_4) by sweeping the frequency of the parametric pulse and the the flux bias amplitude. The experiment sequence is shown in the left. Here we identify transitions by measuring the probability of $|0\rangle$, since the chosen readout frequency doesn't discriminate the first and second excited state. The black dots sharing the same horizontal axis indicate the optimal operation point for the parametric swap between $|101\rangle$ and $|002\rangle$. **d**, Same as **a** but the transition is to $|200\rangle$. **e**, Same as **b** but the resonant transition is between $|101\rangle$-$|200\rangle$. **f**, Same as **c** but the measured qubit is Q_5.

B. Calibration procedures

As discussed in the Methods, rotation angle of an iSWAP operation can be changed by varying the phase of the parametric modulation and only the relative phase between two consecutive iSWAP gates affects the final conditional phase accumulation on state $|11\rangle$. This is a more convenient way, compared to the previously demonstrated approach based on resonant interaction, in which the pulse length has to be varied to calibrate a π-SWAP gate and a 3π-SWAP gate for cancelling the conditional phase [12]. An example of the paired QuAND sequence producing an identity operation and the corresponding process tomography result (after calibration) is shown in Fig. S12.

The phase calibration of an n-CZ gate starts with the CZ gate in the middle, and then progressively extends to the outermost part of the circuit. In each iteration, we set the phase of first parametric pulse (in QuAND) to 0, calibrate the phase of the second parametric pulse (in reverse QuAND) through a conditional Ramsey experiment. In the following, we articulate our calibration procedures step-by-step:

(i) **iSWAP calibration.** We first calibrate all the iSWAP pulses between adjacent qubits – optimizing the frequency and amplitude of the parametric modulation – in order to make the excitation swap as complete as possible, as illustrated in Fig. S10.

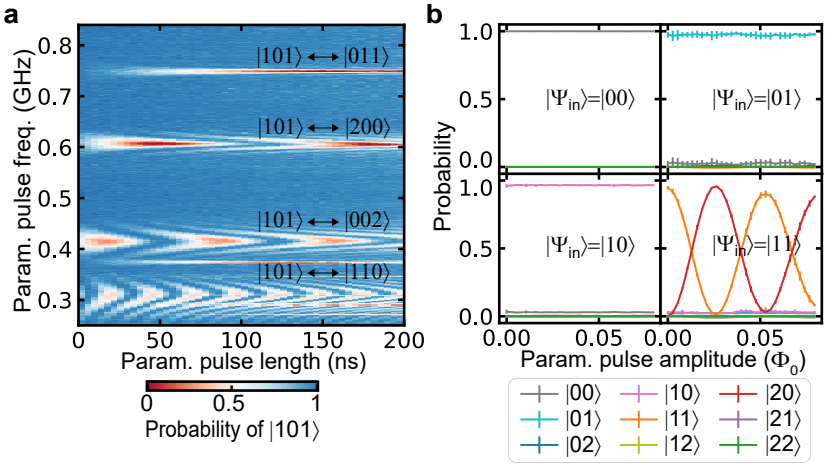


FIG. S10. **Implementation of the coupler-assisted iSWAP gate**. **a**, iSwap spectroscopy (starting from $|101\rangle$)by sweeping the length and frequency of the parametric pulse at $\Phi_e = 0.26\ \Phi_0$, using a weak parametric pulse amplitude ($A_p \approx 0.01$). Several prominent transitions are identified. **b**, Measured probability distribution of the final state after the iSWAP pulse (coupler traced out) versus the parametric pulse amplitude, repeated for four different input states. The parametric pulse length is 30 ns.

(ii) **Single-qubit phase calibration.** Because the qubit frequency is modulated during the iSWAP pulse, the pulse itself induces single-qubit phases (ϕ_1 and ϕ_2) on both qubits as well as a conditional phase as mentioned before. The conditional phase will be handled later, and we can ignore it for now. The single-qubit phases may be compensated by adding virtual-Z gates in the circuit, which can be calibrated using the pulse train method, as illustrated in Fig. S13a-b.

(iii) **Conditional phase calibration.** We then apply the iSWAP gates (single-qubit phase corrected) to the CCZ circuit by sandwiching a previously calibrated CZ gate with a pair of QuAND and reverse QuAND gate, as shown in Fig. S13c. In general, the equivalent circuit is a CCZ gate plus a controlled-phase gate CZ(φ_{zz}), which results from the nontrivial phase accumulated during the idling period and during the iSWAP pulses. The conditional phase φ_{zz} can be calibrated using the standard conditional Ramsey technique. As we discussed before, the phase of the first iSWAP gate can be made arbitrary. Without loss of generality, we set it to zero. We then sweep the phase of the second iSWAP gate and find the correct phase which gives $\varphi_{zz} = 0$, as illustrated in Fig. S13d. Note that the conditional phase only shifts with the pulse phase in the case when the Q_0 is prepared at the ground state, because there is an X pulse before the iSWAP gate in QuAND and the $|11\rangle$-$|20\rangle$ iSWAP is effective only when Q_0 starts at the ground state.

(iv) **Extension to more qubits.** The procedure can be extended to a n-qubit controlled phase gate by adding more QuAND pairs into the circuit. For example, Fig. S13e describes how to synthesize an n-CZ gate from an existing $(n-1)$-CZ gate. Similar to the CCZ case, there is an unwanted conditional phase arising from the two added iSWAP gates, which can be calibrated away in the same way as described in the last step. Note that since we can position the CZ gate in the middle of the qubit chain, the process can be expedited by calibrating QuAND pairs on both sides of the CZ gate in parallel.

(v) **Final check.** The final calibration result can be verified by running a full-scale conditional Ramsey experiment (Fig. S13f).

VI. ERROR ANALYSIS

A. Process tomography

The truth table measures the probability distribution of the final states given a set of eigenstates as input. It may underestimate phase errors in the corresponding process. To fully characterize the multiply controlled gate synthesized from QuAND, we perform standard process tomography for the 4-qubit CZ (CCCZ) gate. Unfortunately, process tomography with larger matrix is unattainable due to limited memory. The reconstructed process matrix χ_{exp} from

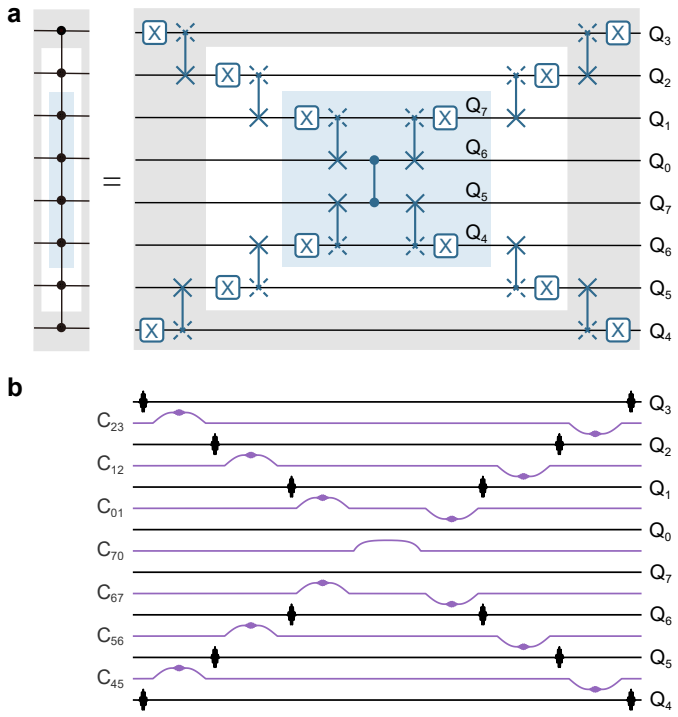


FIG. S11. **Circuit diagram and 8-qubit pulse sequence for n-qubit CZ gates. a**, Circuit diagram for implementing the 4-qubit (blue), 6-qubit (light gray), and 8-qubit (dark gray) controlled-Z gate. **b**, Experimental pulse sequence for the 8-Toffoli gate. The black (purple) curve represents qubit-XY (coupler-Z) signal. The couplers are idly biased at the sweet spot and the second flux pulse is inverted for suppressing low frequency noise.

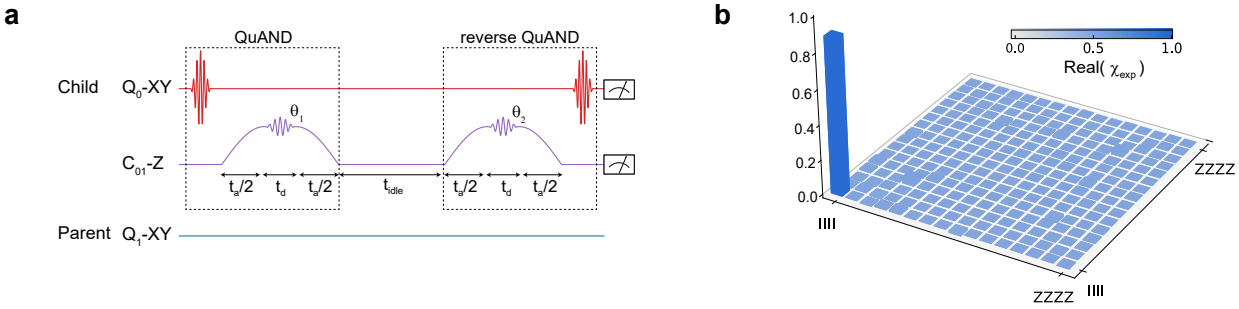


FIG. S12. **Identity operation from a QuAND pair**. **a**, Pulse sequence for QuAND and reverse QuAND gate. The two iSWAP pulses swap the excitation from $|11\rangle$ to $|20\rangle$ and back to $|11\rangle$, however, with a phase factor which can be calibrated away by adjusting the relative phase of the parametric modulation $(\theta_2 - \theta_1)$. **b**, Real part of the experimentally measured process matrix $\chi_{\rm exp}$ of a calibrated identity operation formed by the paired QuAND gates in **a**. The process fidelity $\mathcal{F}_{\rm p} = {\rm Tr}(\chi_{\rm exp}\chi_{\rm I})$ is 89.0%, corresponding to a gate fidelity of $\mathcal{F}_{\rm g} = 91.2\%$. The idling time $t_{\rm idle}$ between the QuAND and the reverse QuAND gate is 100 ns. The process fidelity is lower than the average state fidelity 95.1%, which is a consequence of the higher sensitivity to phase errors in process tomography. The measured leakage rate of the QuAND pair is about 0.35%.

$4^4 = 256$ distinct input states gives process fidelity $\mathcal{F}_{\rm p} = {\rm Tr}(\chi_{\rm exp}\chi_{\rm ideal})$ =82.6% (Fig. S14). Corresponding CCCZ gate fidelity $\mathcal{F}_{\rm CCCZ} = (16 * \mathcal{F}_{\rm p} + 1)/17 = 83.6\%$ is lower then the 4-qubit Toffoli truth-table fidelity shown in the main text (both using $Q_4Q_5Q_6Q_7$), and is close to the fidelity (84.4%) fitted from the Grover's success fidelity (Fig. 4c in the main text). In the following, we discuss the main error processes including relaxation and leakage.

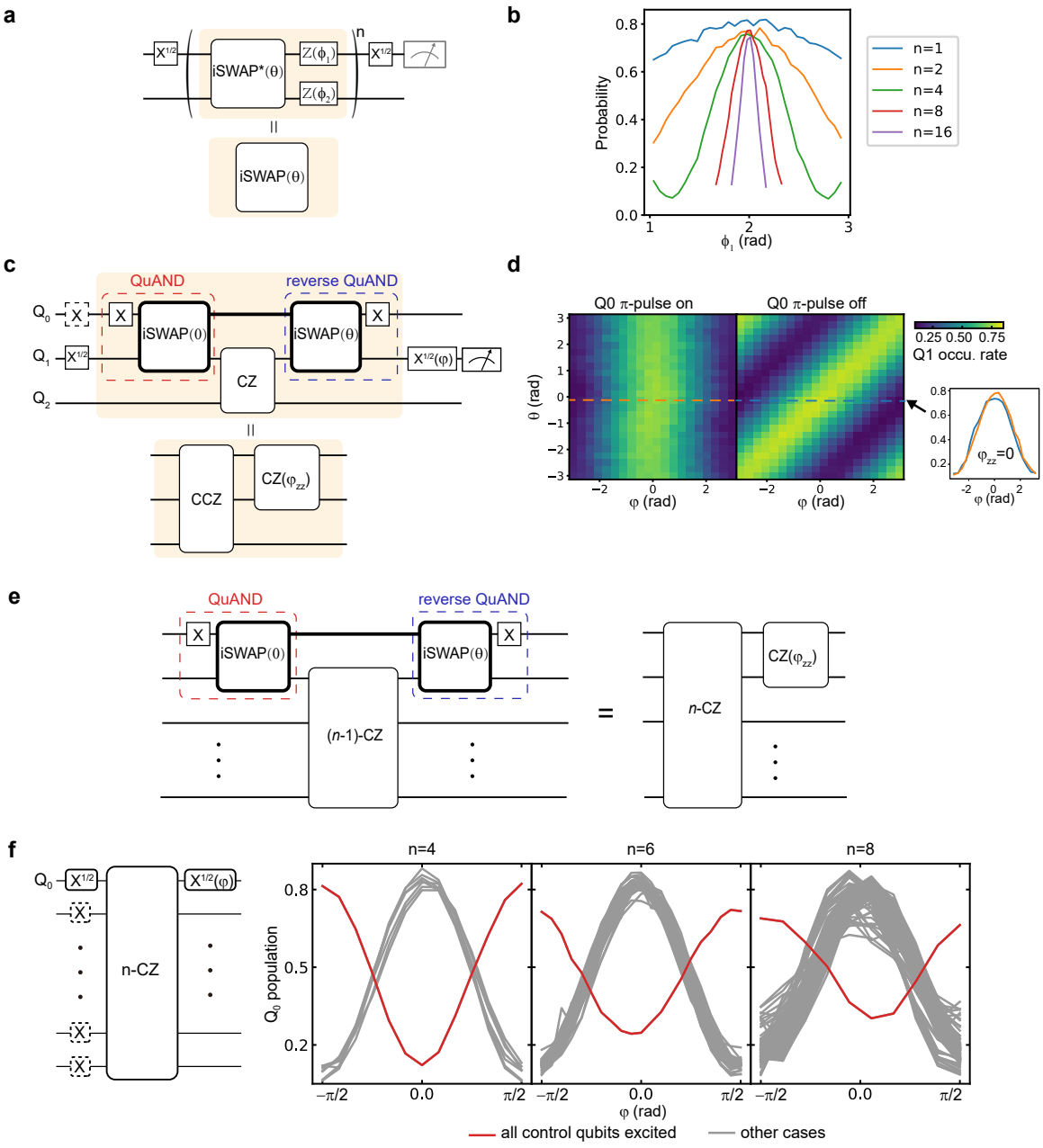


FIG. S13. **Phase Calibration of $n-$CZ gates**. **a**, Circuit diagram of the sequence for calibrating single-qubit phases induced by the iSWAP gate. The unitary of a native iSWAP pulse, iSWAP$^*(\theta)$ is different from an iSWAP gate, iSWAP(θ), by single-qubit Z rotations on both qubits (ϕ_1 and ϕ_2). We use the pulse train method by repeating a subcircuit n times for enhanced sensitivity. **b**, Example of progressively calibrating ϕ_1 with increasing number of repeated cycles. **c**, Circuit diagram of the sequence for calibrating a CCZ gate using previously calibrated iSWAP gate (single-qubit phase corrected) from **a** and a CZ gate between Q_1 and Q_2. The bold lines are used to indicate that part of the circuit diagram should be interpreted differently from the traditional description based on binary states. For example, the iSWAP gate here is not the conventional $|01\rangle$-$|10\rangle$ iSWAP, but involving an ancilla state, which should also be considered for the idling period between the two iSWAP gates. A conditional Ramsey sequence is applied to Q_0 (control qubit) and Q_1 (target qubit) for measuring the conditional phase. The $X^{1/2}(\varphi)$ gate denotes a $\pi/2$ pulse with a varying phase of φ. **d**, The measured response from the sequence in **c** with varying phase of second iSWAP gate θ and with Q_0 initialized at $|0\rangle$ or $|1\rangle$ state. As expected, the conditional phase ϕ_{zz} changes linearly with θ. The $\phi_{zz} = 0$ condition is met at a specific θ (dashed linecuts) where the phase responses are aligned. **e**, Circuit diagram showing how to extend the calibration from a (n-1)-CZ gate to a n-CZ gate and the equivalent circuit. **f**, Multi-qubit conditional Ramsey experiment for verifying the phase calibration for an n-qubit CZ gate ($n = 4, 6, 8$). In the shown example, Q_0 is used as the target qubit, while all the other qubits are prepared at either $|0\rangle$ or $|1\rangle$ state to traverse all possible combinations. Obviously, the phase of the target qubit is flipped only if the control qubits are prepared at $|1\rangle$ state (red curve), confirming the phase calibration result.

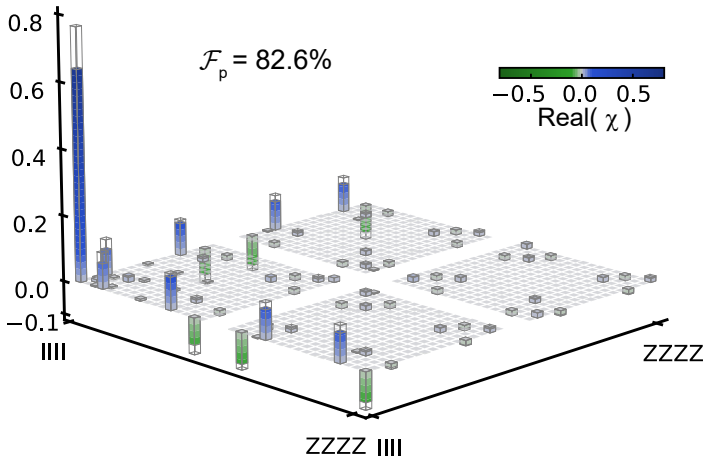


FIG. S14. **Process tomography of the 4-CZ or CCCZ gate (color bar: experiment; frame: theory).**

B. Relaxation error

We estimate the T1-limited gate fidelity ($\mathcal{F}_{\mathrm{T1}}$) by segmenting the circuit (in Fig. S15) and taking the product of T1-limited fidelity of each segment $\mathcal{F}_{\mathrm{T1}} = \Pi_{j,k}\mathcal{F}_{\mathrm{T1}}^{j,k}$. The relaxation rate of an instantaneous eigenstate during a flux pulse generally keeps varying during the pulse, due to the varying wavefunction participation of different bare states [10]. The average relaxation rate of the eigenstate is calculated by summing up contribution from all bare states. The rate is larger than that of idle status, because of the strong overlap with the relatively short-lived coupler (see Table. S3).

The relaxation-limited gate fidelities (total duration) for the 4-qubit, 6-qubit, and 8-qubit Toffoli gates are 92.5% (0.4 μs), 66.7% (1.3 μs, staggered pulses), and 62.3% (1.1 μs), respectively, and are responsible for approximately 70% of the total error. Note that the gate length of 6-Toffoli is longer because we stagger the flux pulses for reducing the otherwise strong spectator effect [10].

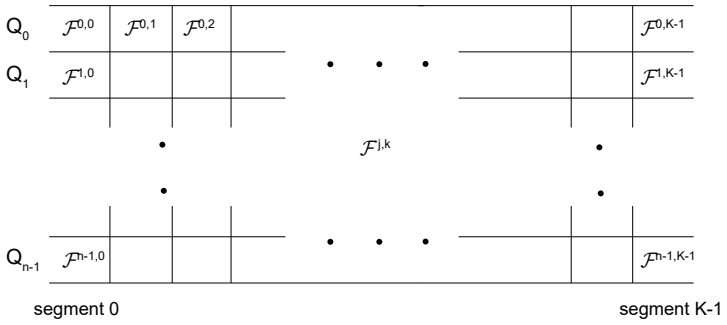


FIG. S15. **Fidelity analysis and pulse sequence for n-qubit Toffoli.** Sketch of segmented circuit for fidelity estimate. $\mathcal{F}_{\mathrm{T1}}^{j,k}$ represents T1-limited fidelity of qubit j in segment k.

C. Leakage error

In Fig. S16, we show an extended 4-qubit Toffoli gate truth table with $|2\rangle$ state included in the readout for analyzing the leakage effect. The average leakage rate to higher energy levels over 16 inputs is about 0.82%. The state leakage mainly arises from the two pair of QuAND gates (∼0.35% for each pair) and the CZ gate (∼0.1%) in between.

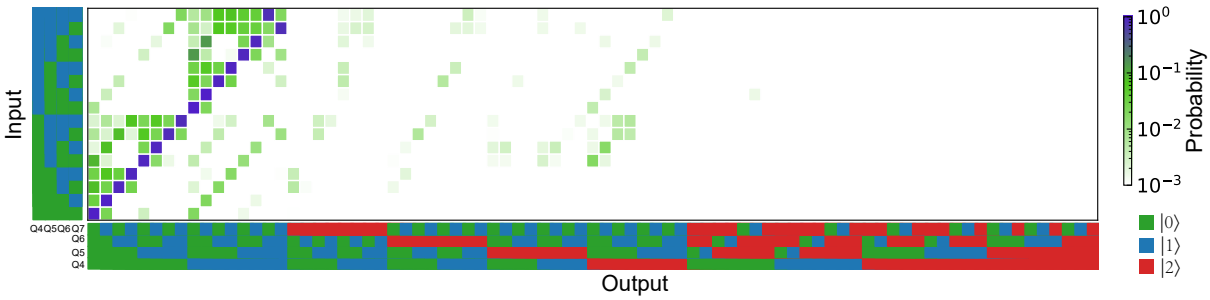


FIG. S16. **4-qubit Toffoli gate truth table including state $|2\rangle$.**

VII. GROVER'S SEARCH ALGORITHM

The Grover's search algorithm generally includes four steps (as shown in Fig. 3a in the main text): (i) initialize the n-qubit system into an equal superposition of all possible bit-string states $\frac{1}{2^{n/2}}\sum_{s=0}^{2^n-1}|s\rangle$; (ii) encode the solution j with a phase oracle $O_j = \sum_{s\neq j}|s\rangle\langle s| - |j\rangle\langle j|$, i.e. a conditional π-phase shift on state $|j\rangle$; (iii) diffuse the encoded phase and amplify the probability of finding $|j\rangle$; (iv) measure the final state. Step (ii) and (iii) may be repeated for M times for further amplification. The algorithm promises quadratic speedup, reaching the optimal amplification at $M = 2^{n/2}$.

A. Error model for algorithm success probability

Here we provide a simple model for estimating the success probability (ASP) in Grover's search algorithm with non-ideal gate fidelity. To find one solution among an unstructured list of size 2^n using Grover's algorithm, the ideal ASP after M cycles of oracle queries is $\mathrm{ASP} = \sin^2\left((2M+1)\arcsin(2^{-\frac{n}{2}})\right)$. When the coherence is completed destroyed, the measurement outcome is a uniformly random number between 0 and 1 because the last layer of the circuit is a layer of Hadamard gates. Hence, the ASP is $\frac{1}{2^n}$. Since the circuit of each encoding-diffusing cycle contains two n-qubit CZ gates with fidelity $\mathcal{F}$ (ignoring single-qubit gate error), the fidelity of the whole circuit with M cycles is then $\mathcal{F}^{2M}$. A empirical ASP model can be written

$$\mathrm{ASP} = \mathcal{F}^{2\mathrm{M}}\sin^2\left((2\mathrm{M}+1)\arcsin(2^{-\frac{\mathrm{n}}{2}})\right) + \frac{1-\mathcal{F}^{2\mathrm{M}}}{2^{\mathrm{n}}}. \tag{2}$$

B. Leakage in Grover's Search

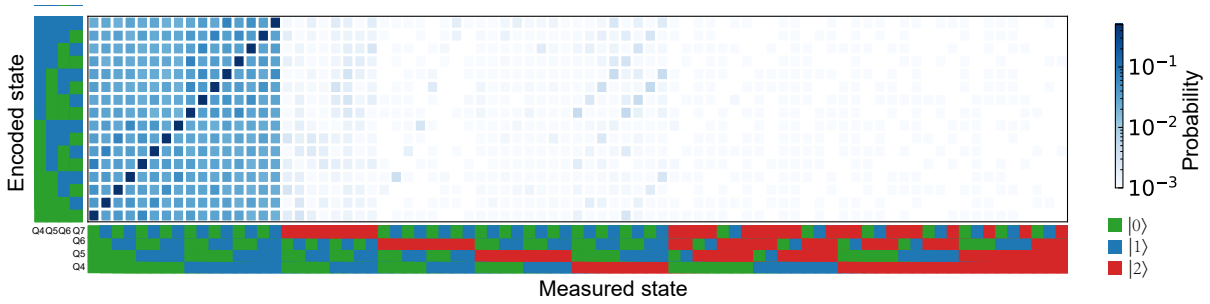


FIG. S17. **4-qubit Grover's search result ($M = 2$) including state $|2\rangle$.**

In Fig. S17, we show the measured leakage to non-computational states in the 4-qubit Grover circuit. We find that the majority of leakage goes to the second excited state of Q_4 and Q_7, which are used as the ancilla states for temporary storage. Moreover, we find that the leakage of the Grover circuit increases with its length or the number of oracle-amplification cycles M, as shown in Fig. S18. The increment slows down with larger M, because the leaked

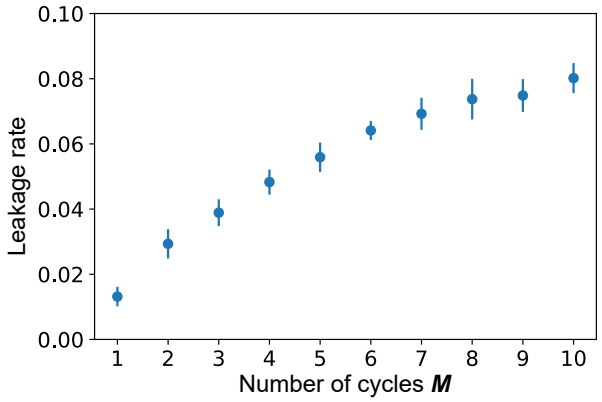


FIG. S18. **Average leakage rate (over 16 encoded states) of 4-qubit Grover's search versus the number of oracle-amplification cycles.** The data are presented as mean values +/- standard deviation.

population can decay back into the computational subspace. The measured leakage rate per cycle (1.3∼1.5%) is consistent with the 4-qubit Toffoli gate leakage (0.82%), given two CCCZ gates in each cycle.

C. Multi-solution Grover's Search

Multiple arbitrary solutions can be conveniently encoded in our scheme with concatenated oracles, as shown in Fig. S19a. Examples of experimental results for two-solution and three-solution Grover's search are shown in Fig. S19b and S19c.

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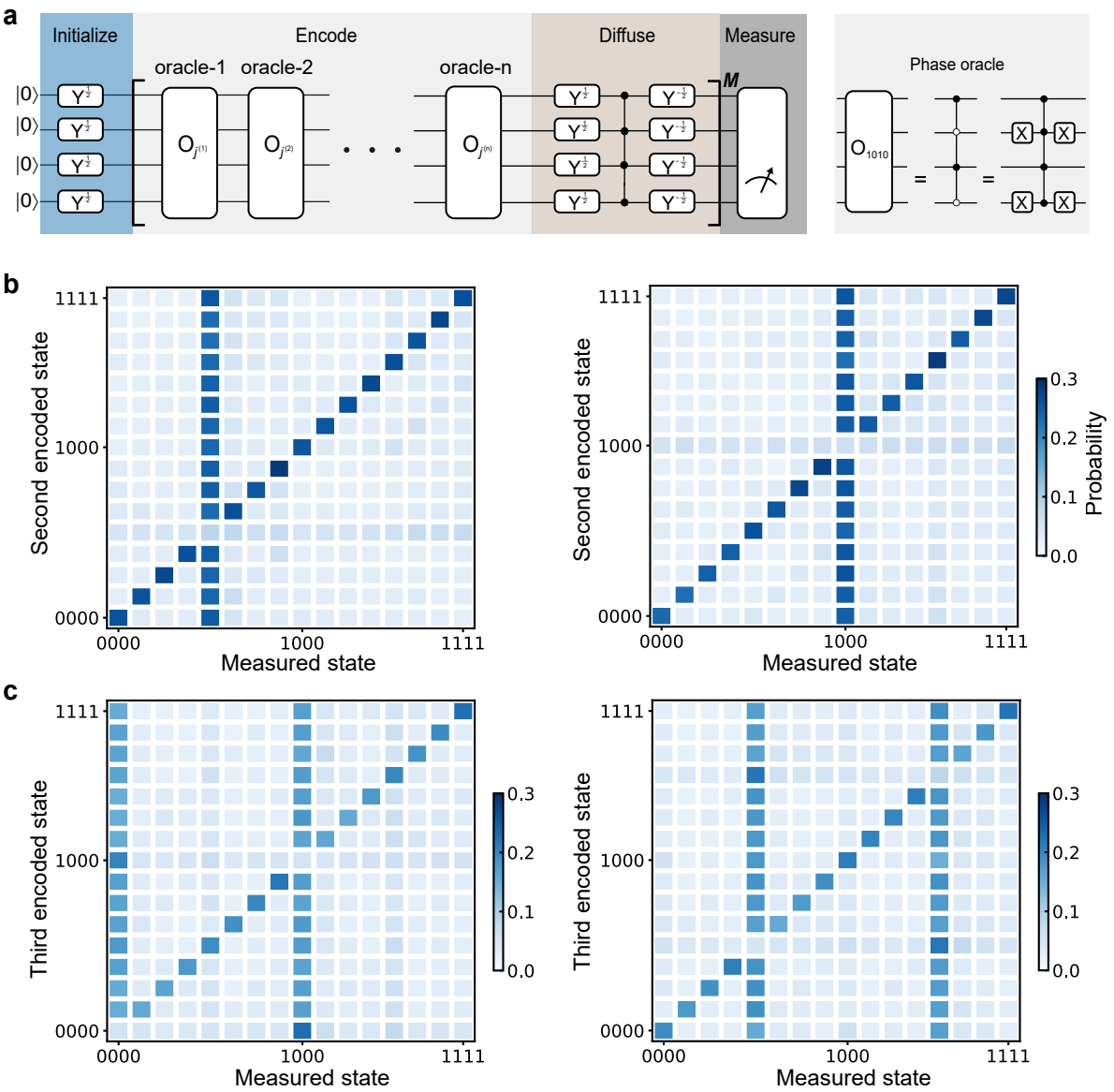

FIG. S19. **Multiple solution Grover's search algorithm**. **a**, Circuit diagram for implementing multi-solution Grover's search algorithm. During the encoding process, we apply multiple phase oracles in succession. An example of a 4-qubit phase oracle is shown on the right. **b**, Four-qubit two-solution Grover's search result ($M = 1$). With the first encoded state fixed as $|0100\rangle$ (left) or $|1000\rangle$ (right), the matrix shows how the measured probabilities of $2^4 = 16$ states vary with the second encode state (y-axis). When state $|0000\rangle$ is encoded twice (bottom), the net effect equals to no encoding and all states are measured with about equal probability. **c**, Four-qubit three-solution Grover's search result ($M = 1$). The first, second encoded states are fixed as $|0000\rangle$,$|1000\rangle$ (left) or $|0100\rangle$,$|1100\rangle$ (right) . The third one traverses over all the 16 logical states (y-axis).