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Supplementary information

High-speed and large-scale intrinsically stretchable integrated circuits

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Supporting information for

High-speed and large-scale intrinsically stretchable integrated circuits

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Supplementary Note I. Rationales for fabrication process development.

- To pattern M-CNTs, the most straightforward way is plasma etching. However, plasma etching will damage the polymer dielectric and cause large hysteresis. Next, we tried the conventional lift-off process. We first tried the lift-off method based on a single-layer photoresist. In this case, most of M-CNTs still remained on the substrate, making it difficult to achieve small channel lengths. We then tried the double-layer LOR/AZ1512 (or S1813) photoresists. However, the large modulus mismatch between LOR and the soft elastomeric substrate caused severe cracking of the LOR layer. In light of all the failed attempts, we developed the metal-assisted lift-off method to pattern M-CNTs, which finally allowed us to achieve small channel lengths without damaging/contaminating the dielectric layer. Liquid metal is also commonly used as drain and source contact materials for CNT transistors. For example, Andrews, J. B. et al. reported EGaIn can be used for printed carbon nanotube transistors[1], which showed the carrier mobility of 3.42 cm^2/Vs and contact resistance of 45.61 MΩ·μm, respectively. Our transistors showed a higher mobility of >20 cm^2/Vs and a lower contact resistance of 0.4 MΩ·μm. The higher performance of our transistors comes from the higher-quality semiconducting CNTs, e.g., higher density and cleaner surface, and better-matched work function for source/drain contacts. The high yield of our newly developed metal-assisted lift-off process results from the following factors: We used a metal layer to assist the lift-off of the M-CNTs. We found that without the metal layer, acetone can penetrate M-CNTs and dissolve the photoresist or PMMA underneath. As a result, M-CNTs will directly drop onto the substrate and cannot be easily lifted off. The existence of the metal layer can slow down the dissolution rate of the underneath PMMA layer, while the metal layer can be lifted off together with M-CNTs. Additionally, we prepared the M-CNTs layer by spray coating. Therefore, the tubes are not packed with a high density and the height difference at the edges of the metal layer may further lower down the density and make it easier to have a clean lift-off.

- To pattern the dielectric nitrile rubber, we used a thiol-ene reaction other than previously used azide[2] or diazirine-based crosslinking methods[3] based on two considerations. The first reason is

the wavelength constraint. The maskless alignment we used has only a 385 nm light source. This would not be effective for azide or diazirine chemistry. For the thiol-ene reaction, we can simply use an initiator that can absorb high wavelength UV (BAPO in our case) to trigger the reaction. The other reason is from the dosage perspective. The thiol-ene click reaction can occur at significantly reduced dosage for better production efficiency.

- To pattern the PEDOT:PSS gate electrodes, we chose plasma etching because PEDOT is the first layer of the process. During that step, no functional layers would be damaged by plasma etching. Compared with the direct photopatterning method in our previous paper[3], there are two main advantages in our new process. (1) Direct photopatterning of PEDOT requires a specific substrate with proper surface energy to achieve a clean patterning. In our previous paper, we used a PMMA-PnBA elastomer. In that work, if we used other elastomers, e.g., SEBS, NBR or TPU, we would have PEDOT residues at unexposed regions because PEDOT could not be completely washed off from these high surface energy elastomers. Our new process can work on all substrates, even non-crosslinked SEBS with very high surface energy. (2) In the previous paper, we found only a very narrow window of the PEDOT/PEGDMA blending ratio that allowed the direct photopatterning, while achieving high conductivity, high resolution, and high stretchability simultaneously. Our new process decouples the crosslinking and patterning. Therefore, we could first optimize the conductivity and stretchability using the PR crosslinker, and then pattern PEDOT. The smallest feature we could achieve was 0.8 μm, as opposed to 2 μm in the previous direct patterning method.

- To pattern S-CNTs, we first deposited S-CNTs on dextran to form a high-density CNT network, then transferred to the fabricated dielectric with the help of PMMA. After removing PMMA, we used SBS to encapsulate S-CNTs in the channel region and then pattern photoresist on top of SBS. This is to prevent contaminations of S-CNTs from the residue photoresist. We then did a short-time plasma etching to remove S-CNTs.

- To pattern EGaIn, we used the lift-off method rather than selective wetting because the selective wetting method does not offer high-resolution features as we needed.

Supplementary Note II. Modeling and simulation of transistors with short channel lengths.

The model of the CNT transistors is shown in Supplementary Fig. S32. In the linear region, if contact resistance is very small, then drain current I_{d} is given by

$$I_{\mathrm{d}} = \mu_0 C_{\mathrm{ox}} \frac{W_{\mathrm{Ch}}}{L_{\mathrm{Ch}}} \left((V_{\mathrm{gs}} - V_{\mathrm{th}}) V_{\mathrm{ds}} - \frac{{V_{\mathrm{ds}}}^2}{2} \right), \qquad \text{(Equation 1)}$$

where μ_0 represents low-field mobility of semiconductor, C_{OX} represents areal dielectric capacitance, W_{ch} and L_{ch} represent channel width and channel length, V_{gs}, V_{ds} and V_{th} represent gate-source voltage, drain-source voltage and threshold voltage. Considering the inner transistor (Fig. S31), the drain current is given by

$$I_{\mathrm{d}} = \mu_0 C_{\mathrm{ox}} \frac{W_{\mathrm{Ch}}}{L_{\mathrm{Ch}}} \left((V_{\mathrm{gs}'} - V_{\mathrm{th}}) V_{\mathrm{d's'}} - \frac{{V_{\mathrm{d's'}}}^2}{2} \right). \qquad \text{(Equation 2)}$$

Considering the contact resistance, drain current is given by

$$I_{\mathrm{d}} = \frac{V_{s's}}{R_{\mathrm{C}} W_{\mathrm{Ch}}} = \frac{V_{\mathrm{dd'}}}{R_{\mathrm{C}} W_{\mathrm{Ch}}}. \qquad \text{(Equation 3)}$$

The voltage across three parts should follow

$$V_{\mathrm{d's'}} + V_{\mathrm{dd'}} + V_{\mathrm{s's}} = V_{\mathrm{ds}}.$$

According to the above three equations, we can calculate I_{d}. All simulations were performed using Matlab. To evaluate how large the contact resistance impacts the performance of CNT transistor, we calculated the ratio of contact resistance and the total resistance by

$$\frac{2R_{\mathrm{C}}}{R_{\mathrm{tot}}} = \frac{2R_{\mathrm{C}} I_{\mathrm{d}}}{V_{\mathrm{ds}}}. \qquad \text{(Equation 4)}$$

When channel length was reduced to 2 μm, the ratio was up to 69.2%, proving that the contact

resistance largely degraded the device performance of short-L_{ch} CNT transistors.

Supplementary Note III. Modeling and simulation of transistors with interconnects.

To simplify the modeling and simulation process, we used the channel sheet resistance to describe the channel region operated in the linear regime, which was given by

$$R_{\text{ch,sheet}} = \frac{1}{\mu_0 C_{\text{ox}}(V_{\text{gs}} - V_{\text{th}})}, \quad \text{(Equation 5)}$$

then the device resistance can be calculated by

$$R_{\text{device}} = R_{\text{Ch,sheet}} \frac{L_{\text{Ch}}}{W_{\text{Ch}}} + 2R_C + 2R_{\text{SD,sheet}} \frac{L_{\text{SD}}}{W_{\text{SD}}}, \quad \text{(Equation 6)}$$

where L_{SD} and W_{SD} represent the length and width of S/D electrodes, and $R_{SD,sheet}$ represents the sheet resistance of S/D electrodes. The schematic diagram of the transistor geometry with S/D electrodes is shown in Fig. S37a. To model the wiring effect, we used a simple way to connect the source electrodes of all transistors together and connected the drain electrodes of all transistors together, as shown in Fig. S37b. The width of the wires is ~8 μm to maximize the device density (100,000 transistors/cm^2). All simulations were performed using COMSOL.

Supplementary Note IV. Development of intrinsically stretchable high-density active-matrix tactile sensor array.

To demonstrate braille recognition, tactile sensors need to be developed and integrated with transistors to form an active matrix. Monolithic integration is required to maintain the advantage of high density, so the sensors need to be fabricated with transistors together. As shown in Fig. 5b, here we used resistive tactile sensors, which consist of an upper electrode, a lower electrode, an air gap, and a structure-supporting elastomer. Applying pressure will reduce the air gap, and once the pressure reaches the threshold value, two electrodes will connect to each other to turn the sensor resistance from infinite to a small value.

One challenge is the possible leakage between the source/drain electrodes of transistors and the

upper electrode of sensor, since the M-CNTs can poke through the thin dielectric to cause huge leakage, as shown in Fig. S3. Therefore, SBS encapsulation of the transistor part needs to be thick enough to prevent the leakage, while not too thick to secure a good connection between the top and bottom electrodes. Since SBS encapsulation only covers the transistor, it creates a via structure for the lower electrode, and then a global top electrode (embedded in elastomer) is transferred to cover both via and transistors. The tactile sensor is formed at the via region, which is the most sensitive region to pressure because of the existence of the air gap. The detailed fabrication process is shown in Method and Fig. S52.

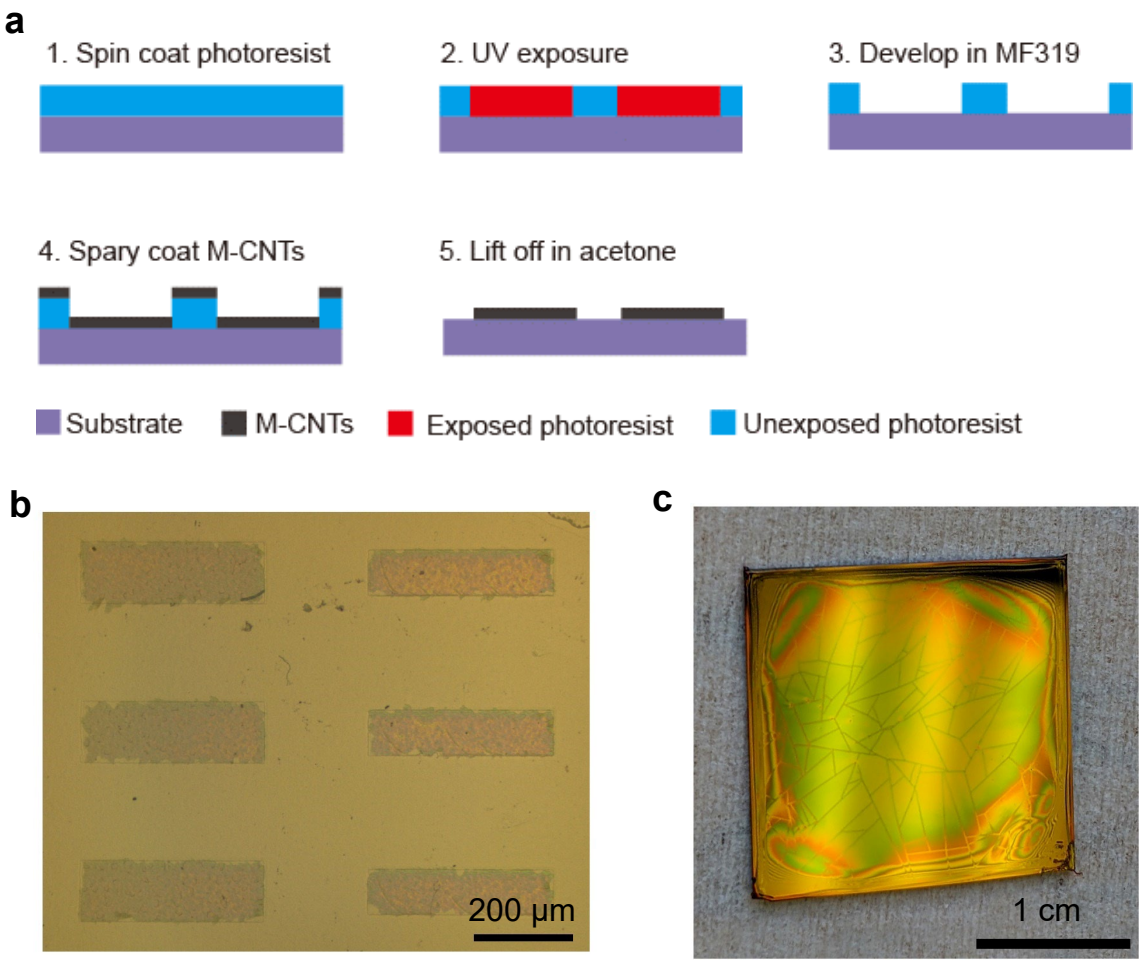
As shown in Fig. S53, to investigate the optimal SBS thickness, a series of tactile sensors was divided into two groups, and half of them were covered by SBS encapsulation to mimic the source/drain electrode of the transistor. When SBS thickness is ~2.7 μm, the probability of leakage between the upper electrode and the 'transistor' (if the measured resistance is smaller than 100 MΩ, we regard it as leakage) is about 16.7%, while the contact resistance between the top and bottom electrodes is maintained below 2 kΩ. If SBS thickness is increased to ~5.1 μm, the probability becomes 0%, while the contact resistance is still maintained below 2 kΩ Therefore, SBS with a thickness of ~5 μm is chosen to make tactile sensors for the demonstration.

As shown in Fig. 5, to construct an active-matrix tactile sensor array, one lower electrode is connected to the ground, another is connected to the drain electrode of the transistor, while the source electrode is connected to Bit line, and the gate electrode is connected to Word line. There are two ways to use the active-matrix tactile sensor array, one is for 3D object sensing (Fig. S54), and another is for flat conducting pattern sensing (Fig. S55). For 3D object sensing, when the active-matrix tactile sensor array touches the object, and raised part will deform the tactile sensor to reduce the sensor resistance, so the pixel will show a high on-state drain current during mapping. The on-state drain current mapping will show the shape of the objects. For flat conducting pattern sensing, the global upper electrode will be removed, and the active-matrix tactile sensor array will directly contact with the flat conducting pattern. In this way, all tactile sensors will deform, but

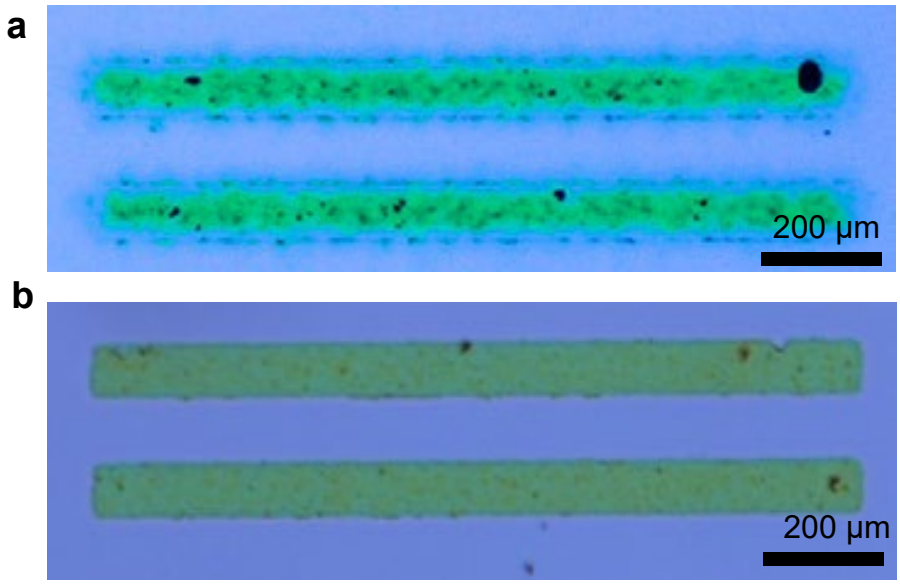
only those pixels with the existence of the conductors will show a high on-state drain current, so on-state drain current mapping will show the shape of the patterns. In the braille demonstration, we use the second way, since we can make very small braille patterns using photolithography.

Supplementary Note V. Bonding stretchable electronics to flexible electronics.

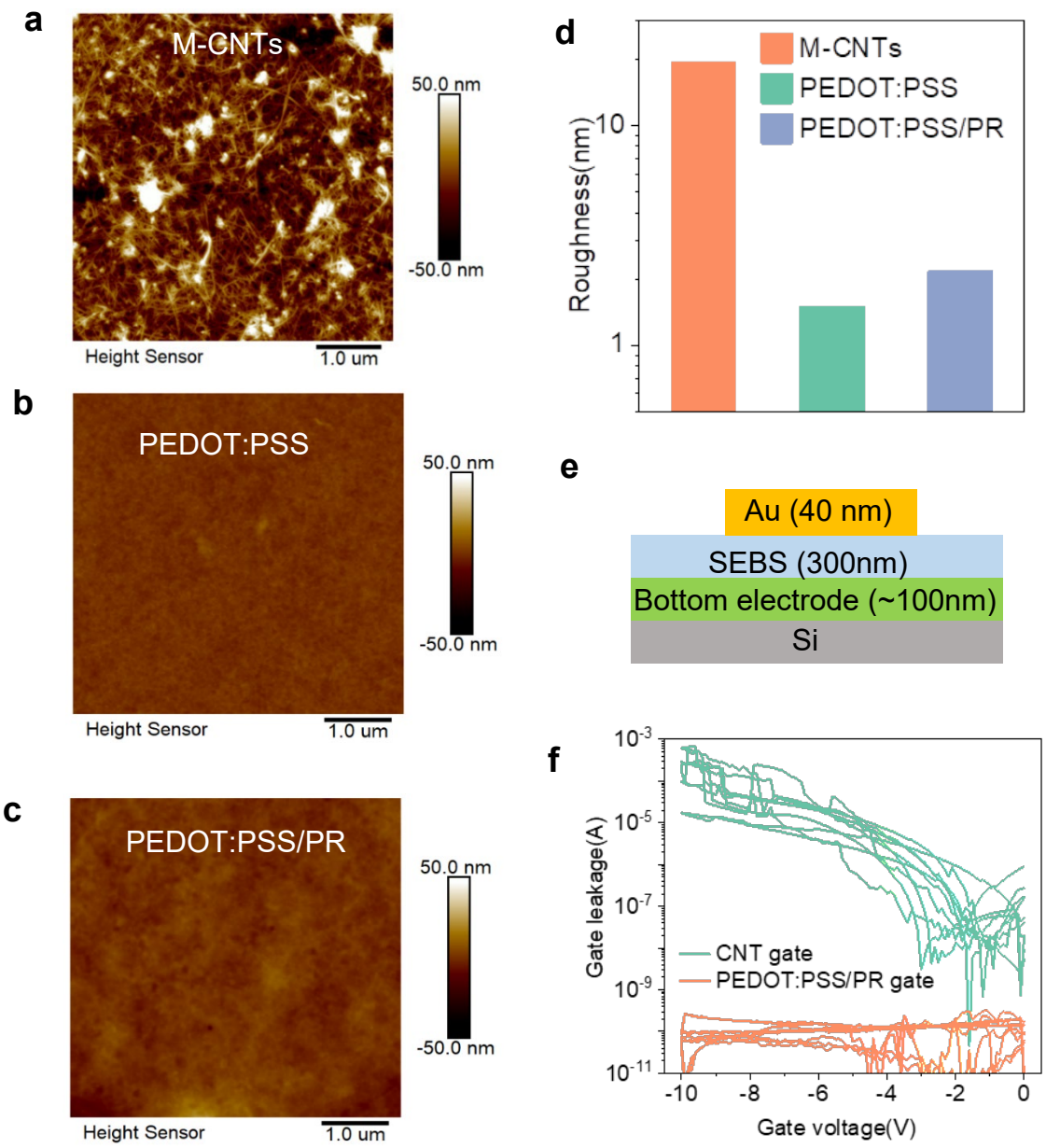
To access the intrinsically stretchable active-matrix tactile sensor array, we used flat flexible cable (FFC) and anisotropic conducting film (ACF) tape to bond. As shown in Figs. S56-59, we've compared three strategies. The first way is to bond with EGaIn interconnect and then release from Si substrate. Although the initial electrical connection was good, after releasing, the resistance increased from below 1 kΩ to larger than 1 MΩ. The electrical degradation probability came from the large deformation in the FFC/EGaIn interface because of the large stiffness mismatch between the thin stretchable substrate (~3 μm) and FFC cable. The second way is to first transfer thin active-matrix tactile sensor array to a thick SEBS substrate (~100 μm) on OTS/Si, then bond EGaIn interconnect with FFC cable, and finally release from OTS/Si. Using this way, the electrical connection can be well maintained after releasing from OTS/Si. The third way is to bond with Cr/Au interconnect rather than EGaIn interconnect, but the pressing operation helping the bonding would generate cracks on the Cr/Au interconnect, so the electrical connection couldn't be formed. Therefore, we used the second way, e.g., first transferring to a thick SEBS substrate and then bonding with EGaIn interconnect, to demonstrate shape sensing and braille recognition. To increase the mechanical robustness of the bonding, we use PI tape to cover the FFC/EGaIn interface to reduce the concentrated stress. Even stretched to ~50%, the electrical connection of flexible (FFC cable) and stretchable electronics (EGaIn interconnect) could still be well maintained.



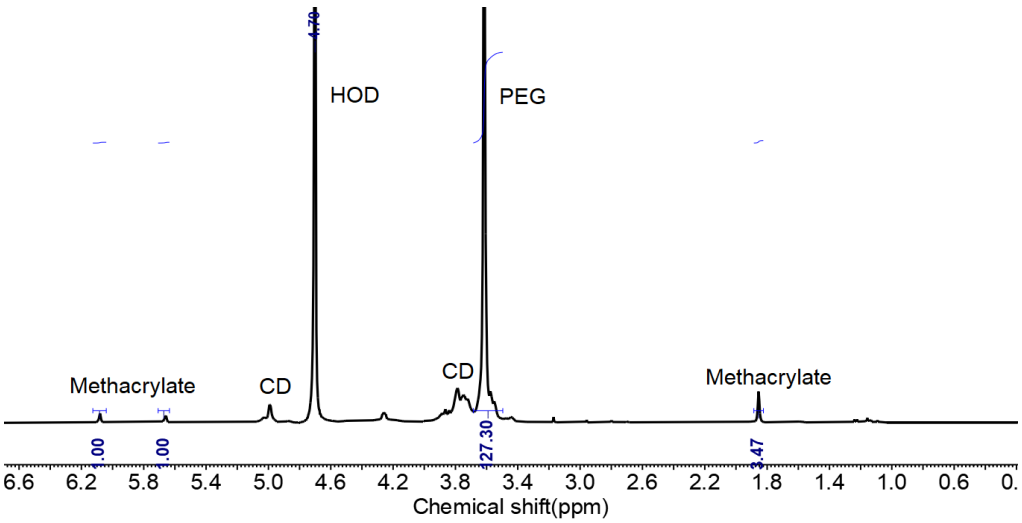
Supplementary Fig. 1. Patterning of M-CNTs electrodes using traditional lithography. a, Lift-off fabrication process of M-CNTs electrodes using a single-layer positive photoresist (AZ 1512) with a thickness of about 1.5 μm. **b**, Optical microscope image of the fabricated M-CNTs electrodes, showing highly rough edges. This is because M-CNTs would form a continuous web across the entire substrate with strong inter-tube van der Waals forces. **c**, Large cracks of double-layer LOR 3A/AZ 1512 with a thickness of ~2 μm /~1.2 μm on a soft substrate. LOR 3A is a photo-insensitive lift-off resist material, and AZ1512 is a photo-sensitive lift-off resist material.



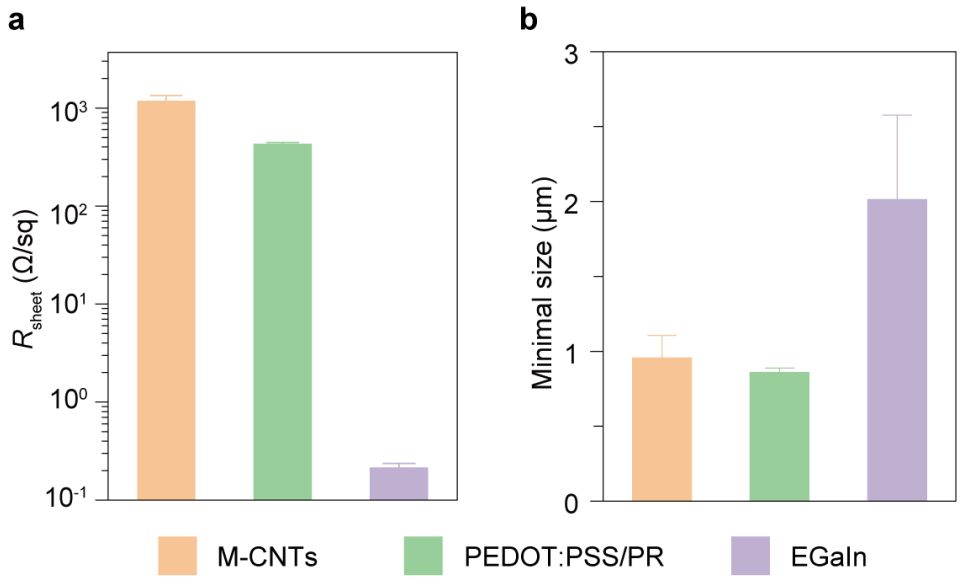
Supplementary Fig. 2. Comparison of edge roughness from M-CNTs fabricated via different processes. a, Optical microscope image of the fabricated M-CNTs electrodes via spray-coating through a shadow mask. Because of the gap between the metal mask and the substrate, M-CNTs solution would inevitably leak into the channel areas, causing fuzzy edges of the S/D electrodes and potential shorting of the channel when scaling down the channel length. **b**, Optical microscope image of M-CNTs patterned using the metal-assisted lift-off method. The fabricated M-CNTs electrodes showed clear boundaries so the channel length can be easily scaled down to sub-micrometers without the shorting issue.



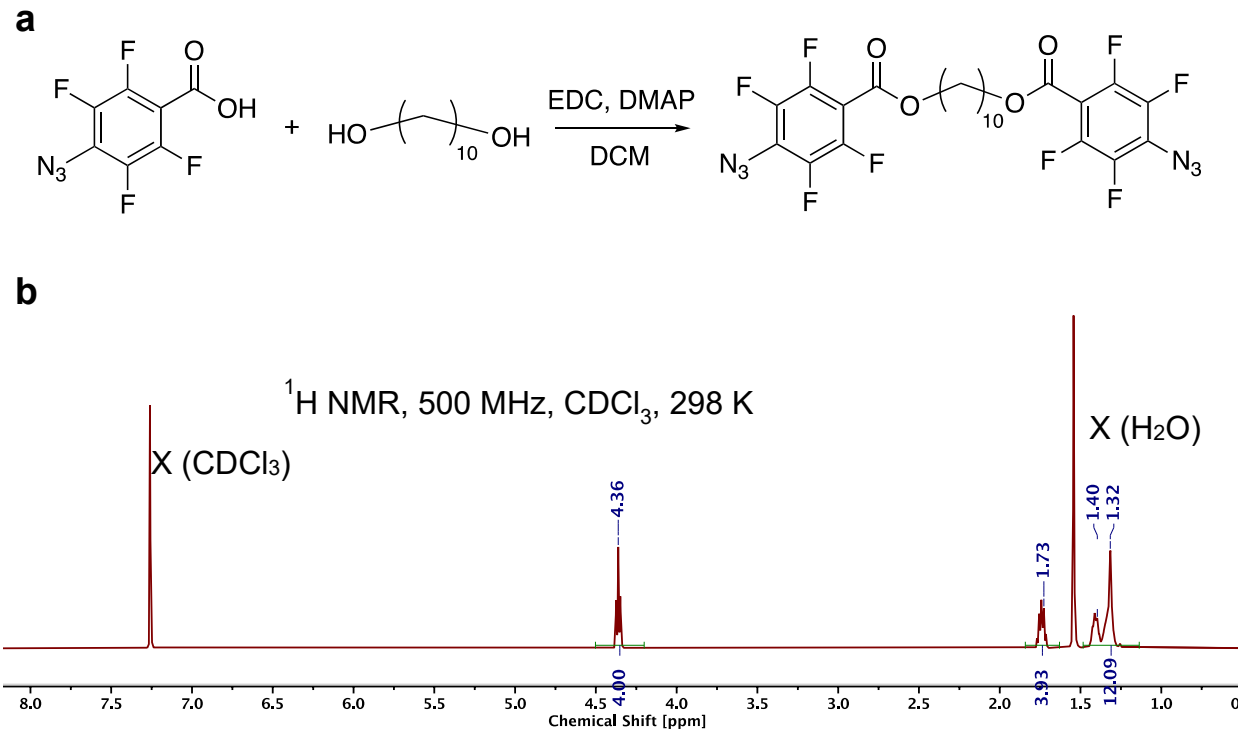
Supplementary Fig. 3. Comparison of leakage current using different conductors as bottom electrodes. a-c, AFM height image of spray coated M-CNTs (**a**), spin-coated PEDOT:PSS (**b**) and spin-coated PEDOT:PSS/PR (**c**). **c**, AFM height image of. **d**, Comparison of surface roughness between PEDOT:PSS and M-CNTs electrodes. The average was calculated for 256∑256 data points from the two AFM images. **e**, Device structure for measuring gate leakage. SEBS layer with a thickness of ~300 nm was spin-coated on bottom electrodes. Top electrodes were made by evaporating Au through a shadow mask. M-CNTs electrodes showed much higher leakage current because of the high surface roughness. The area of the top electrodes is 0.1 mm^2. **f**, Measured dielectric leakage current using PEDOT:PSS/PR and M-CNTs as bottom electrodes. Five devices were measured for each electrode.



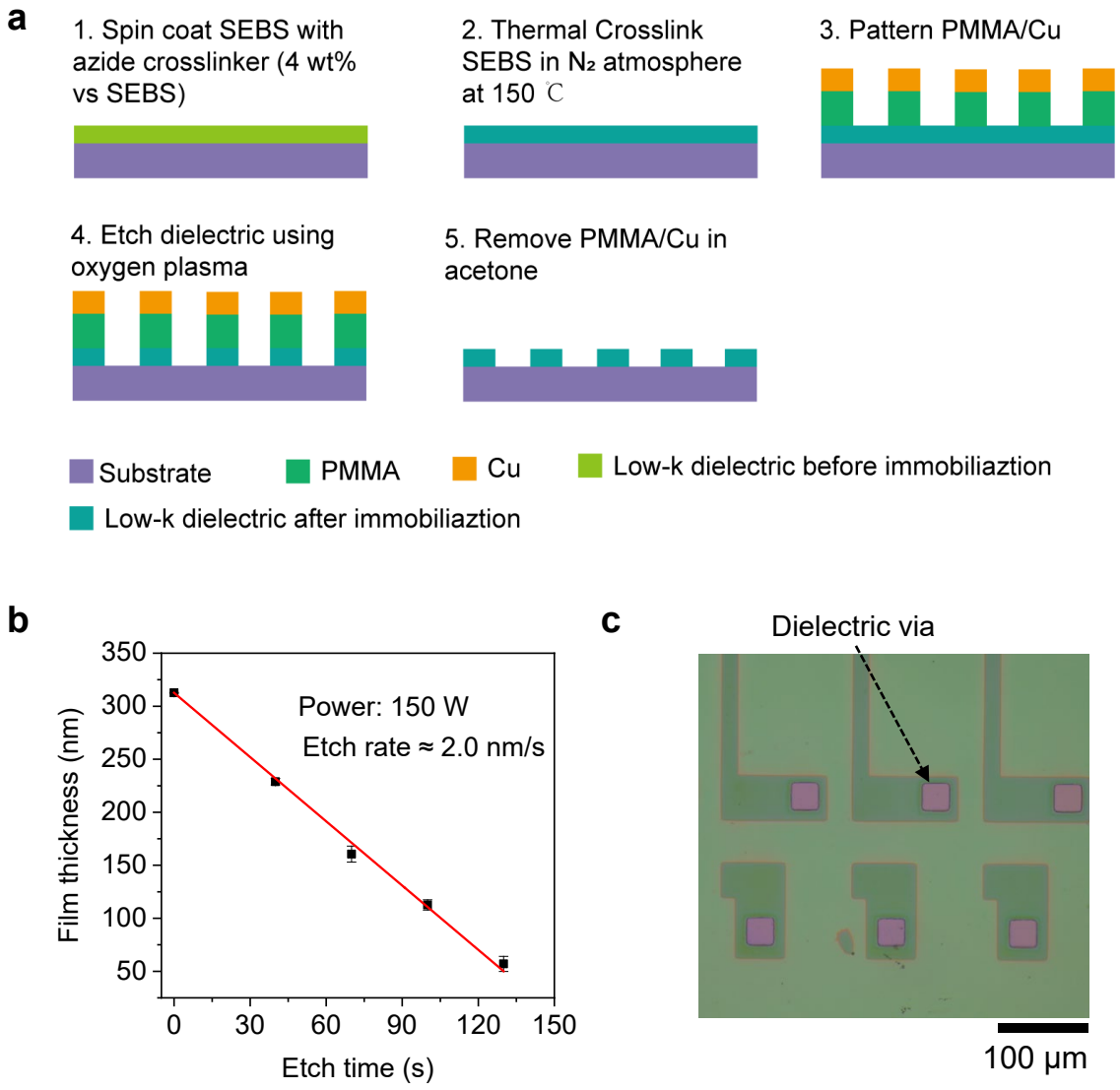
Supplementary Fig. 4. Highly conductive and stretchable PEDOT:PSS film with the topological supramolecular network. NMR spectrum of PR-PEGMA$_9$ in DMSO-d_6. Detailed synthesis and characterization of PR-PEGMA can be found in ref. S4.



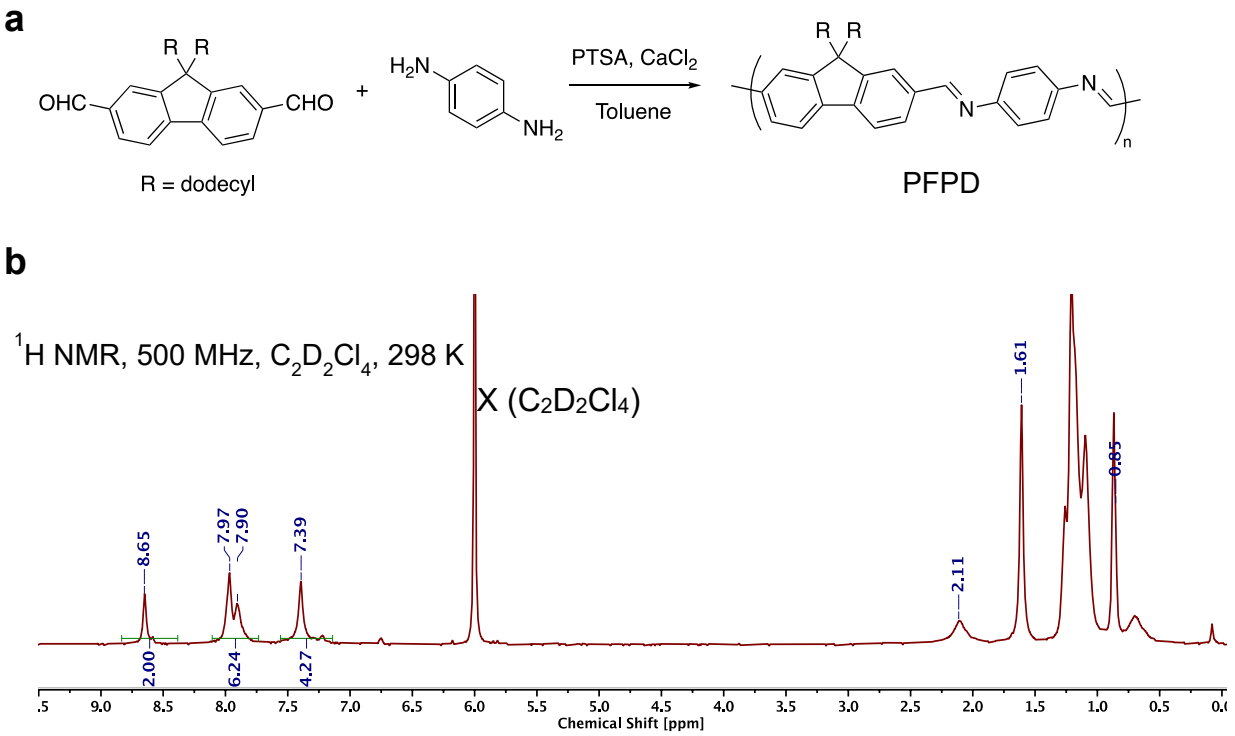
Supplementary Fig. 5. a, Sheet resistances of three different conductors. Ten electrodes were averaged for M-CNTs, four electrodes were averaged for PEDOT:PSS/PR, and data from twelve electrodes were averaged for EGaIn. **b**, Minimal feature sizes of three different conductors. Twelve locations were averaged for PEDOT:PSS/PR, eighteen locations were averaged for EGaIn, and data from six locations were averaged for M-CNTs.



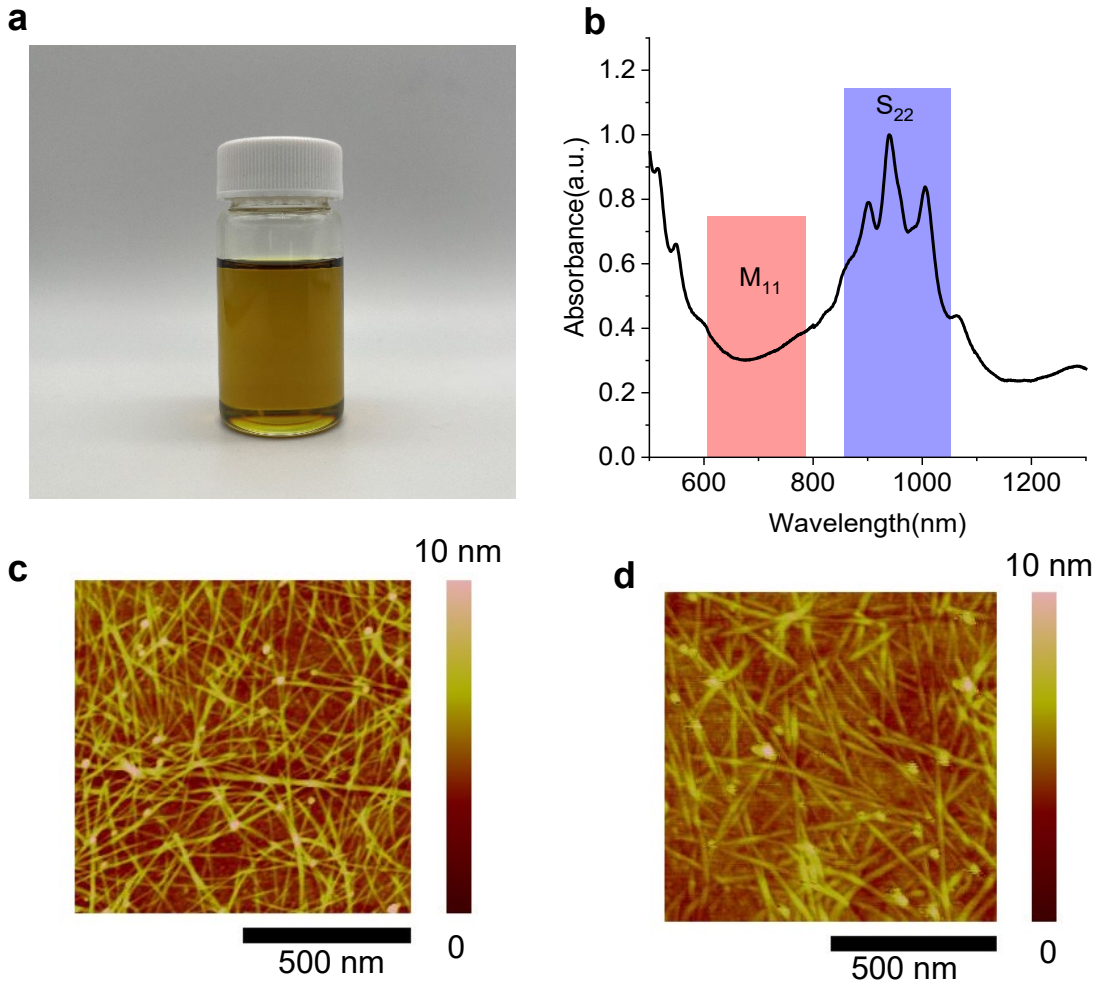
Supplementary Fig. 6. C10-azide based crosslinker for SEBS dielectric. a, Synthesis of C10-azide crosslinker: 4-azido-2,3,5,6-tetrafluorobenzoic acid (0.90 g, 3.83 mmol), DMAP (0.047 g, 0.038 mmol), EDC (0.77 g, 4.00 mmol), and 1,10-decanediol (0.30 g, 1.74 mmol) were added into a 200 mL round-bottom-flask. 100 mL anhydrous DCM was added at 0 ˚C. The reaction was stirred for 18 h. The mixture was poured into 100 mL water and extracted with diethyl ether (3×50 mL). The organic layers were combined and dried over $MgSO_4$. The crude product was purified by flash chromatography with SiO_2 column and eluent (hexane/ethyl acetate=5/1). The product was collected as a white solid (1.00 g, 95%). **b**, NMR spectrum of the C10-azide crosslinker. ^{1}H NMR (500 MHz, CDCl3, δ/ppm): 4.36 (t, 4H, *J*=6.6 Hz), 1.74 (t, 4H, *J*=6.8 Hz), 1.48-1.21 (m, 12H).



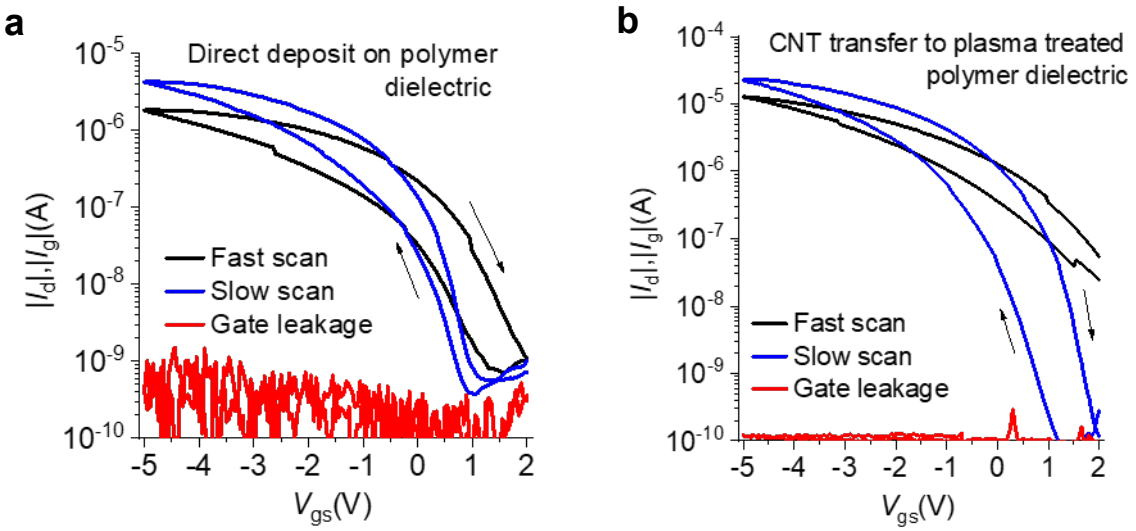
Supplementary Fig. 7. Patterning of low-κ SEBS dielectric layer. a, Schematic diagram showing the process of patterning low-κ SEBS dielectric layer based on photolithography and oxygen plasma etching. Cu was used to protect other areas. This method can be used to pattern low-κ polymer dielectric SEBS using a more convenient direct-writing lithography tool with 385 nm wavelength other than a UV lamp with 254 nm wavelength. **b**, Etch rate of crosslinked SEBS H1062 using March Instruments PX-250 Plasma Asher. Data from three locations were averaged for each etching time. **c**, Optical microscope image of dielectric vias on PEDOT gate electrodes.



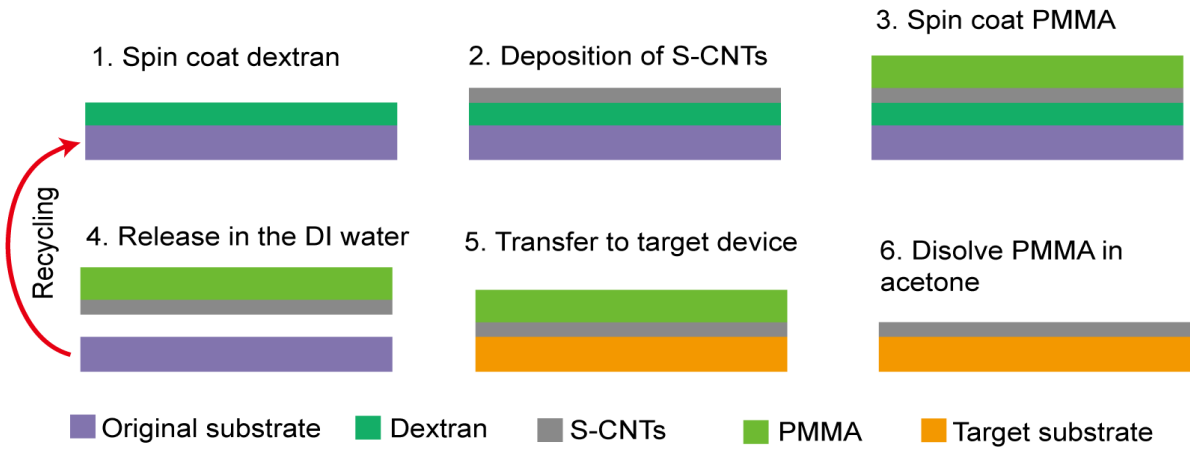
Supplementary Fig. 8. PFPD for CNT sorting. a, Synthesis route of PFPD. Into a 50-mL Schlenk tube, 9,9-didodecyl-2,7-dicarbaldehyde-fluorene (243 mg, 0.43 mmol), 1,4-diaminobenzene (47 mg, 0.43 mmol), PTSA (4 mg, 0.02 mmol), anhydrous $CaCl_2$ (60 mg), and anhydrous toluene (15 mL) were added under N_2. The tube was degassed with freeze-pump-thaw for 3 times and sealed. The reaction was stirred at 110 ˚C for 48 h. After completion, dry K_2CO_3 (20 mg) was added into the mixture and stirred for 30 min at 110 ˚C. The mixture was filtered through a nylon membrane (0.45 μm). The Solvent was removed under reduced pressure and the residue was washed with hexane. The polymer was collected as a yellow solid (0.20 g, 74%). **b**, NMR spectrum of PFPD. ^{1}H NMR (500 MHz, C_2D_2Cl4, δ/ppm): 8.65 (br, 2H), 7.97-7.91 (6H), 7.39 (br, 4H), 2.11 (br, 4H), 1.26-1.09 (36H), 0.87 (br, 6H), 0.70 (br, 4H). HT-GPC (180 ˚C, trichlorobenzene): M_n = 10 kg/mol, PDI = 2.8.



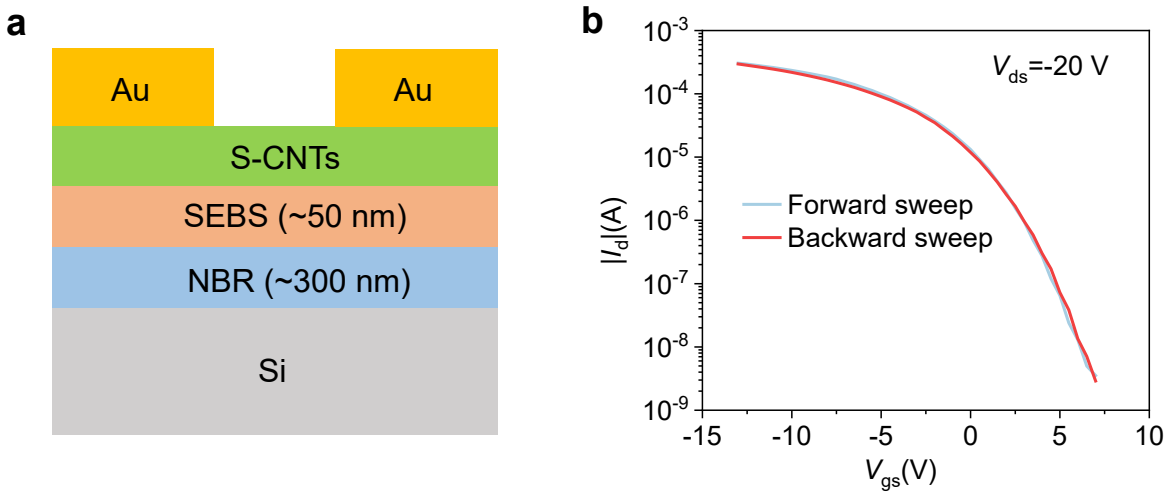
Supplementary Fig. 9. CNT sorting and deposition. a, Photo of sorted CNT solution. **b**, Absorption spectra of as-sorted SWNTs. M_{11} is the first inter-band transition of m-SWNTs. S_{22} is the second inter-band transition of s-SWNTs. The S-CNT solution was prepared by sonicating PFPD/CNT mixed solution (5 mg of PFPD and 5 mg of raw RN-020 SWNTs in 20 ml toluene) for 30 min at an amplitude level of 45% (Cole Parmer ultrasonicator 750 W) while externally cooled with a dry ice bath, centrifuged at 8000 rpm for 5 mins 14 °C to remove most of the un-dispersed residues, centrifuged (Sorvall lynx 4000) at 17000 rpm for 25 min at 14 °C for further purification, and then 80% of the upper supernatants were collected for use. AFM height images of as-deposited S-CNTs networks on Si/SiO_2 substrate (**c**) and on NBR substrate (**d**). Both substrates were modified with poly-L-lysine to improve the wettability of the CNT solution, which can help to increase the CNT density on substrates. CNT deposition process: substrate (Si/SiO_2 or polymer substrate) was treated by oxygen plasma (March Instruments PX-250 Plasma Asher, 100 W) for 1 s, modified by soaking in a poly-L-lysine solution (from sigma, P4832-50 mL) for 30 mins, washed by DI water, dried by N_2, immersed into the S-CNT solution for 48 hours, washed by soaking in toluene twice for 10 mins each time, dried by N_2, and then baked at 150°C for 30 mins in ambient.



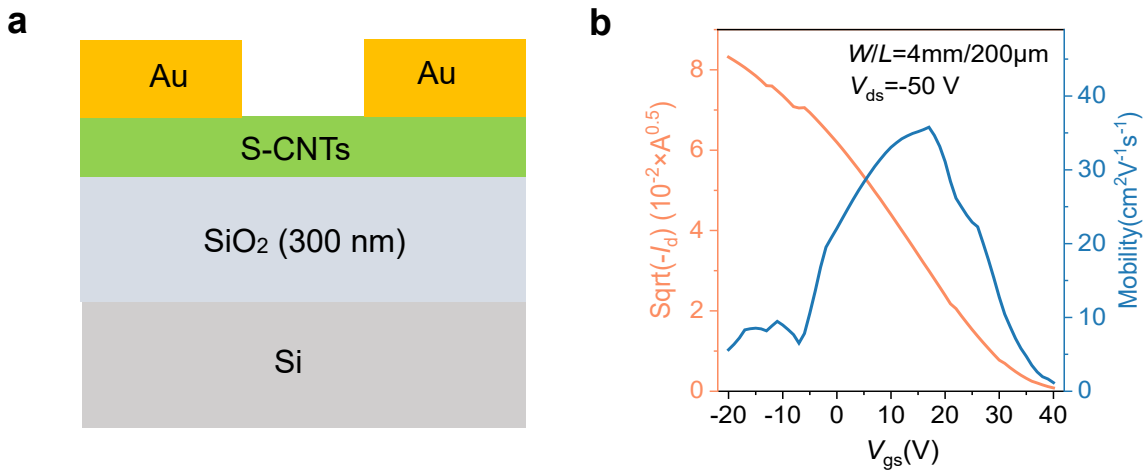
Supplementary Fig. 10. Transfer characteristics of transistors with various CNT deposition methods. a, CNTs were directly deposited on polymer dielectric by soaking into CNT solution for two days. **b**, CNT films deposited onto dextran were transferred onto plasma-treated polymer dielectric. The polymer dielectrics (crosslinked SEBS on NBR) were treated by oxygen plasma at 100 W for 1s. The large hysteresis and scanning speed-dependent drain current implied that ions were injected into the polymer dielectric by oxygen plasma. W_{ch}=600 μm, L_{ch}=100 μm, and the thickness of NBR/SEBS is about 300/50 nm. Plasma represents March Instruments PX-250 Plasma Asher. Slow, medium and fast sweep modes are default modes of Keithley 4200.



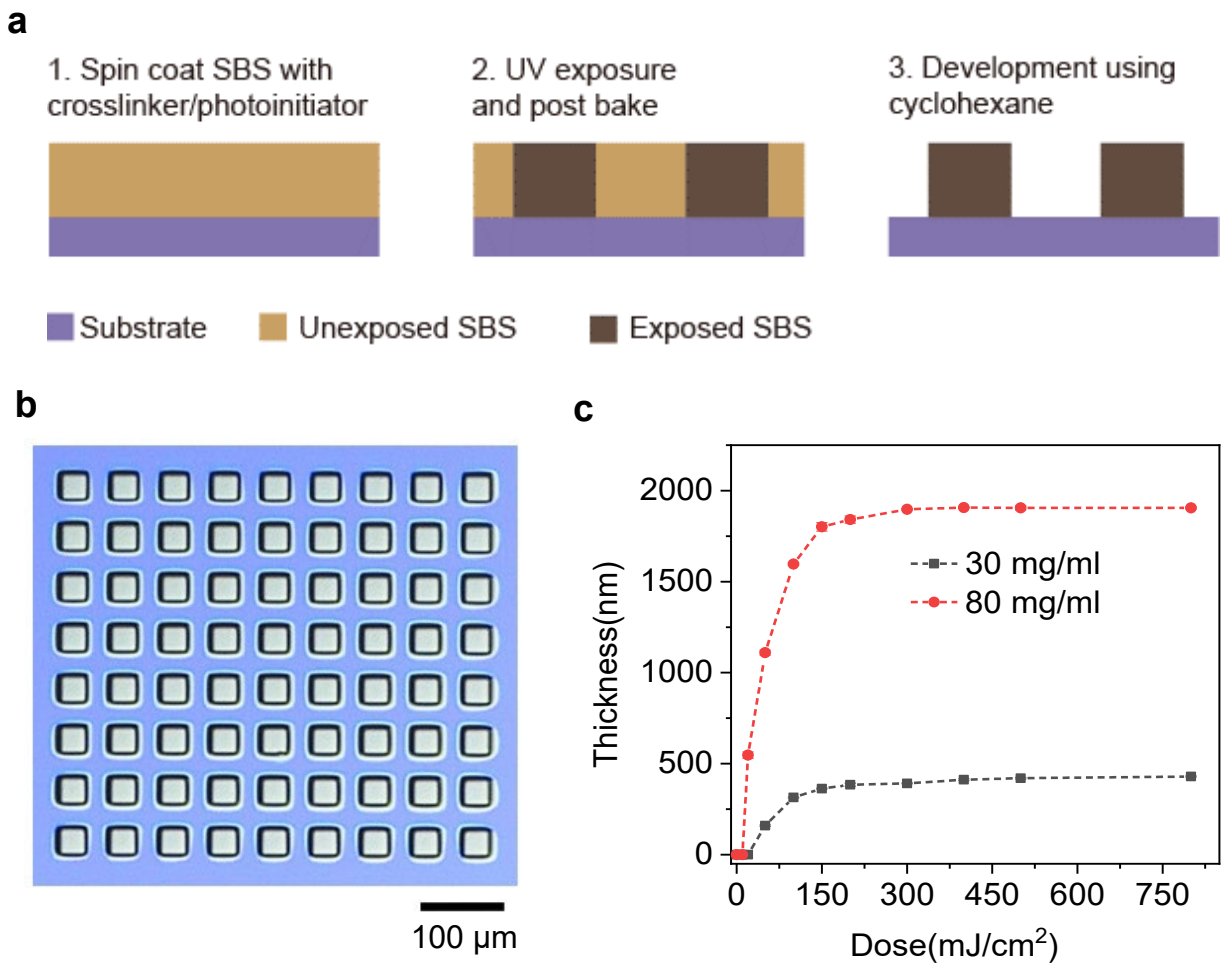
Supplementary Fig. 11. Schematic diagram showing the process of transferring S-CNTs as the semiconductor channel. Dextran: ~100 nm spin coated from 50 mg/ml dextran in water. PMMA: ~500 nm spin coated from 40 mg/ml PMMA in anisole. The rigid substrate can be recycled after releasing the PMMA layer. Compared to using Si/SiO_2 as the temporary transfer medium, water-soluble dextran does not require the use of 'harsh' hydrofluoric acid (HF) to etch SiO_2, making the transfer process much safer and more cost-effective, compared with ref. S3. The yield of the transfer step using PMMA 495K from MicroChem is around 95%, which can be further improved by increasing PMMA thickness. Compared to the transfer process in Figure S10, this process does not involve plasma treatment of the SEBS polymer dielectric surface, which can introduce current-voltage hysteresis.



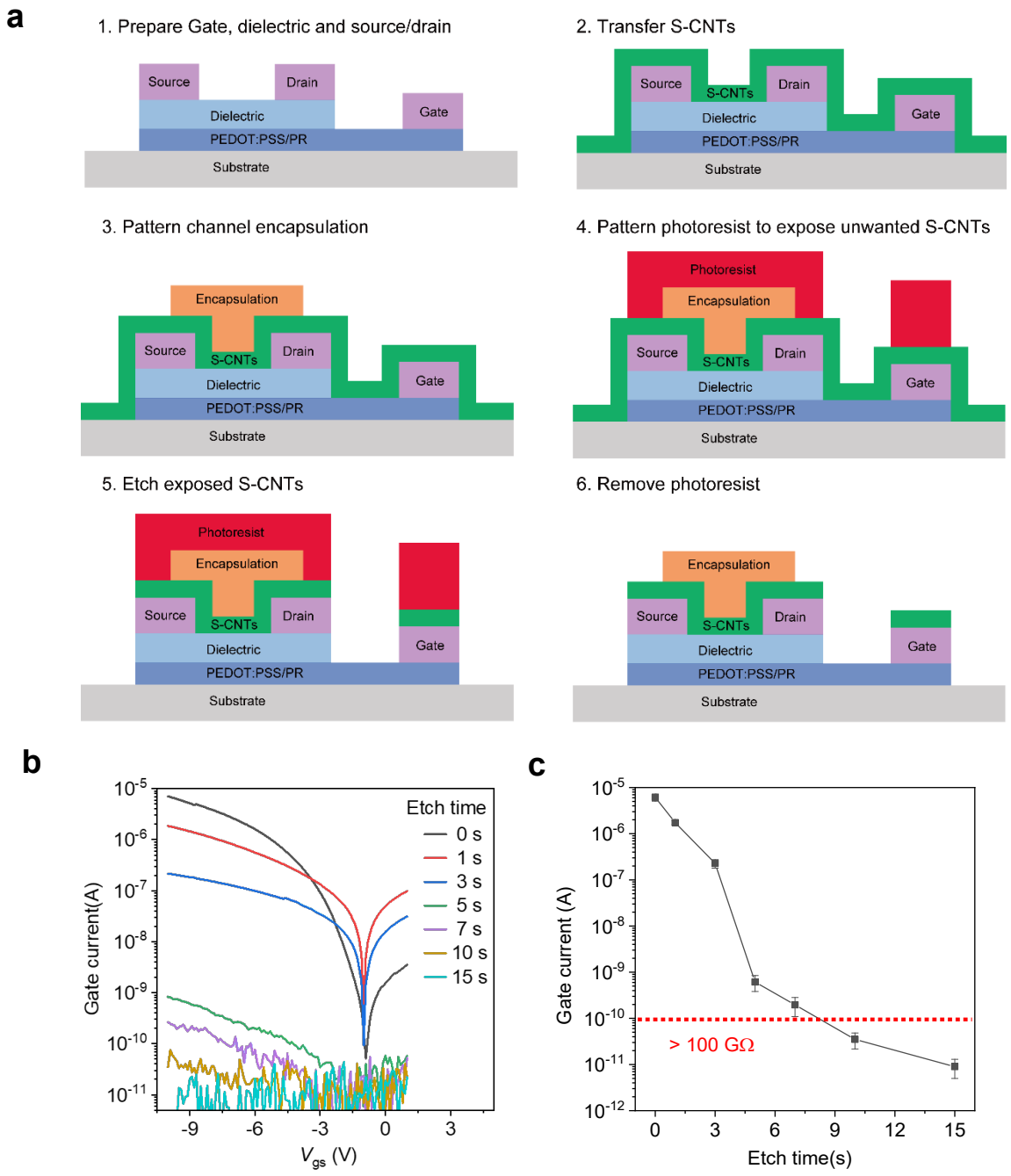
Supplementary Fig. 12. Hysteresis measurement of the transistor using PMMA-assisted transferred S-CNTs on polymer dielectric. a, Schematic of the device structure. **b**, Transfer characteristic with negligible hysteresis. On/off ratio is higher than 10^5. W_{ch}=1 mm, L_{ch}= 50 μm.



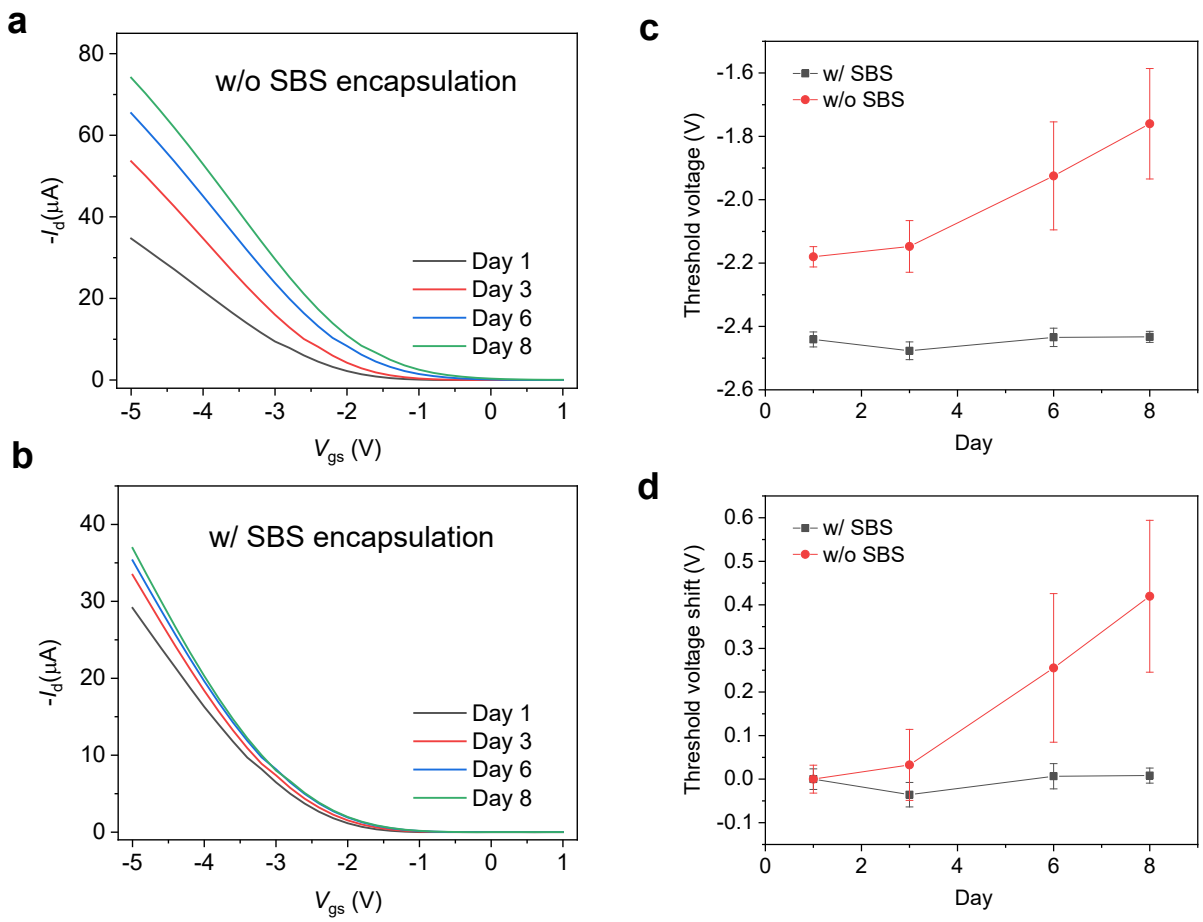
Supplementary Fig. 13. Characteristic of a transistor with S-CNTs directly deposited on Si/SiO_2 substrate. a, Device structure. **b,** Carrier mobility extraction. V_{ds} =- 50 V.



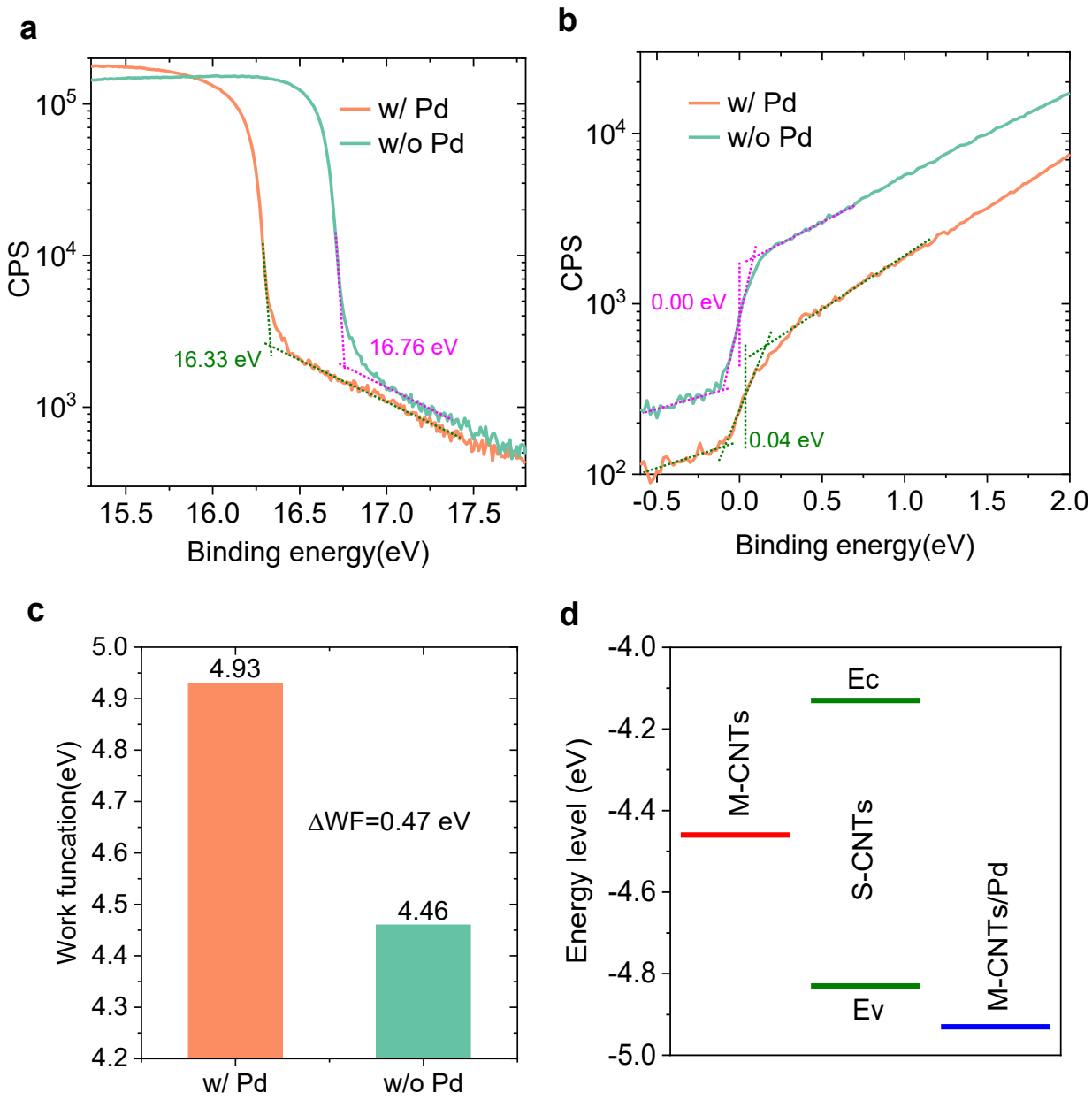
Supplementary Fig. 14. Patterning of low-κ dielectric layer SBS. a, Schematic diagram showing the process of patterning SBS via direct photopatterning. Crosslinker is PETMP (4wt%), and photoinitiator is BAPO (4wt%). **b**, Optical microscope image of SBS array. **c**, Relation of the thickness of patterning thickness and exposure dose.



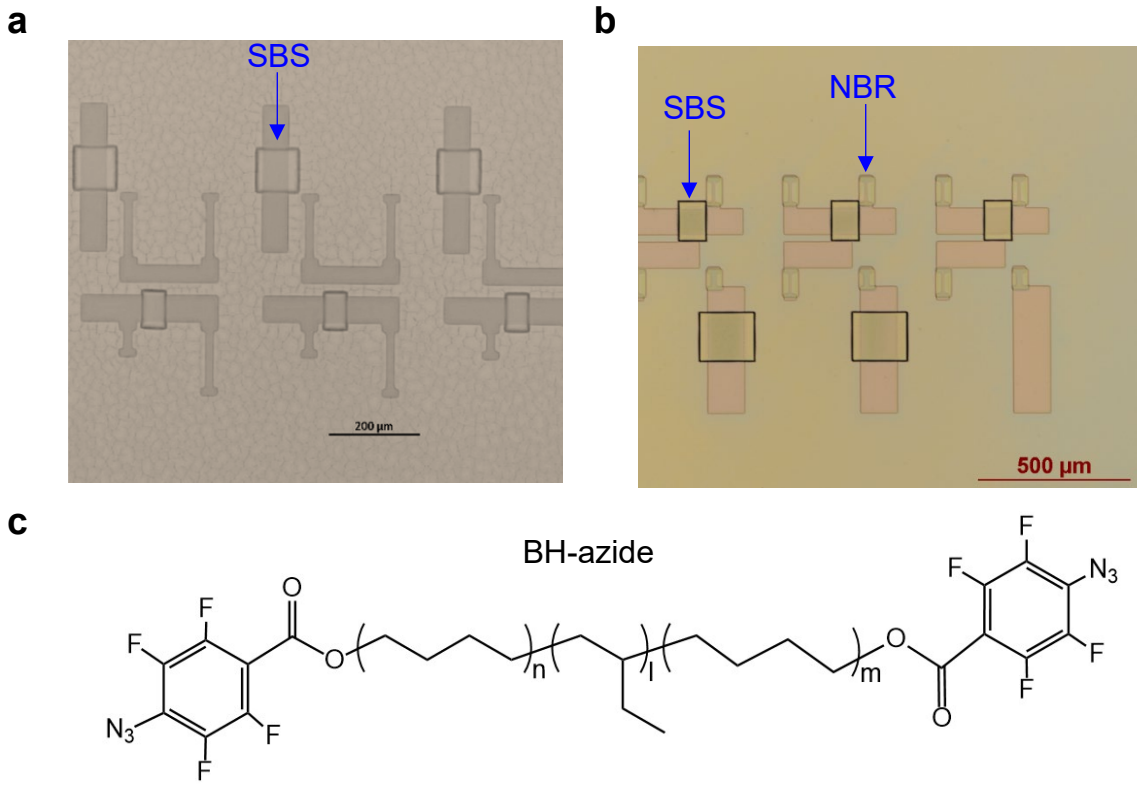
Supplementary Fig. 15. Patterning of semiconducting CNTs. a, Schematic diagram showing the process of patterning S-CNTs. **b**, Gate leakage measurement current for different etching time. Oxygen plasma using March Instruments PX-250 Plasma Asher model and 100 W power. **c**, Relation of the gate leakage and etching time.



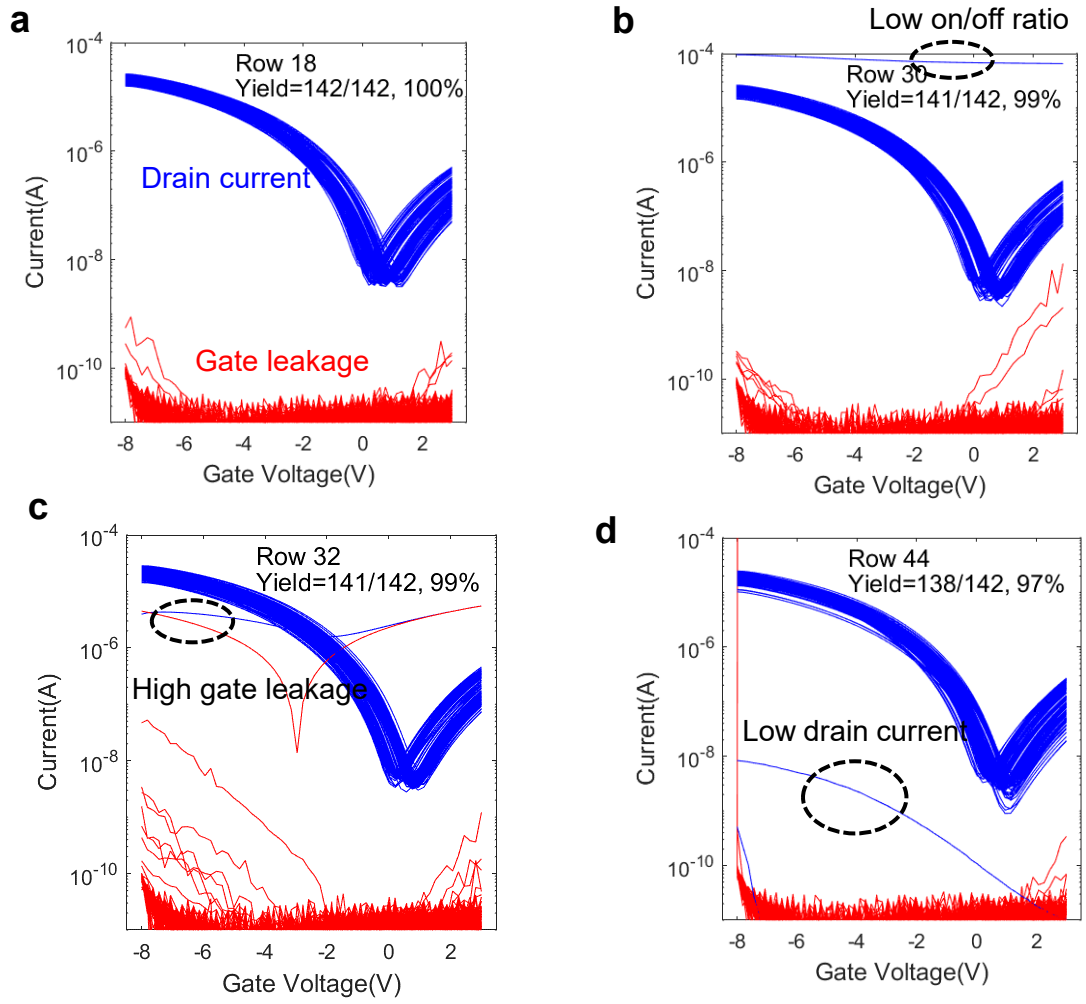
Supplementary Fig. 16. Channel encapsulation for improved device stability in air. a, Transfer curves over time for transistors without SBS encapsulation. **b**, Transfer curves over time for transistors with ~1 μm SBS encapsulation. **c**, Comparison of threshold voltage over time for w/o or w/ encapsulation. **d**, Comparison of threshold voltage shift over time for w/o or w/ encapsulation. Humidity is about 54%, and the temperature is about 21 ℃. Data from eight transistors were averaged for each condition.



Supplementary Fig. 17. Increased work function by Pd. a-b, Work function measured from a M-CNT film (**a**) and M-CNT/Pd (**b**) by UPS (He I light source). **c**, Work function is increased by 0.47 eV with Pd. **d**, Energy levels of S-CNTs, M-CNTs, and M-CNT/Pd.

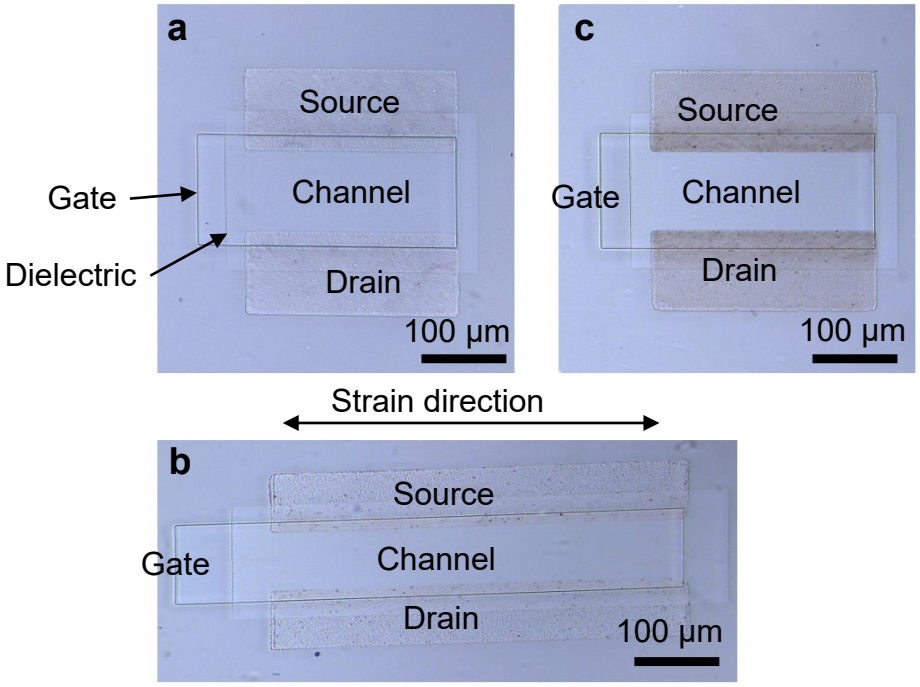


Supplementary Fig. 18. Solvent resistance comparison of different stretchable substrates. a-b, Optical microscope images of (**a**) C10-azide crosslinked SEBS H1062 and (**b**) BH-azide crosslinked SEBS H1062 after jumper dielectric layer SBS patterning. BH-azide crosslinked SEBS showed a better solvent resistance to toluene. **c**, Chemical structure of BH-azide crosslinker. Detailed synthesis and characterization of BH-azide can be found in ref. S4.

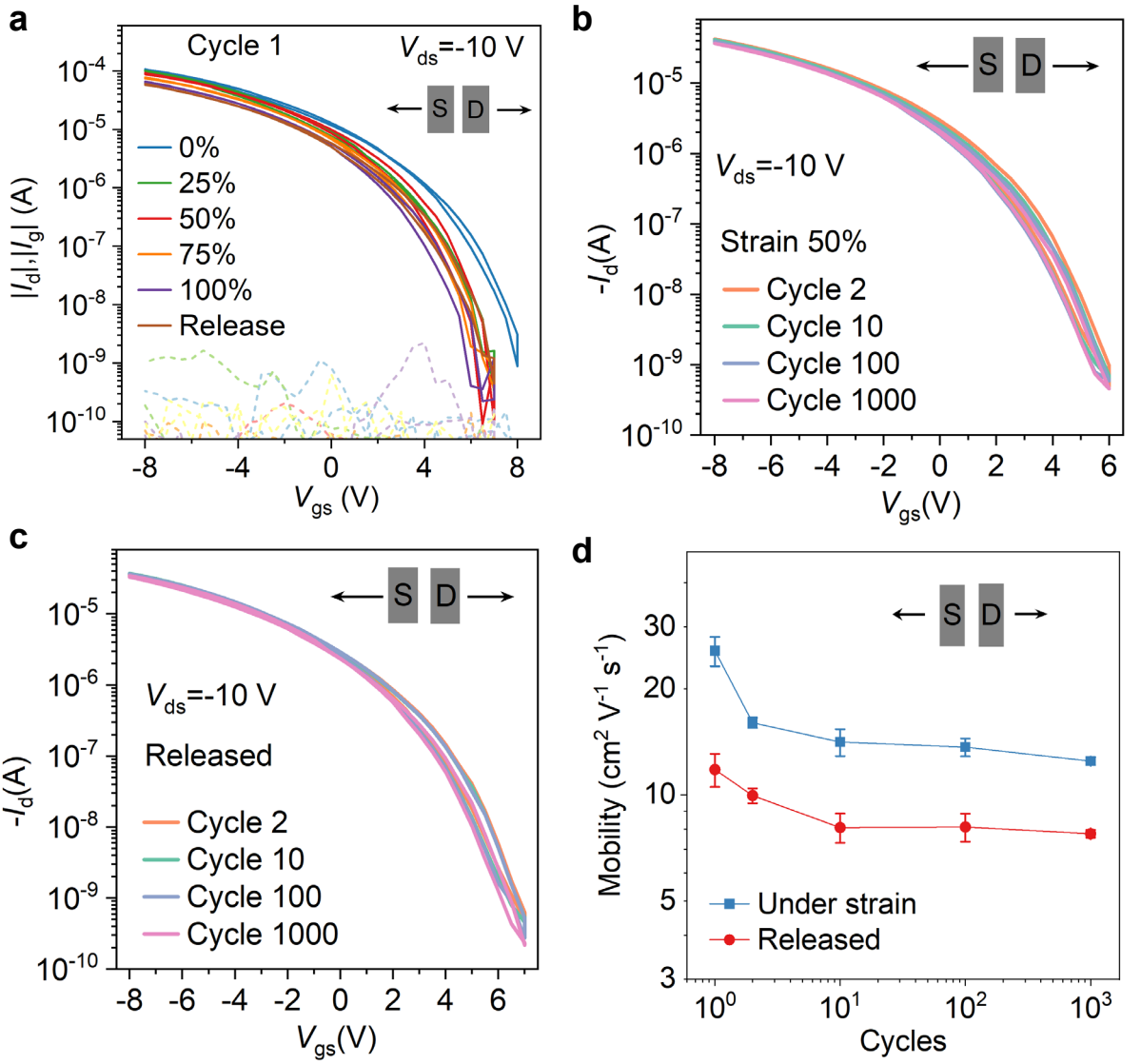


Supplementary Fig. 19. Characterization of device yield and uniformity of intrinsically stretchable transistor array shown in Figure 3. a-d, Transfer curves of different rows of CNT transistors. We defined working devices as those with on/off ratios>500, on current>3 μA, and drain current one order of magnitude higher than gate current for the calculation of device yield.

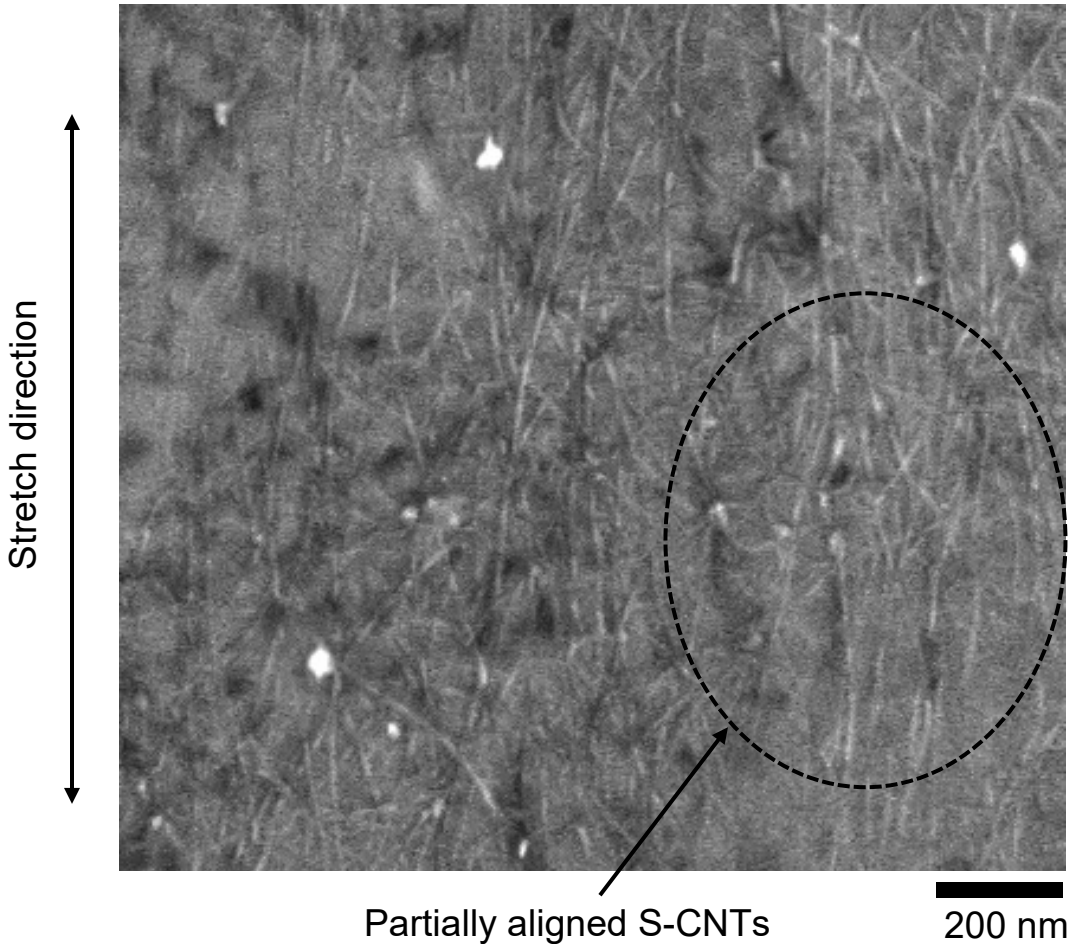
Supplementary Fig. 20. Transfer curves of all 10,082 CNT transistors measured by an automatic probe station. In total, 10,018 transistors showed an on-state drain current (I_{on}) higher than 3 μA (V_{ds} = -3V, V_{gs} = -8V) and a drain current on/off ratio higher than 500, leading to a device yield of up to 99.37%, which is higher than other intrinsic stretchable transistor arrays.



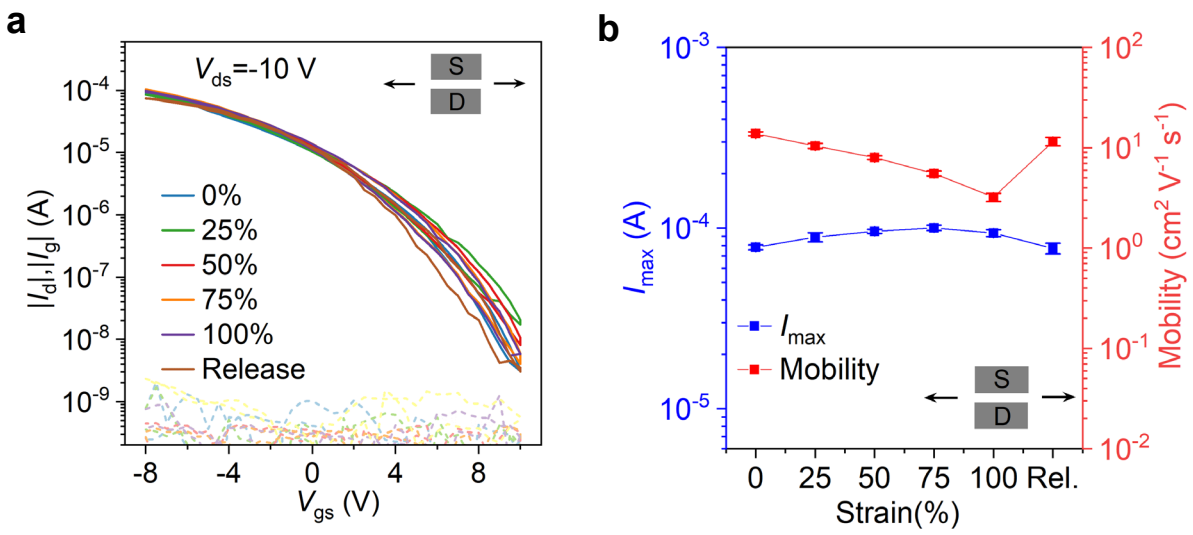
Supplementary Fig. 21. Optical microscope images of CNT transistors under different strain in the direction perpendicular to the charge transport direction. a, 0% strain (initial). **b**, 100% strain. **c**, 0% strain (released).



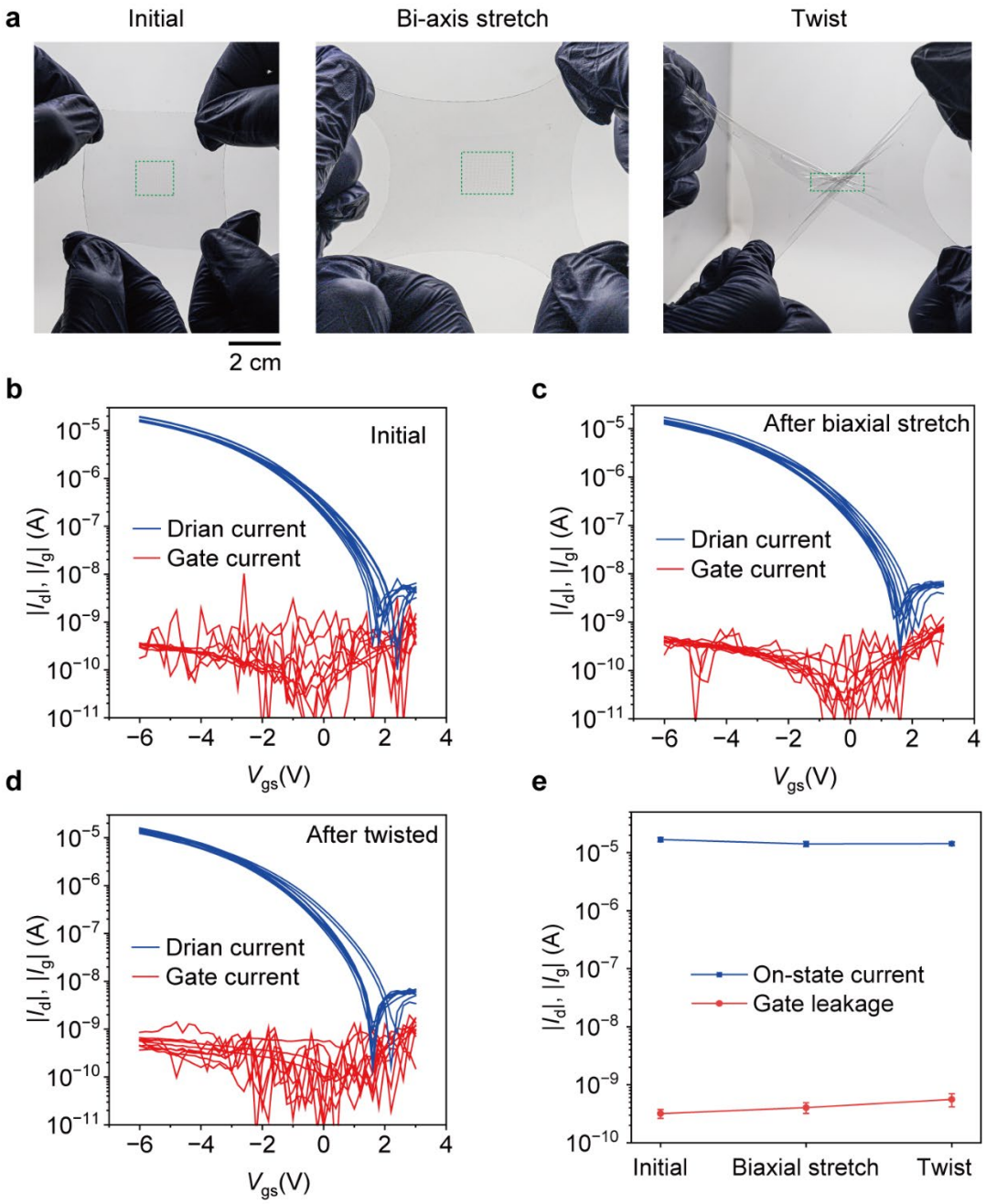
Supplementary Fig. 22. Characteristics of intrinsically stretchable transistors under different strains and cycles. a, Transfer curves under stretching along the charge transport direction from 0% to 100% strain and subsequently released. W_{ch}/L_{ch} =250/100 μm. **b-c**, Transfer curves after the first strain cycle in (**a**) and subsequently under repeated stretching/release cycles for 1000 times. Transfer curves were obtained under 50% strain (**b**) and after releasing (**c**). **d**, Mobilities obtained under 50% strain and in the released states during 1,000 stretching cycles. Data from three transistors were averaged for each cycle.



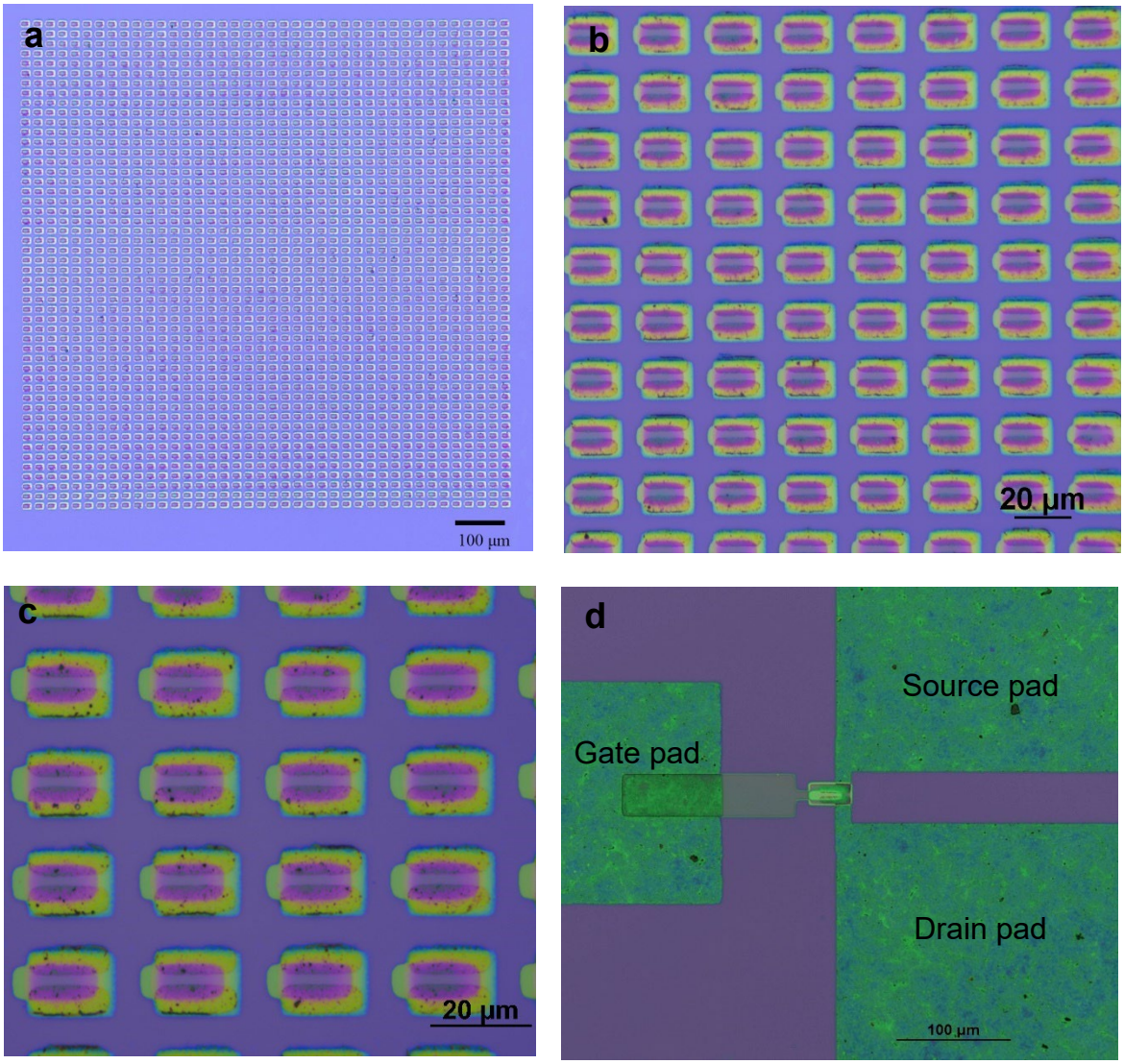
Supplementary Fig. 23. SEM image of S-CNTs under strain. Strain-induced alignment may increase the charge mobility of the intrinsically stretchable transistors.



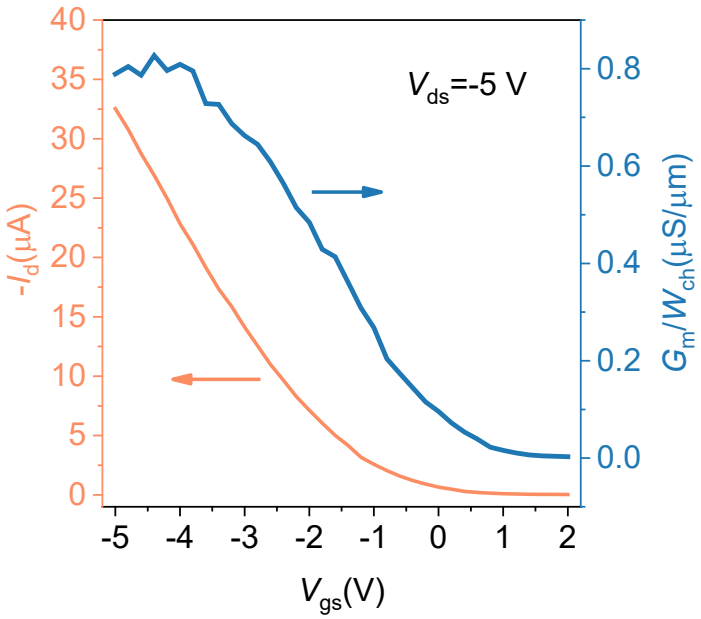
Supplementary Fig. 24. Electrical performance of intrinsically stretchable transistors under different strains and cycles. a, Transfer curves under stretching perpendicular to the charge transport direction with strain from 0% to 100%. W_{ch}/L_{ch} =250/100 μm. **b**, Mobility and maximum current (V_{gs} = -8 V, V_{ds} = -10 V) obtained under 50% strain and in the released states during 1,000 stretching cycles. Data from three transistors were averaged for each cycle.



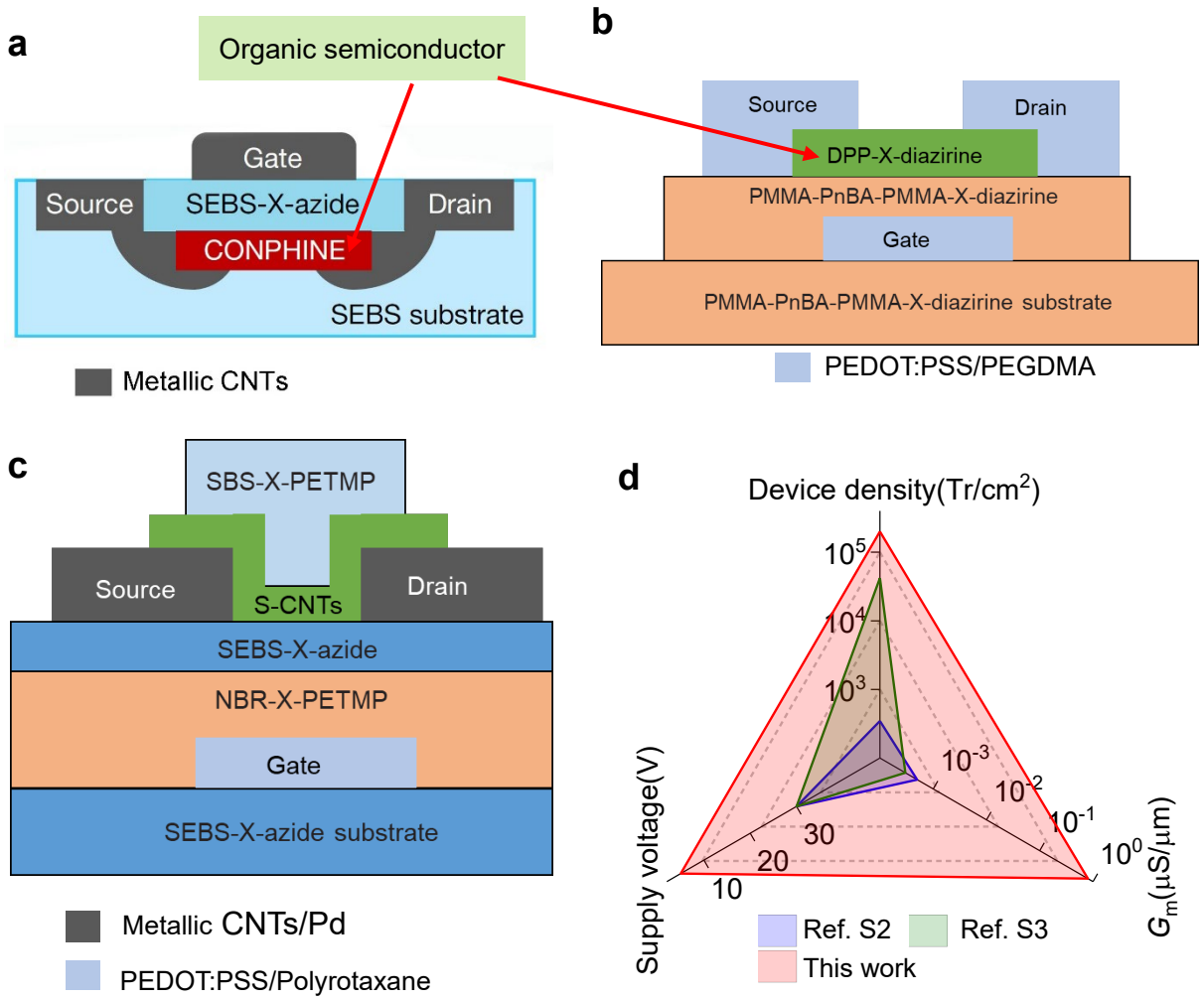
Supplementary Fig. 25. Characteristics of intrinsically stretchable transistors with biaxial strain and twist deformation. a, Photographs of transistor arrays under relax, bi-direction stretched (~30% on each axis) and twisted (180°). In total, there are 144 transistors in the green box. **b**, Transfer curves before deformation. **c**, Transfer curves after biaxial strain. **d**, Transfer curves after twist deformation. **e**, On-state current and gate leakage changes of intrinsically stretchable transistors after applying large strain. In total, 10 transistors with channel width of 250 μm and channel length of 50 μm were measured at V_{ds}=-3 V. Data from ten transistors were averaged for each condition.



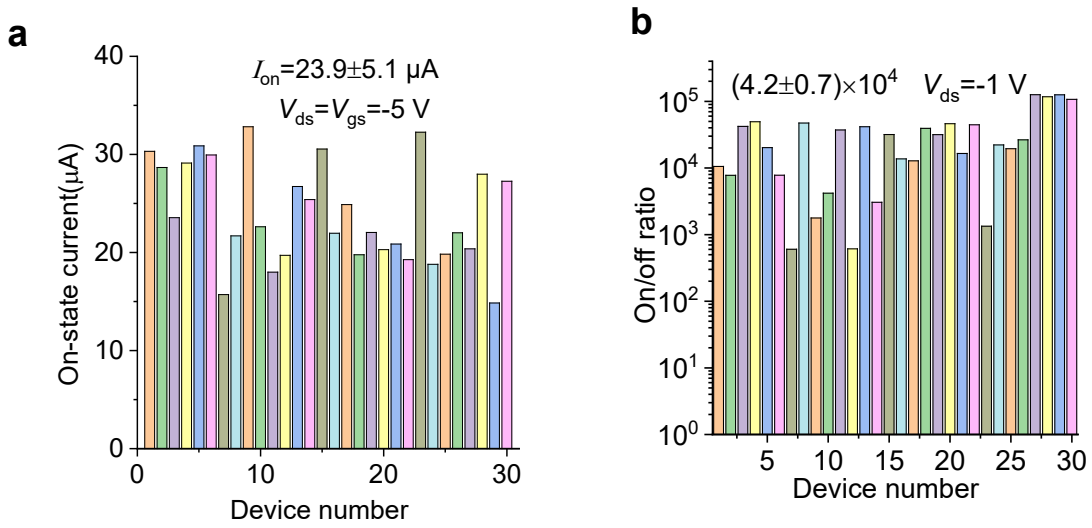
Supplementary Fig. 26. High-density intrinsically stretchable transistor array. a-c, Optical microscope images of a high-density transistor array (200,000 transistors/cm^2). **d**, Optical microscope image of a transistor connected with pads for measurement. The size of the core device area is the same as the device in the high-density transistor array.



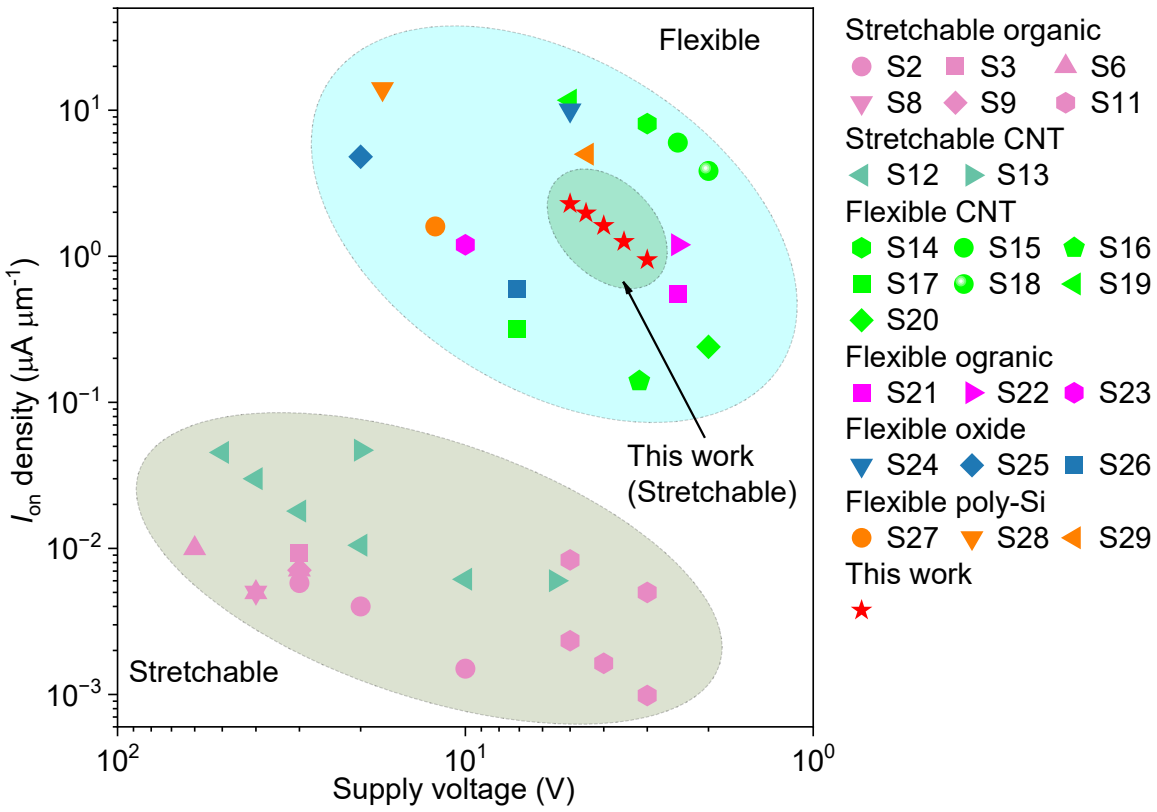
Supplementary Fig. 27. Transconductance extraction of a typical short-L_{ch} intrinsically stretchable transistor. Normalized transconductance is up to 0.8 μS/μm. W_{ch}/L_{ch} ~12/2 μm.



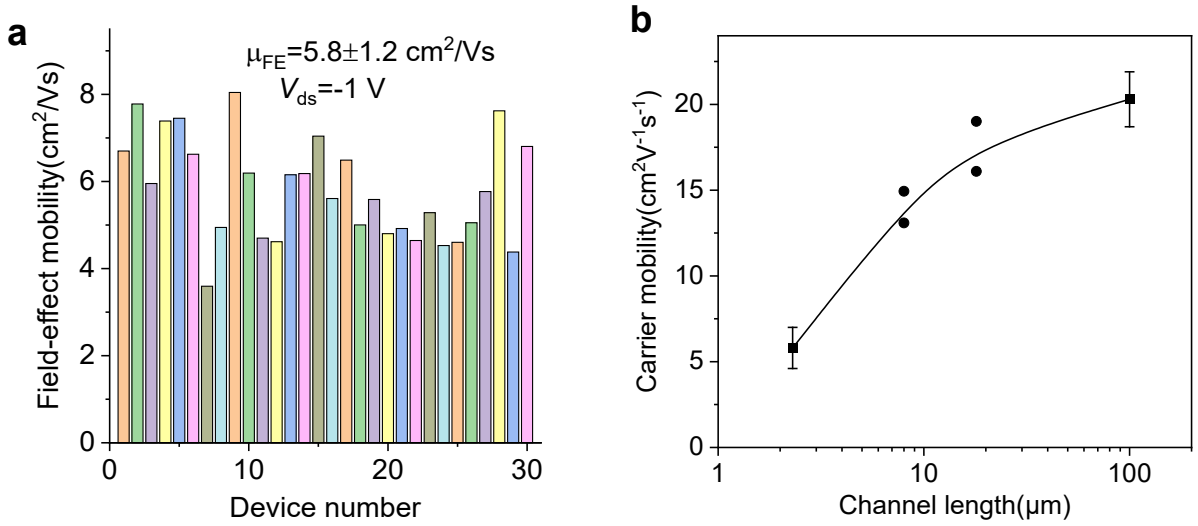
Supplementary Fig. 28. Schematic diagram and performance of device structures of three generations of intrinsically stretchable transistor arrays. a, Ref. S2: *Nature* **555**, 83–88 (2018). **b,** Ref. S3: *Science* **373**, 88–94 (2021). **c**, This work. **d,** Comparison of device density, supply voltage and on-state current with other reported intrinsically stretchable high-density transistor arrays.



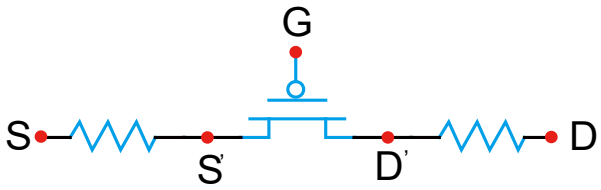
Supplementary Fig. 29. Transistor performance of a high-density transistor array with 200,000 transistors/cm^2. a, On-state currents. **b**, On/off ratios. On-state currents were measured at V_{gs}=V_{ds}=-5 V. On/off ratios and linear field-effect mobilities were measured at V_{ds}=-1 V. The channel width/length was ~12 μm/2 μm, and dielectric thickness was ~300 nm. In total, 30 transistors were measured.



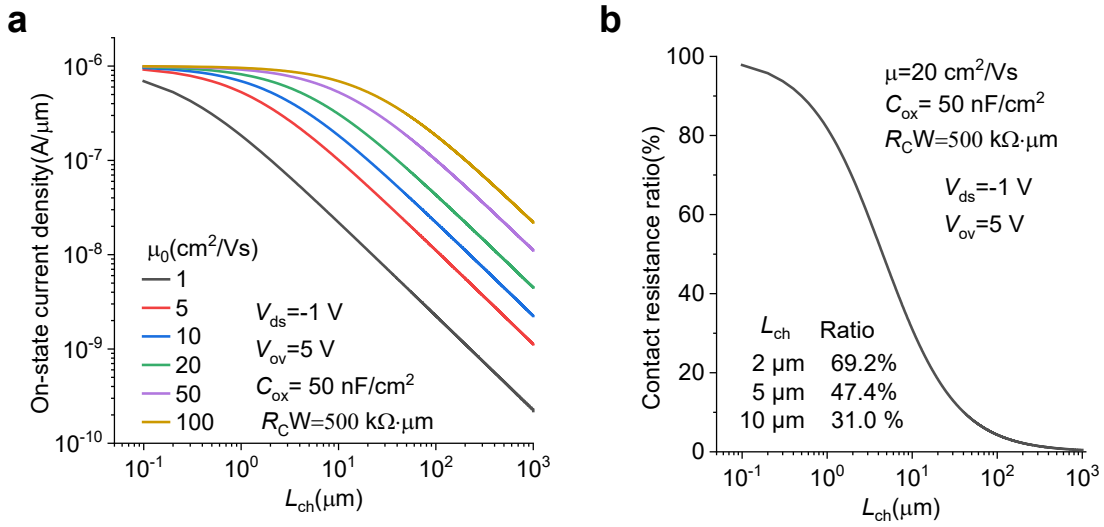
Supplementary Fig. 30. Performance comparison of our intrinsically stretchable transistors with previously reported state-of-the-art intrinsically stretchable transistors and flexible transistors reported in the past decade.



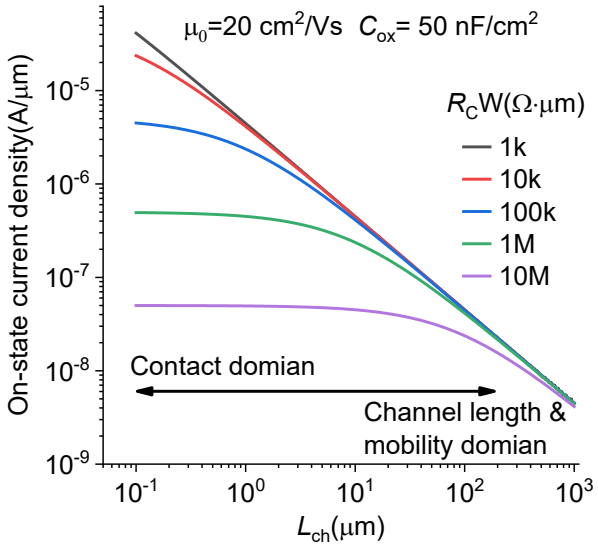
Supplementary Fig. 31. a, Linear field-effect mobilities of the high-density transistor array with 200,000 transistors/cm^2. **b**, Carrier mobility versus channel length for intrinsically stretchable transistors. Thirty transistors were averaged for 2 μm L_{ch}, two transistors were averaged for 8 μm L_{ch}, two transistors were averaged for 18 μm L_{ch}, and four transistors were averaged for 100 μm L_{ch}.



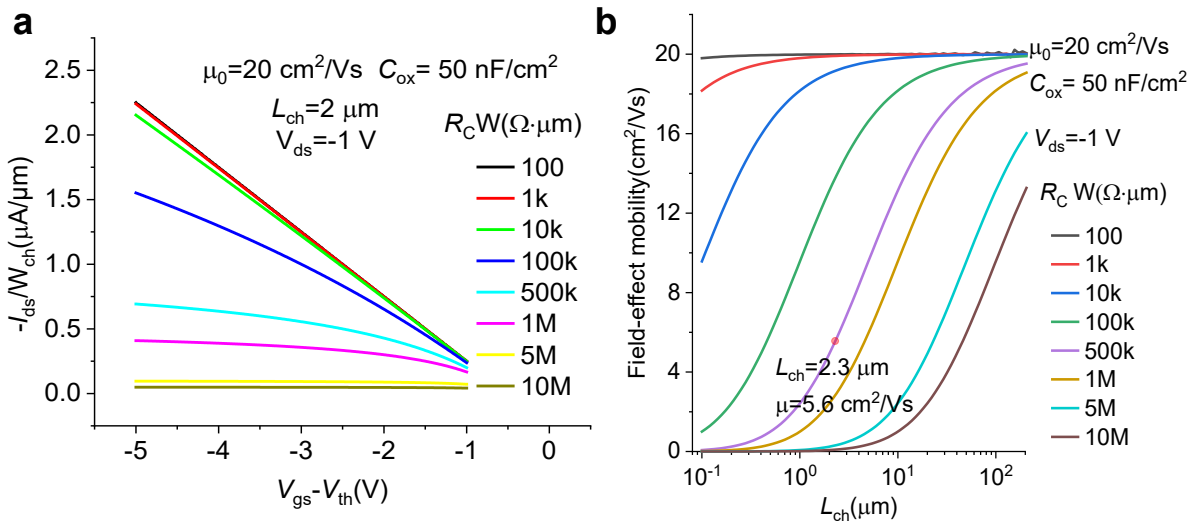
Supplementary Fig. 32. Circuit model of a transistor with contact resistance. G, S and D represent gate, source and drain electrodes, while S' and D' represent the real source and drain for the channel.



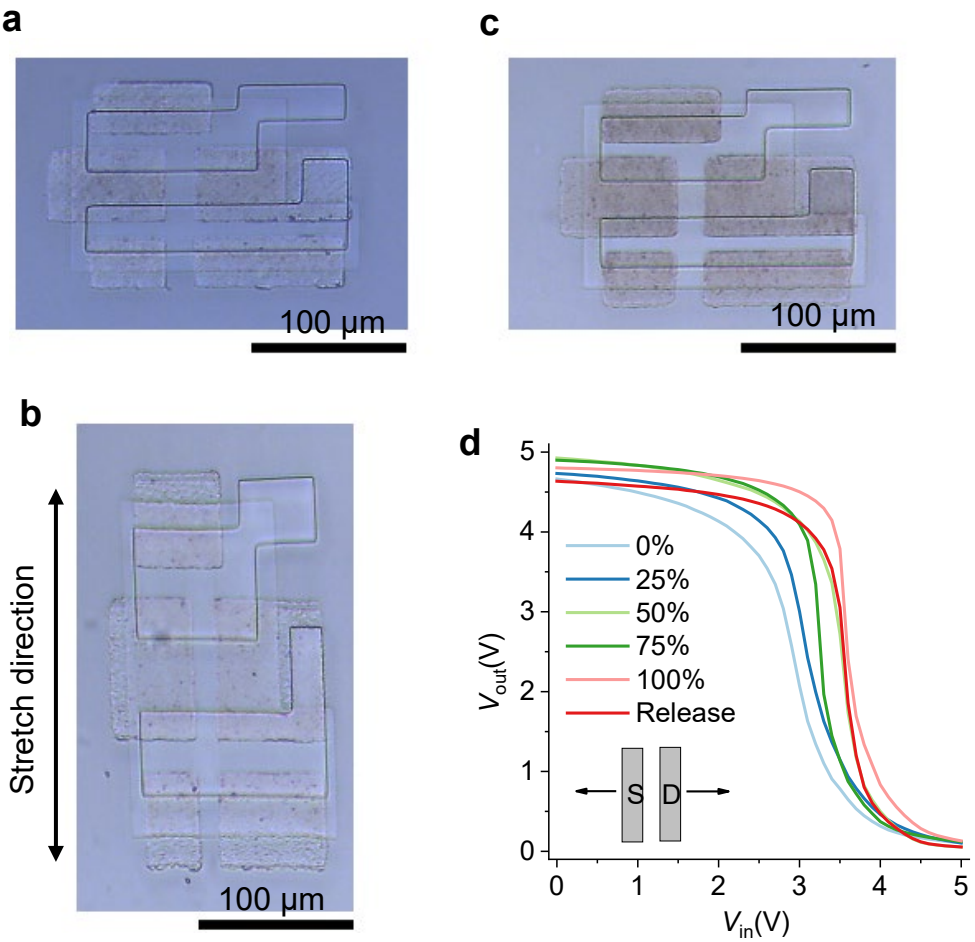
Supplementary Fig. 33. Influence of contact resistance for different channel lengths and carrier mobilities based on simulation. a, On-state current density versus channel length under different mobilities. Linear field-effect mobility μ_0=1-100 cm^2/V/s, C_{ox}=50 nF/cm^2, R_cW=500 kΩ·μm, V_{ds}=-1 V and overdrive voltage V_{ov}=5 V. Because of the large contact resistance ratio at short channel length, on-state current density cannot increase effectively even when the mobility is largely increased. **b**, Contact resistance ratio versus channel length. The contact resistance ratio is defined by the ratio of contact resistance over the total resistance of the transistors. Linear field-effect mobility μ_0=20 cm^2 V^{-1} s^{-1}, C_{ox}=50 nF/cm^2, R_cW=500 kΩ·μm, V_{ds}=-1 V and overdrive voltage V_{ov}=5 V. With the decrease of change length, the contact resistance over the total resistance ratio would increase.



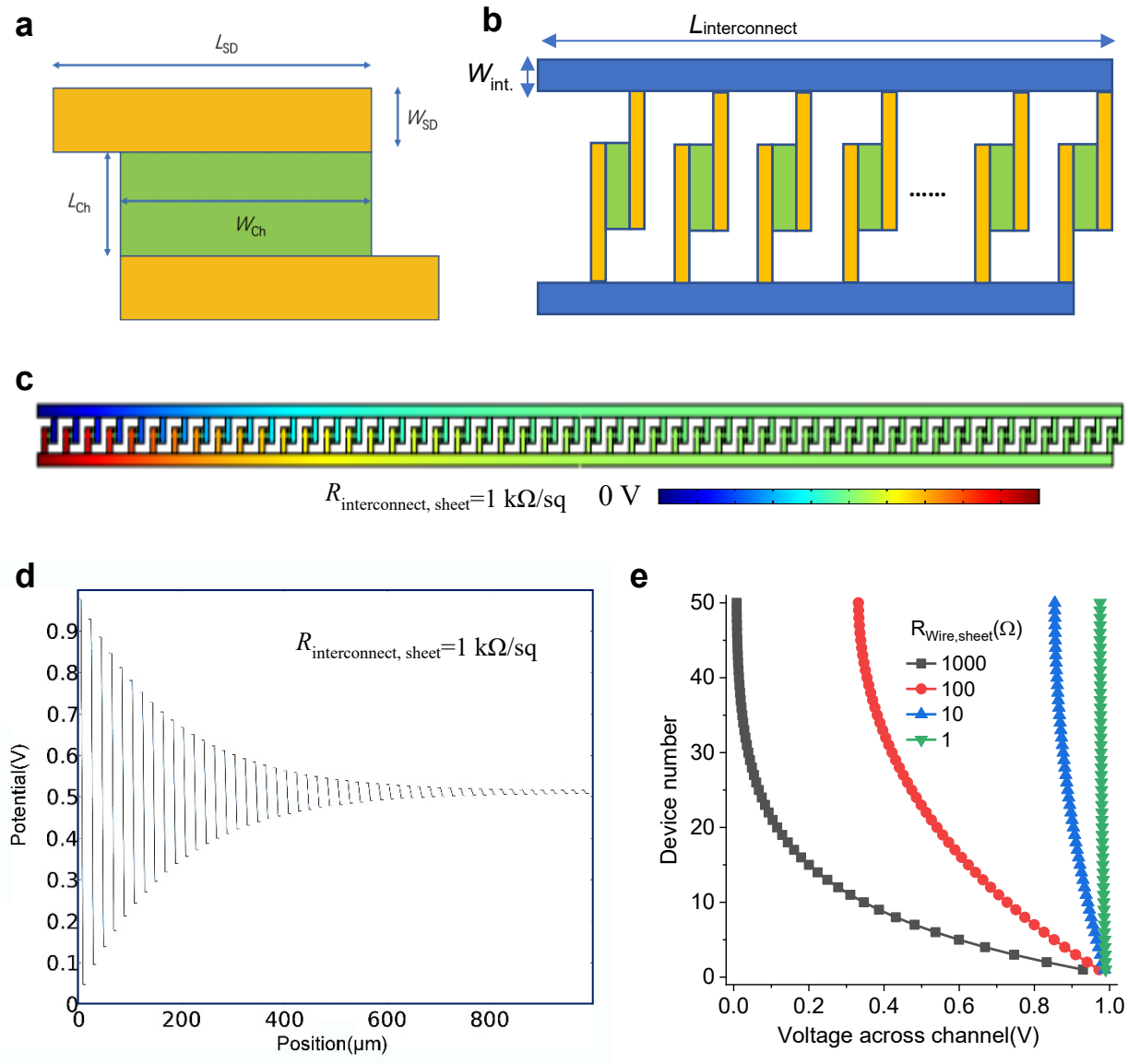
Supplementary Fig. 34. On-state current density versus channel length under different contact resistance based on simulation. Linear field-effect mobility μ_0=20 cm^2 V^{-1} s^{-1}, C_{ox}=50 nF/cm^2, V_{ds}=-1 V and overdrive voltage V_{ov}=5 V. At longer channel lengths, the on-state current density is dominated by the channel length and mobility. At shorter channel lengths, the on-state current density is dominated by the contact resistance. The transition point shifts to the left, when the contact resistance is decreased.



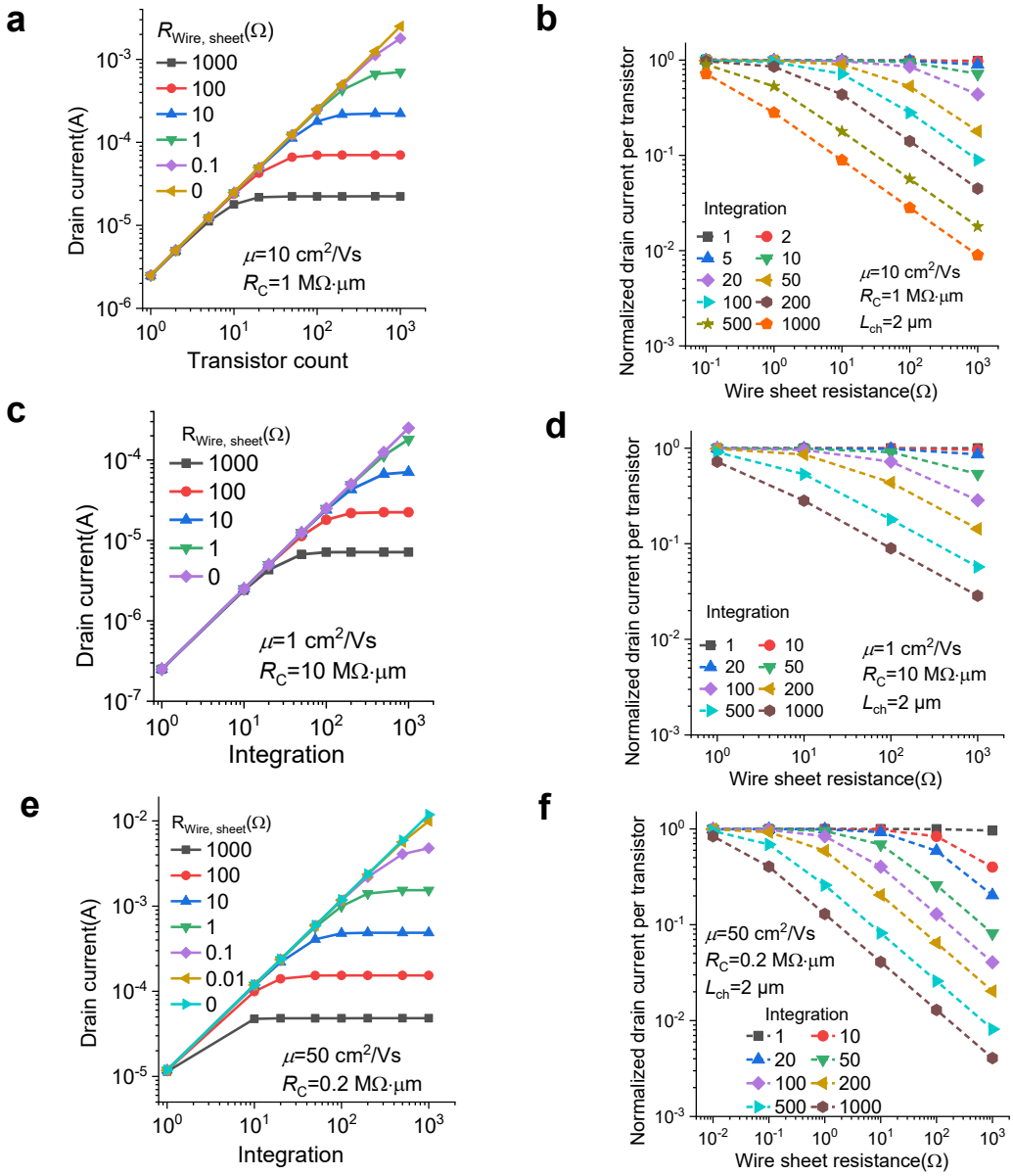
Supplementary Fig. 35. Calculation of field-effect mobility from I_d-V_{gs} curves in the linear region. a, Simulated I_d-V_{gs} curves under different contact resistance. L_{ch}=2 μm. **b**, Linear field-effect mobilities extracted from simulated transfer curves from -1 V to -5 V. When the contact resistance is at 500 kΩ·μm, field-effect mobility drops from 19.5 $cm^2\ V^{-1}\ s^{-1}$ at 100-μm L_{ch} to 5.6 $cm^2\ V^{-1}\ s^{-1}$ at L_{ch}=2.3 μm, which is close to the measured mobility for short-L_{ch} transistors. To further improve the short-L_{ch} transistor performance in the future (e.g., μ_{FE} larger than 10 $cm^2\ V^{-1}\ s^{-1}$ at the L_{ch} of 1 μm), the contact resistance needs to be further reduced by ~71% down to 100 kΩ μm.



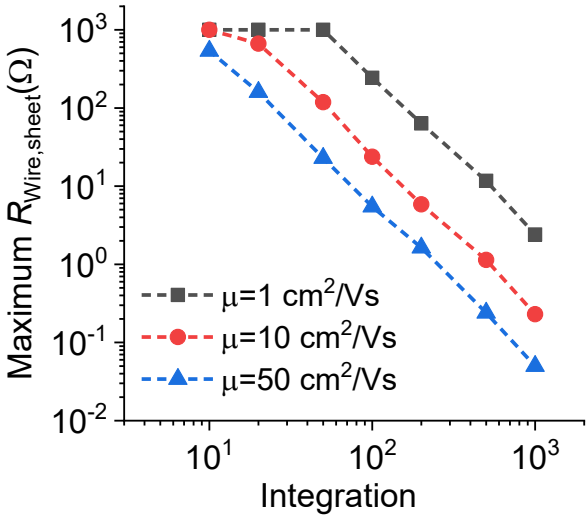
Supplementary Fig. 36. Characteristics of a small-size Pseudo-D inverter under different strains. a-c, Optical microscope images of a Pseudo-D inverter at (**a**) 0% strain, (**b**) 100% strain and (**c**) release from 100 % strain. **d**, Voltage transfer curves of the Pseudo-D inverter under different strains.



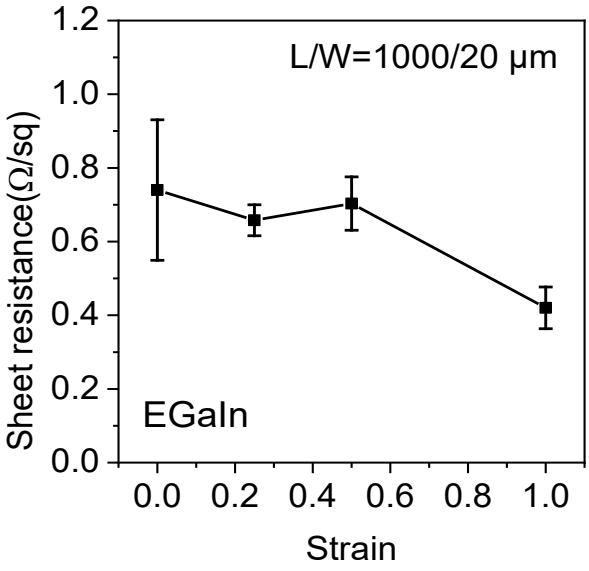
Supplementary Fig. 37. Modeling and simulation of the influence of interconnect resistance on integrated circuits with multiple transistors. a, Schematic diagram of transistor geometry with S/D electrodes. **b**, Schematic diagram of multiple transistors connected using long wires. **c**, Simulated potential distribution of the integrated circuits with 50 transistors. The sheet resistance of the channel is 1 MΩ/sq, the contact resistance is 1 MΩ·μm, and the sheet resistance of long wires is 1 kΩ/sq. **d**, Voltage drops across the transistors channel. The further the transistor is from the power source, the smaller the voltage drops across the transistor channels. **e**, Voltage drops across the transistors channel with different conductive wirings. The smaller the sheet resistance of the wiring, the larger the voltage drops across the channels.



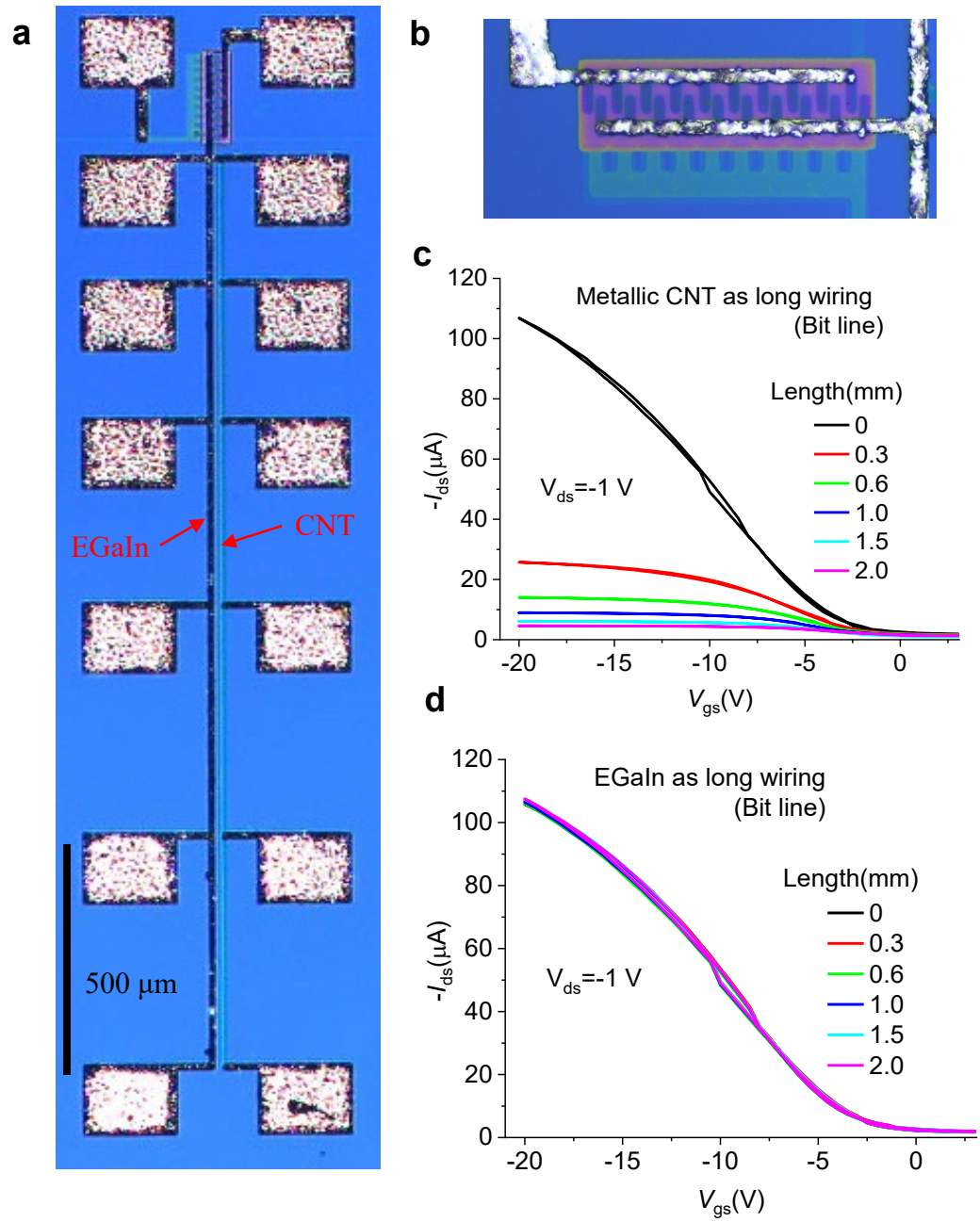
Supplementary Fig. 38. Relationship between normalized drain current and interconnect sheet resistance. Normalized drain current per transistor is defined by average drain current per transistor divided by average drain current per transistor when the transistor number is one. **a**, **b**, μ_0=10 cm^2 V^{-1} s^{-1}, R_cW= 1 MΩ·μm, L_{ch}= 2 μm. **c**, **d**, μ_0=1 cm^2 V^{-1} s^{-1}, R_cW= 10 MΩ·μm, L_{ch}= 2 μm. **e**, **f**, μ_0=50 cm^2 V^{-1} s^{-1}, R_cW= 0.2 MΩ·μm, L_{ch}= 2 μm.



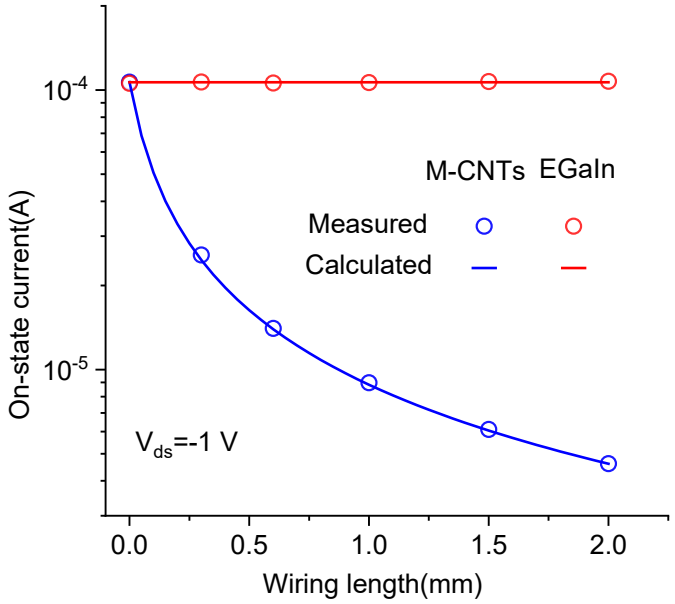
Supplementary Fig. 39. Relationship between circuit integration scale and interconnect sheet resistance. A larger number of the transistors requires a smaller sheet resistance to maintain normalized drain current. Based on the simulation results, we can calculate the minimal sheet resistance requirement for different integration scales. Here, we set the normalized drain current per transistor to 50%.



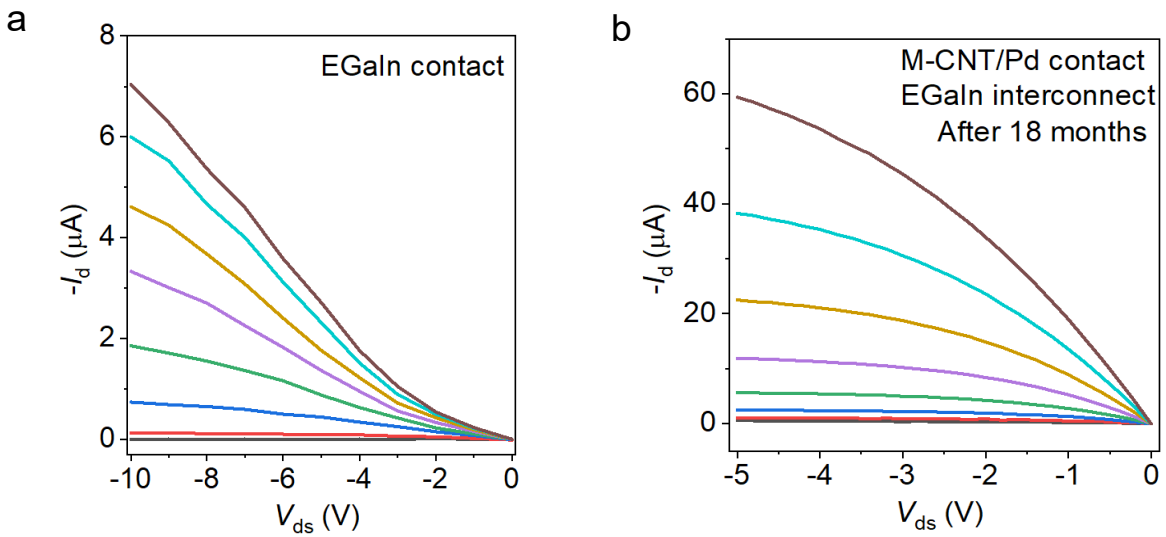
Supplementary Fig. 40. Sheet resistance of EGaIn under different strains from 0% to 100%. The sheet resistance can well maintain under 1 Ω/sq. Three EGaIn electrodes were measured for each strain.



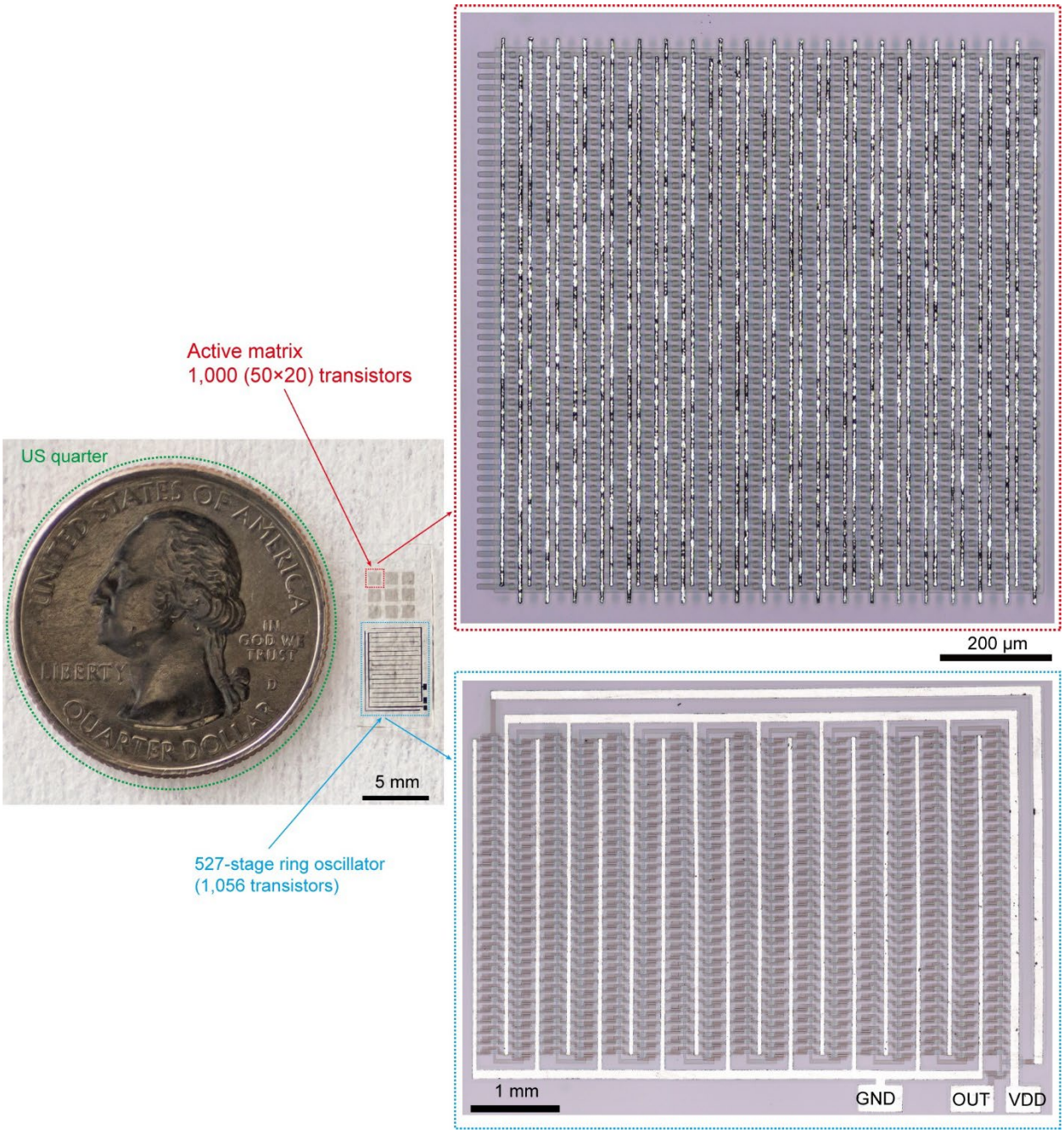
Supplementary Fig. 41. Comparison of M-CNTs and EGaIn as long interconnect. a, Optical microscope images of intrinsically stretchable transistors with long M-CNTs or EGaIn interconnects. Multiple pads are designed to measure drain currents with different interconnect lengths. **b**, Zoomed-in optical microscope image of the transistors. **c-d**, Transfer curves were measured with different lengths using (**c**) M-CNTs (8 μm width and ~100 nm thickness) and (**d**) EGaIn (8 μm width and 1.5 μm thickness). When the interconnect length was increased, a significant decrease in drain current was observed for M-CNTs, while the drain current remained constant for EGaIn.



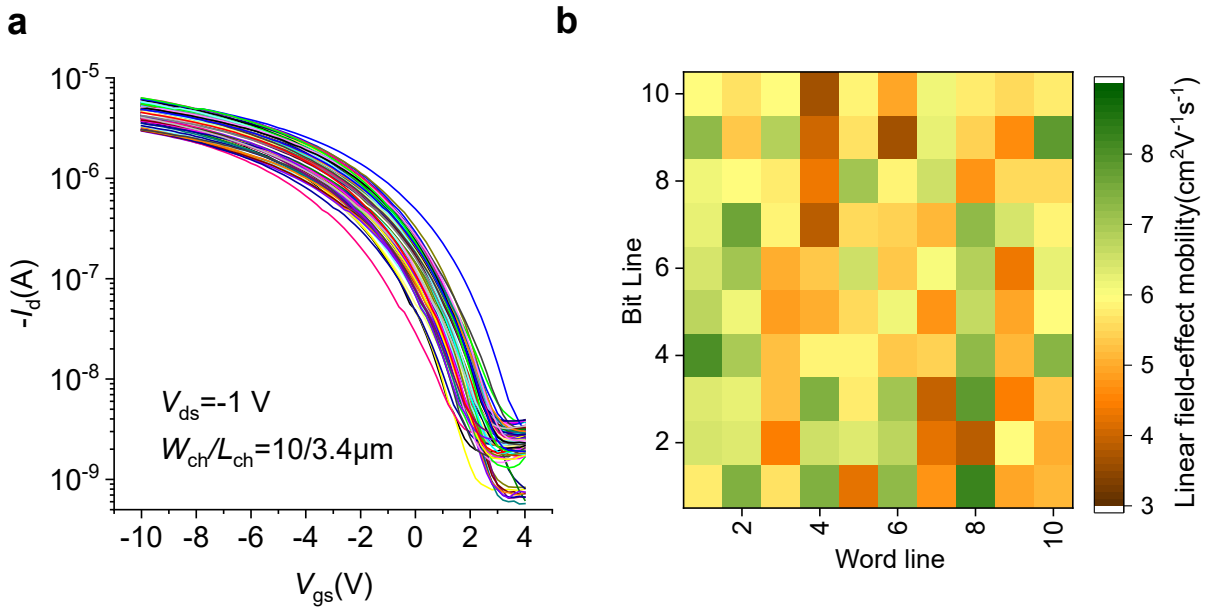
Supplementary Fig. 42. Comparison of measurement and simulation of stretchable transistors with long interconnect. The simulated drain current agrees well with the measured results. The sheet resistances of M-CNTs and EGaIn were 727.2 Ω/sq and 0.21 Ω/sq, respectively.



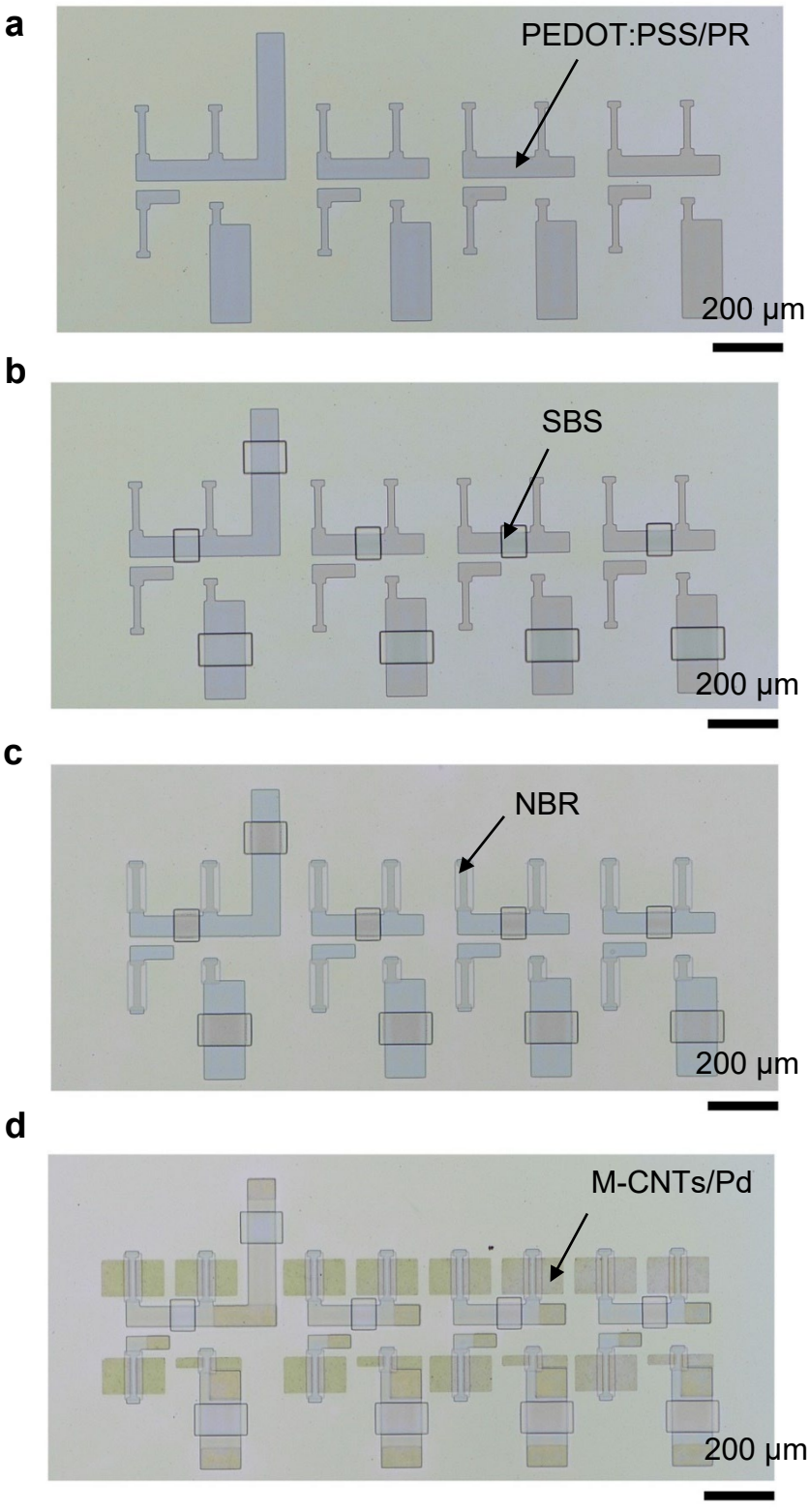
Supplementary Fig. 43. a, Output curves of a CNT transistor with EGaIn contact. b, Output curves of a CNT transistor with EGaIn interconnect and M-CNT/Pd contact after over 18 months from device fabrication.

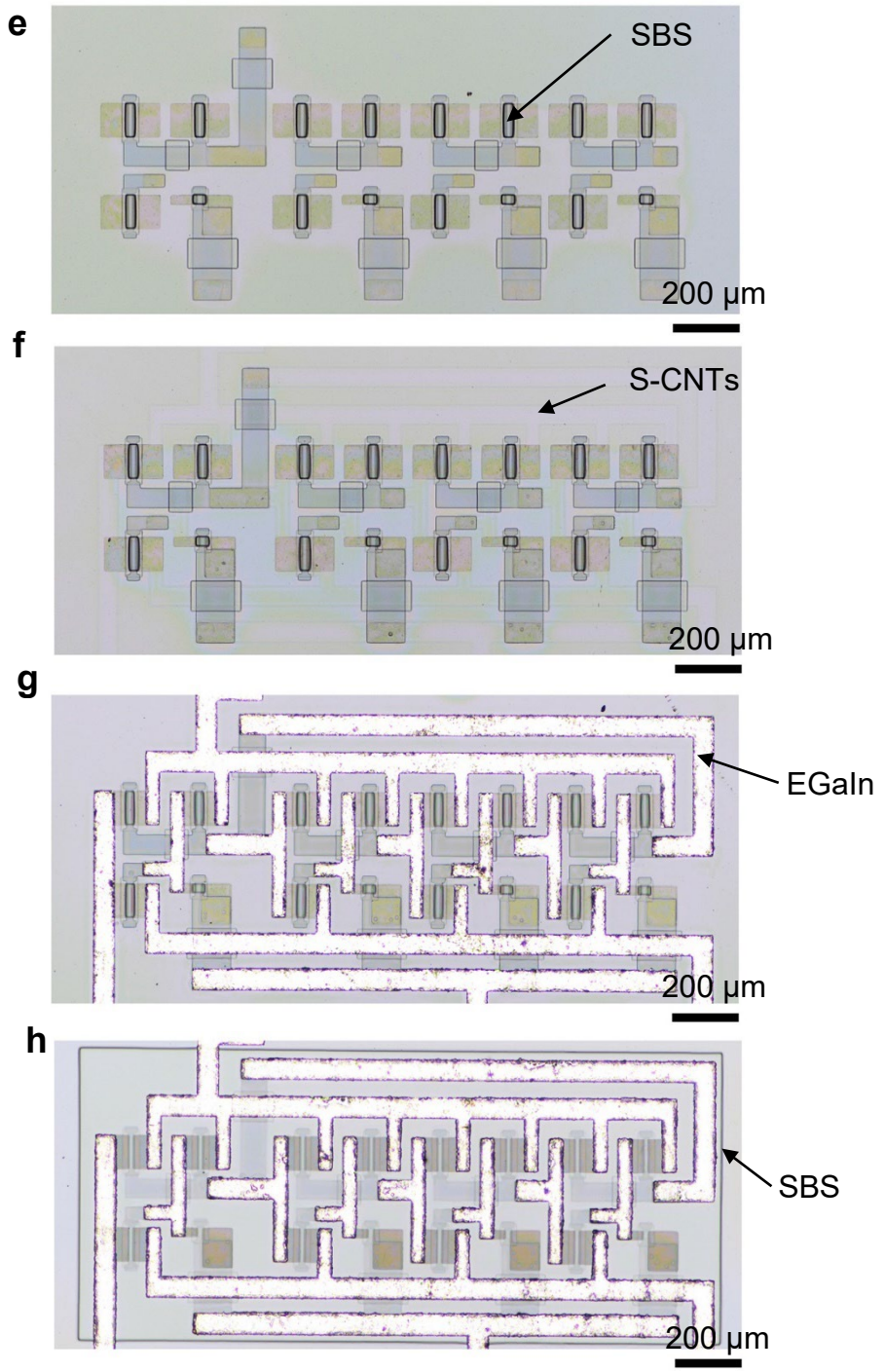


Supplementary Fig. 44. Size comparison between the 527-stage ring oscillator, active-matrix transistor array and a US quarter. For the active matrix, the dimension of a single cell including one transistor and three accessing interconnect lines is 20 μm in height and 50 μm in width, so the overall device density is 100, 000 transistor per cm^2. EGaIn was used for bit lines and ground lines, and PEDOT:PSS/PR was used for word lines, respectively.

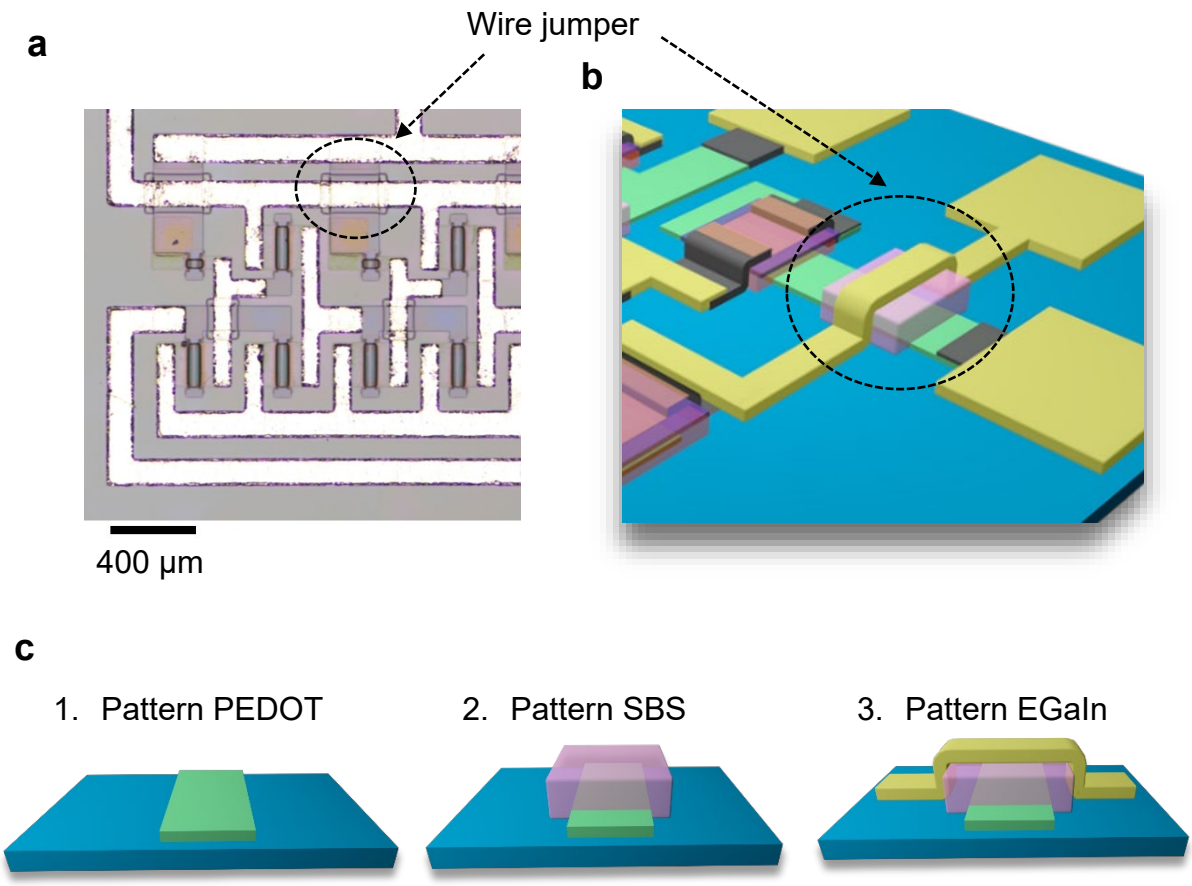


Supplementary Fig. 45. Characteristics of the transistor matrix with EGaIn interconnects. a, Schematic diagram (**a**) and photo (**b**) of the bonding method for the transistor matrix with a flat flexible cable (FFC), which was used to be connected to Keithley 4200 and the power source. **c**, Optical microscope image of an intrinsically stretchable high-density transistor matrix. The cell area is 50×20 μm^2, and the device density is 100,000 transistors/cm^2. **d**, Transfer curves of transistors from a 10×10 transistor matrix. **e**, Mapping of linear field-effect mobilities. V_{ds}=-1.0 V, V_{gs} is from -5 V to -10 V.

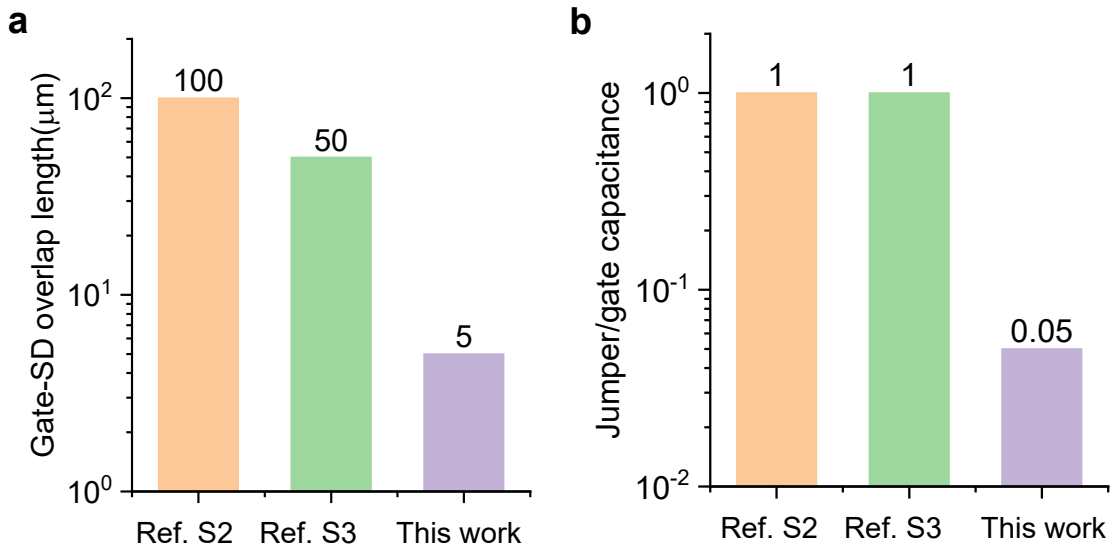

a
PEDOT:PSS/PR
200 μm
b
SBS
200 μm
c
NBR
200 μm
d
M-CNTs/Pd
200 μm



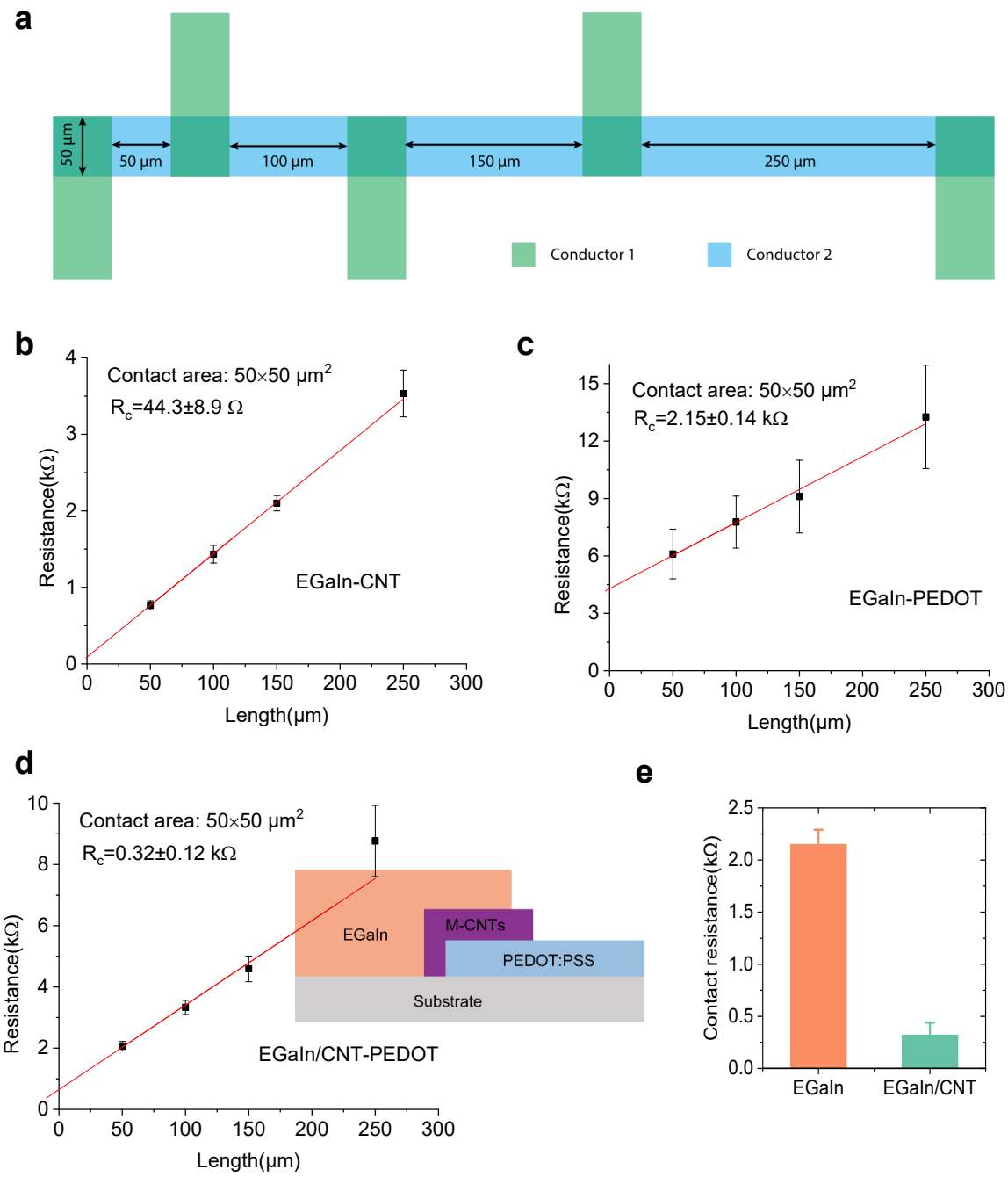
Supplementary Fig. 46. Optical microscope images of the fabrication process of high-speed integrated circuits. a, Pattern PEDOT:PSS/PR as gate electrodes and bottom electrodes of wire jumpers. **b**, Pattern low-κ dielectric SBS as the dielectric of wire jumpers. **c**, Pattern high-κ gate dielectric NBR. **d**, Pattern M-CNTs/Pd as source/drain electrodes. **e**, Pattern low-κ dielectric SBS as channel encapsulation. **f**, Etch unwanted S-CNTs. **g**, Pattern EGaIn as top electrodes and long wires. **h**, Pattern low-κ dielectric SBS as circuit encapsulation.



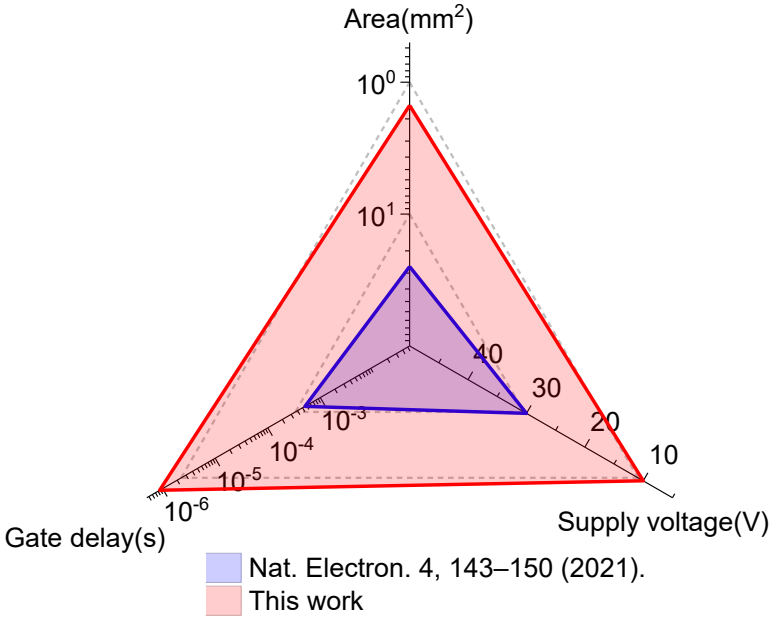
Supplementary Fig. 47. Fabrication process of wire jumpers. a, Optical microscope image of a wire jumper. **b**, Schematic diagram of a Pseudo-E inverter with a wire jumper. **c**, Schematic process of the wire jumper, 1.5 μm thick low-κ elastomer SBS was used as the jumper dielectric to reduce the parasitic wiring capacitance.



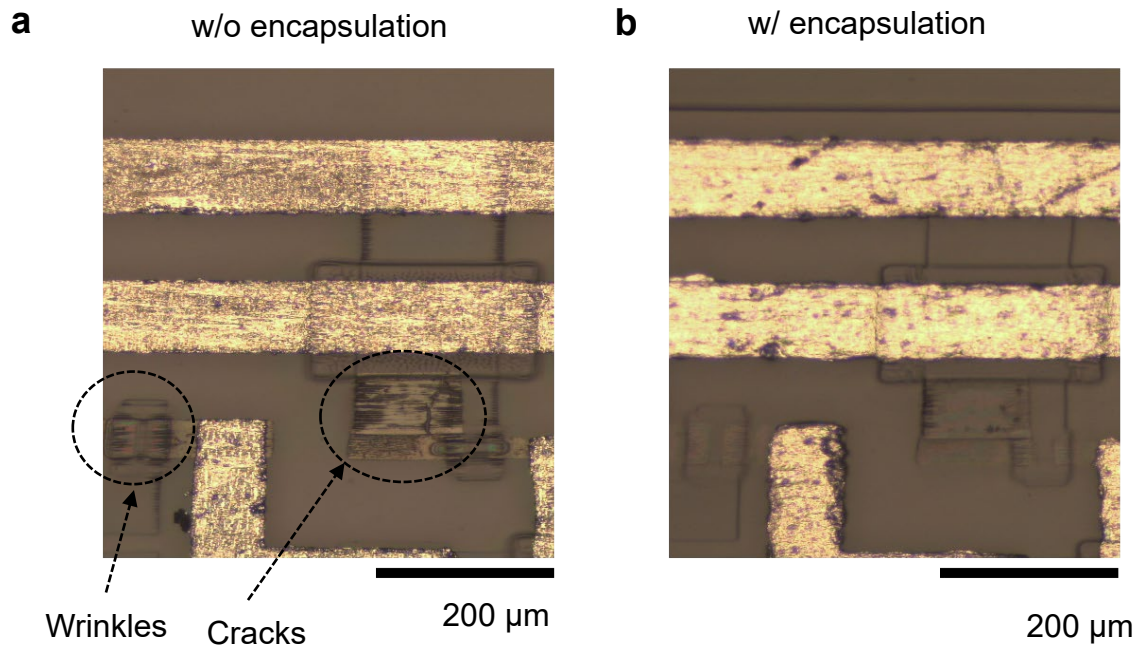
Supplementary Fig. 48. Reduced parasitic capacitance is required for improved operation speed of intrinsically stretchable circuits. a, With the optimal circuit layout to reduce overlap size as well as the improved fabrication process for smaller patterning size and better alignment, our latest intrinsic stretchable electronics show one order of magnitude reduction of Gate-SD overlap length compared to previous reports. **b**, Jumper/gate capacitance comparison with other intrinsically stretchable electronics. Jumper/gate capacitance is defined by the ratio of jumper capacitance per unit over gate capacitance per unit. Larger gate capacitance is preferred for the reduction of the operation voltage, while smaller jumper capacitance should be used to reduce additional charging/discharging time to improve the operation speed of integrated circuits. For all reported intrinsically stretchable technologies, jumper dielectric layers are fabricated with the gate dielectric layer. The jumper/gate capacitance ratio is 1, such that it could not be optimized together. To solve this issue, we used ~300 nm NBR/SEBS with high capacitance as the gate dielectric and 1.5 μm thick low-κ elastomer SBS with small capacitance as the jumper dielectric. In our case, the jumper/gate capacitance ratio is only ~0.05. S2: Wang, S. *et al.* Skin electronics from scalable fabrication of an intrinsically stretchable transistor array. *Nature* **555**, 83–88 (2018). S3: Zheng, Y. *et al.* Monolithic optical microlithography of high-density elastic circuits. *Science* **373**, 88–94 (2021).



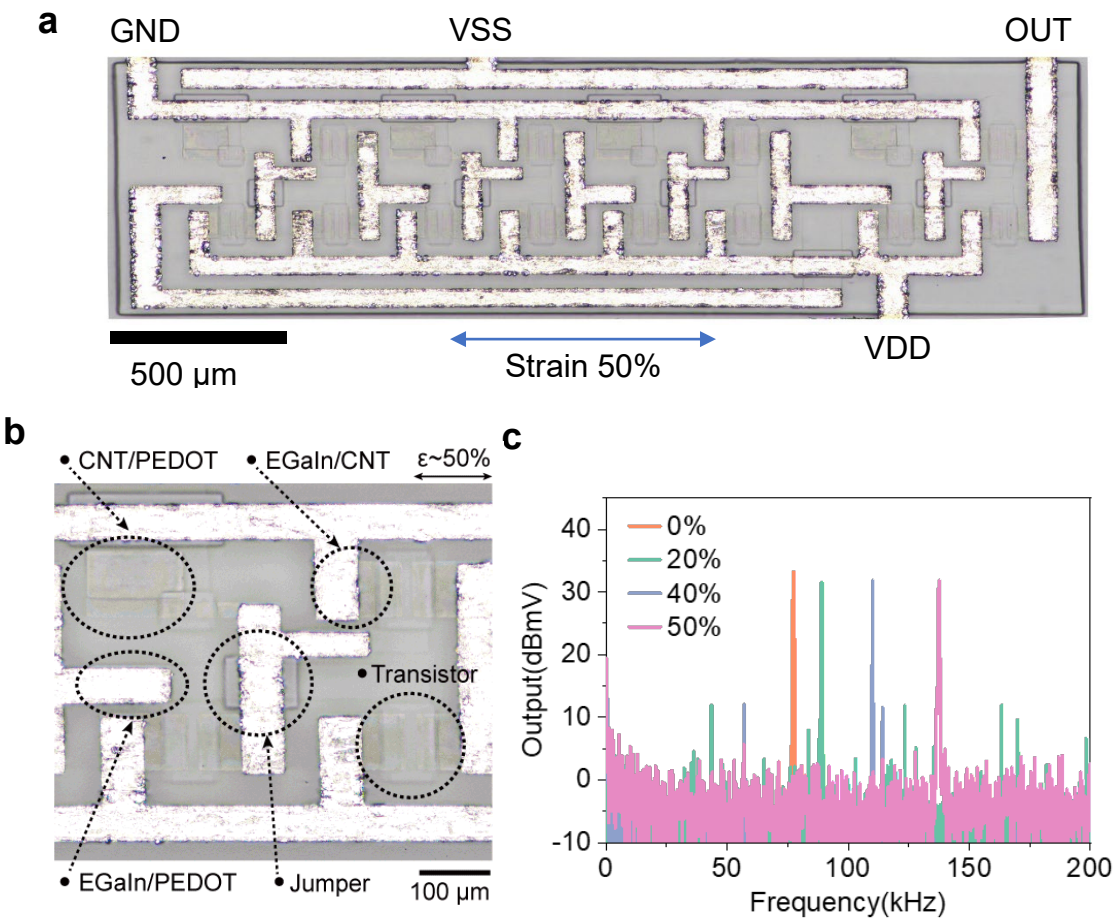
Supplementary Fig. 49. Contact resistance between different conductors. a, Schematic diagram showing contact resistance measurement. **b**, EGaIn and M-CNTs/Pd: 44.3±8.9 Ω. **c**, EGaIn and PEDOT:PSS/PR: 2.15±0.14 kΩ. **d**, EGaIn/M-CNTs/Pd and PEDOT:PSS/PR: 0.32±0.12 kΩ. All contact areas are 50×50 μm^2. **e**, Contact resistance comparison of EGaIn with PEDOT:PSS/PR w/ or w/o M-CNTs/Pd as the interface layer. With M-CNTs/Pd as the interface layer, the contact resistance can be reduced by about 85%. Three devices were measured for each condition.



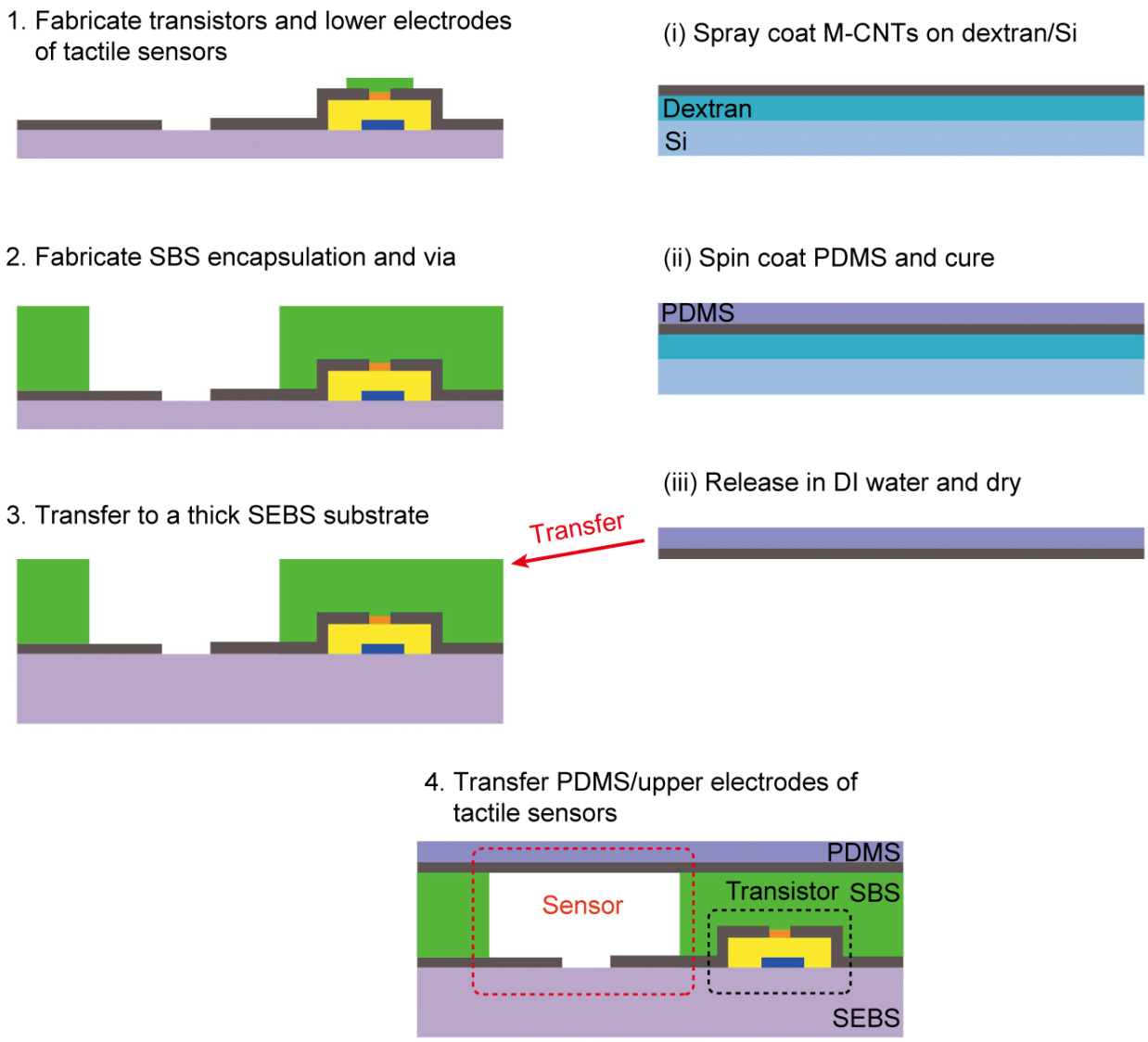
Supplementary Fig. 50. Comparison of our work with state-of-art intrinsic all stretchable 3-stage ring oscillator. We reduced the circuit area from 25 mm^2 to 1.5 mm^2, reduced the supply voltage from 30 V to 10 V, and reduced the gate delay from 0.51 ms to 0.88 μs.



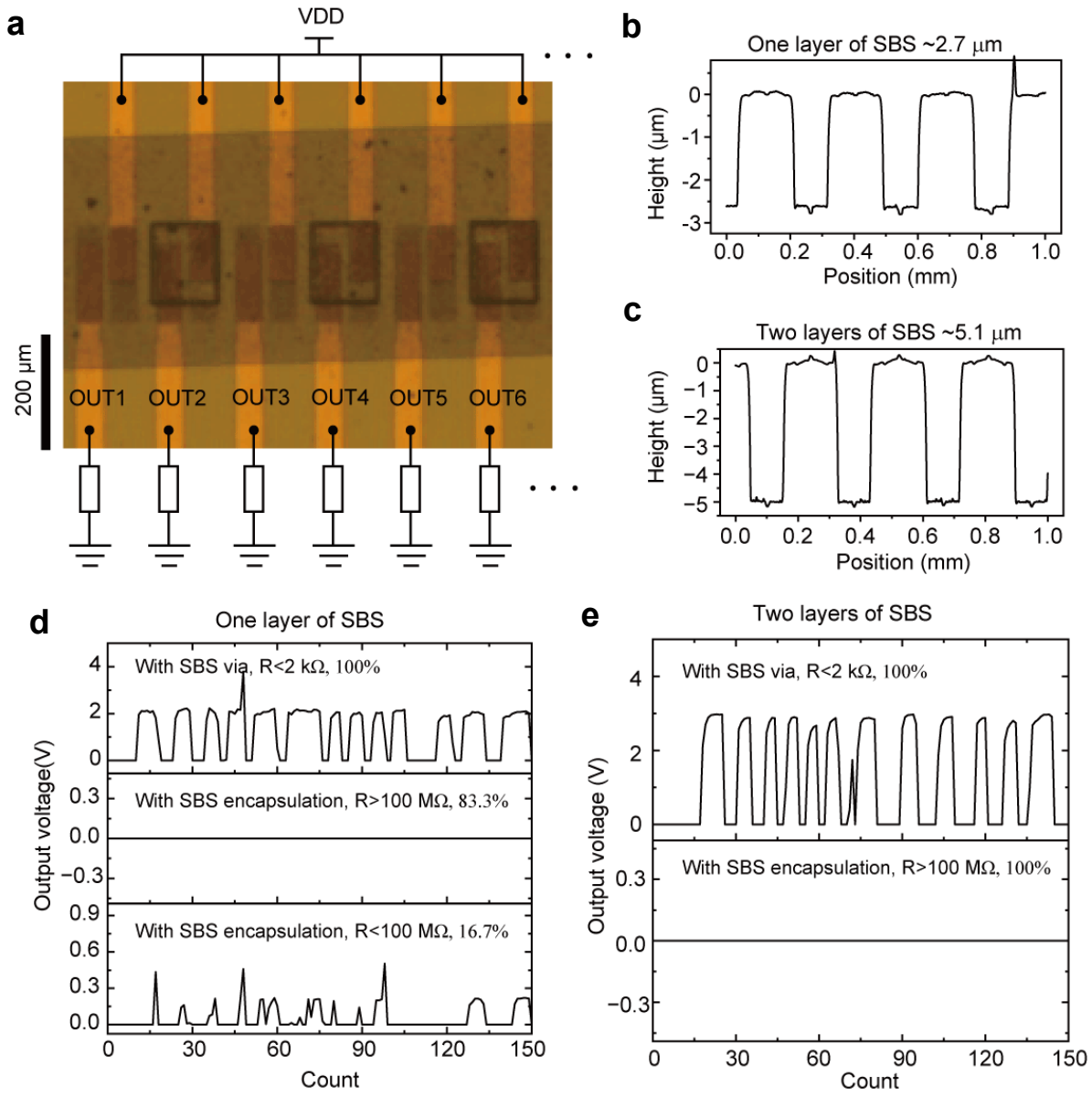
Supplementary Fig. 51. Reduce local maximum strain by encapsulation. a-b, OM images of integrated circuits under strain w/o encapsulation (**a**) and w/o encapsulation (**b**).



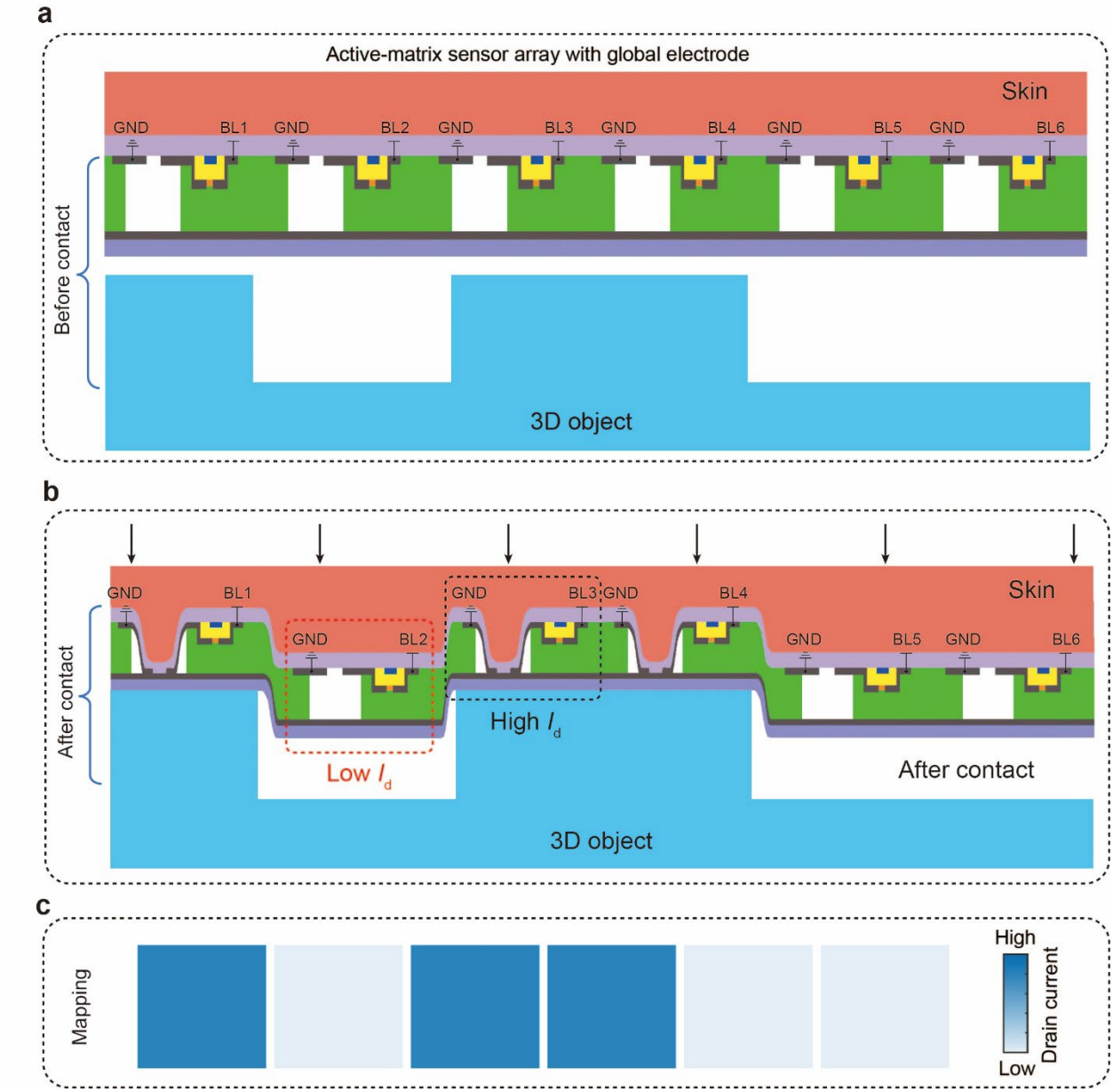
Supplementary Fig. 52. Measurement of 3-stage ring oscillator under strain. a, OM image of a 3-stage ring oscillator under 50% strain. **b**, Zoom-in OM image of a 3-stage ring oscillator under 50% strain. **c**, Measured output spectrum of the ring oscillator under different strains.



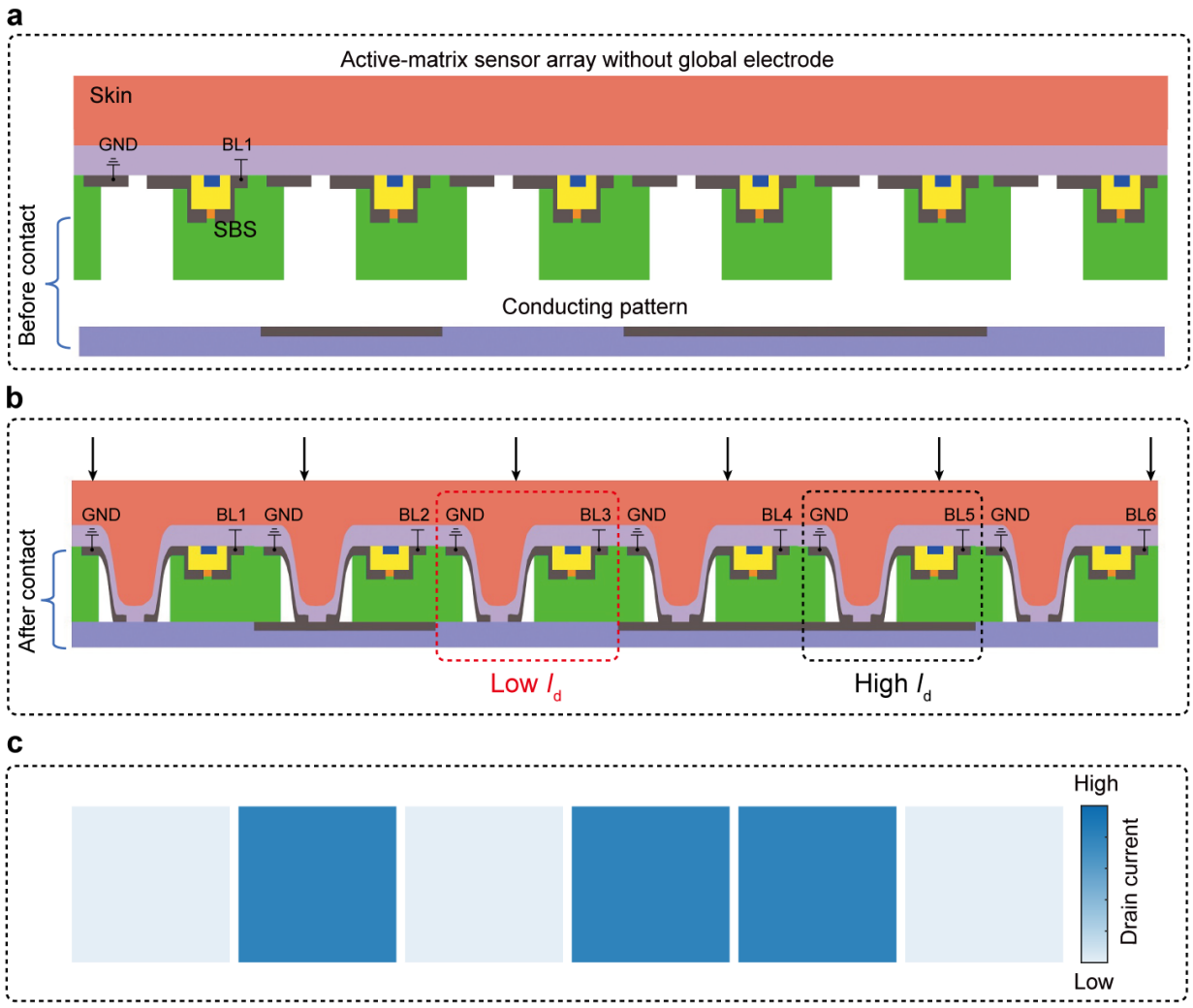
Supplementary Fig. 53. Fabrication process of intrinsically stretchable high-density active-matrix tactile sensor array.



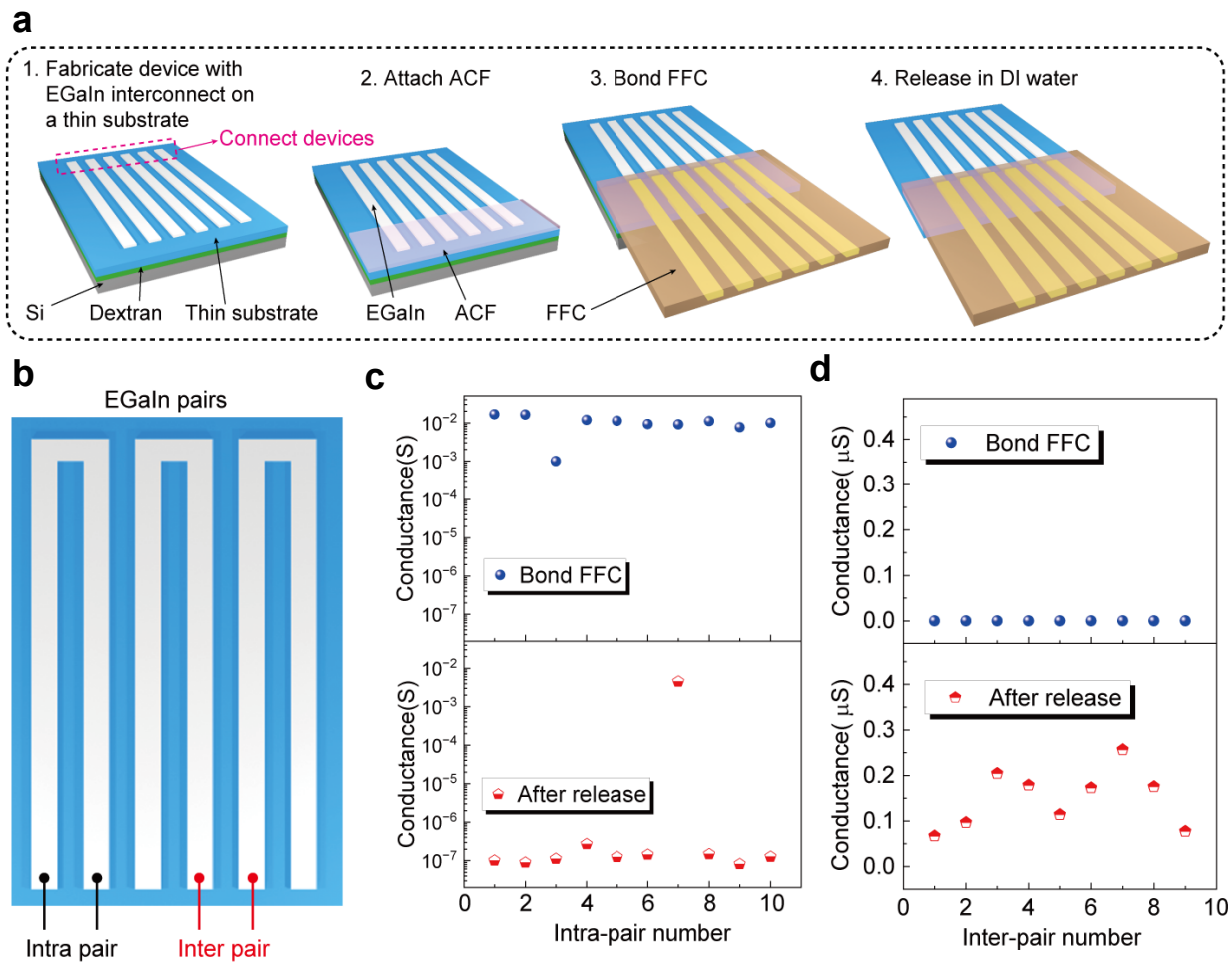
Supplementary Fig. 54. Optimization of tactile sensor via depth optimization for minimizing the leakage between transistors and sensor electrodes made by metallic CNTs. a, OM image and schematic diagram of the tactile sensor array. Those electrode pairs with SBS vias are tactile sensors, while those without SBS vias can be regarded as source/drain electrodes of transistors. Resistances of electrode pairs were measured by voltage dividers. Smaller output voltage means higher resistance. **b-c**, Depths of vias with one layer (**b**) and two layers (**c**) of SBS. **d-e**, Representative output voltages of different depths of vias with one layer (**b**) and two layers (**c**) of SBS under repeated pressing test. For SBS via with a depth of ~2.7 μm, ~16.7% showed a leakage between top and bottom metallic CNT electrodes caused by pressing, while using SBS with ~5.1 μm, the leakage is negligible.



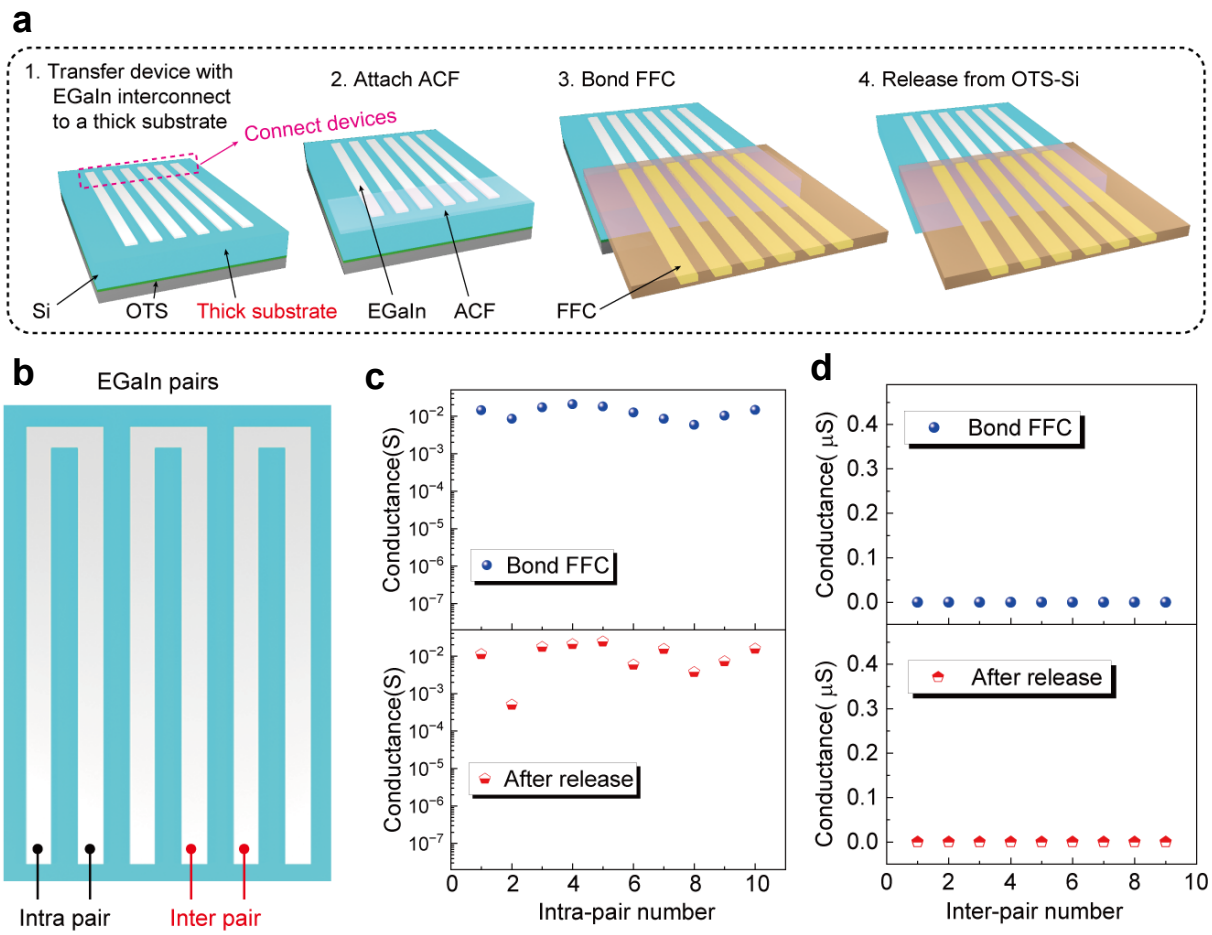
Supplementary Fig. 55. Working principle of the active-matrix tactile sensor array for sensing 3D object. a, Before contacting for active-matrix sensor array and 3D object. **b**, After contacting for active-matrix sensor array and 3D object. For the pixel on the raised part of the object, pressing operation will cause the top electrodes of tactile sensors to contact with the bottom electrodes to reduce the series resistance, so the pixel can show high drain current, while for the pixel on the recessed part, top electrodes do not contact the bottom electrodes, so the pixel will show low drain current. **c**, Schematic diagram of drain current distribution corresponding to **a**-**b**.



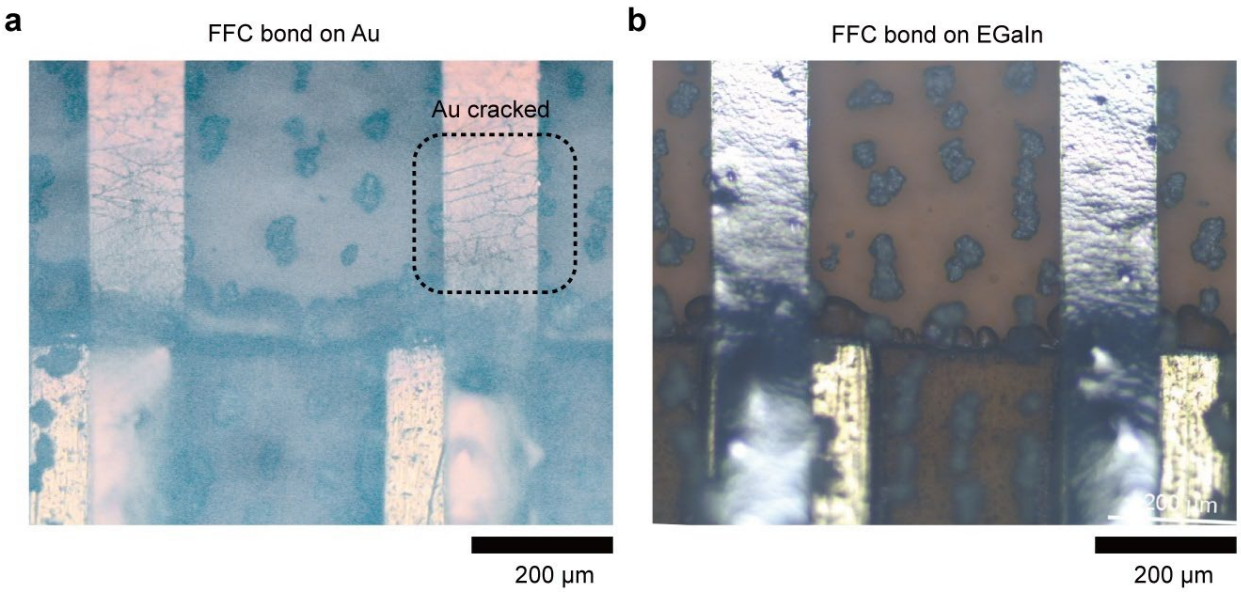
Supplementary Fig. 56. Working principle of active-matrix tactile sensor array for sensing 2D conducting pattern. a, Before making contact between the active-matrix sensor array and the 2D conducting pattern. **b**, After making contact between the active-matrix sensor array and the 2D conducting pattern. Pressing operation will cause all top electrodes to contact with the 2D object, but only the pixels with the bottom conductor can reduce the series resistance to induce high drain current. **c**, Schematic diagram of drain current distribution corresponding to **a**-**b**.



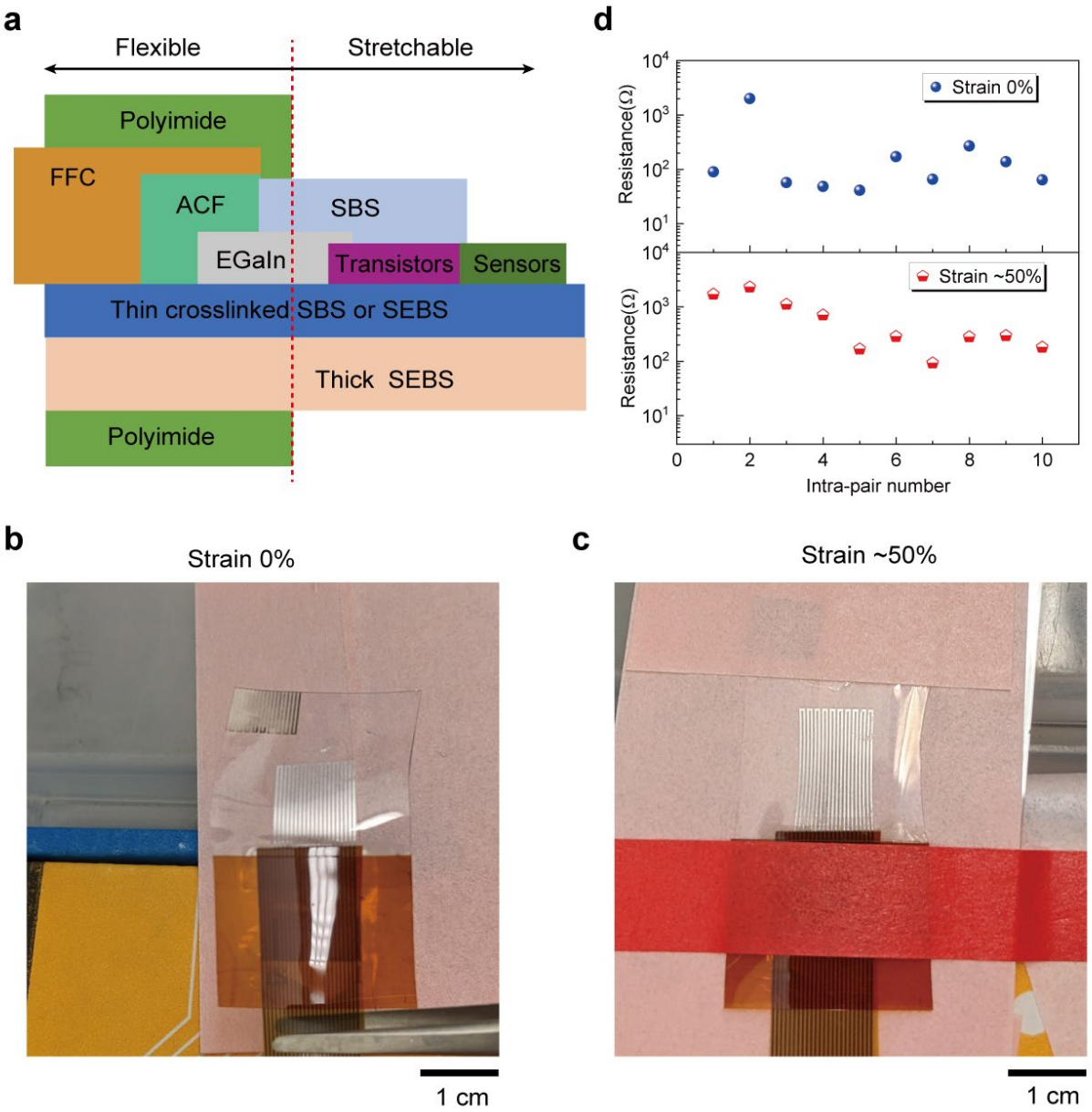
Supplementary Fig. 57. Bonding flat flexible cable to EGaIn interconnect on a thin stretchable substrate. a, Schematic diagram of the bonding process. ACF: anisotropic conducting film from Adafruit. FFC: flat flexible cable. The thickness of the thin stretchable substrate is ~ 2 μm. The width of the EGaIn electrode is 150 μm. **b**, Schematic diagram of how to characterize bonding of FFC and EGaIn. Ideally, the intra pair will show a short circuit, while the inter pair will show an open circuit. **c**, Measured conductance of intra pairs after bonding and releasing from the Si substrate via the dextran sacrificial layer. **d**, Measured conductance of inter pairs after bonding and releasing from dextran. Conductance measurement was performed using a multimeter, and the 0 μS means the measured resistance showed an open circuit. After releasing, the conductance of intra pairs decreased by 5 orders of magnitude, and the conductance of inter pairs also increased from 0 to above 0.1 μS. Since there is a large probability of the degradation of bonding after releasing, the direct bonding with FFC is not suitable for the thin stretchable substrate.



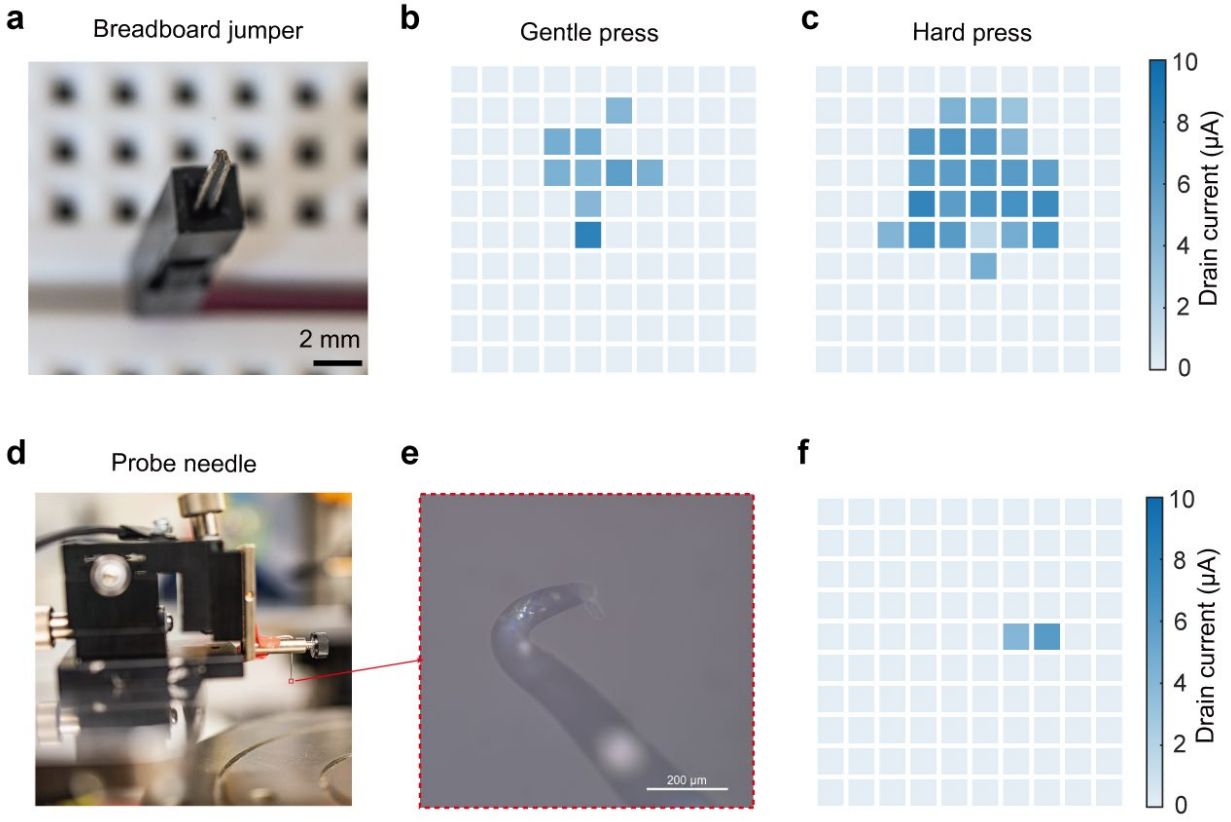
Supplementary Fig. 58. Bonding flat flexible cable to EGaIn interconnect on a thick stretchable substrate. a, Schematic diagram of the bonding process. ACF: anisotropic conducting film. FFC: flat flexible cable. OTS: Octadecyl trichlorosilane. Before bonding, the thin stretchable electronics is transferred onto a thick stretchable substrate, e.g., SEBS with a thickness of ~ 100 μm. **b**, Schematic diagram of how to characterize bonding of FFC and EGaIn. Ideally, the intra pair will show a short circuit, while the inter pair will show an open circuit. **c**, Measured conductance of intra pairs after bonding and releasing from OTS-Si. **d**, Measured conductance of inter pairs after bonding and releasing from OTS-Si. Conductance measurement was performed using a multimeter, and the 0 μS means the measured resistance showed an open circuit. After releasing, the conductance of intra pairs almost maintained at a high value, and the conductance of inter pairs also maintained at a low value. The good consistency of conductance before and after the release makes this approach suitable for the demonstration requiring lots of interconnects.



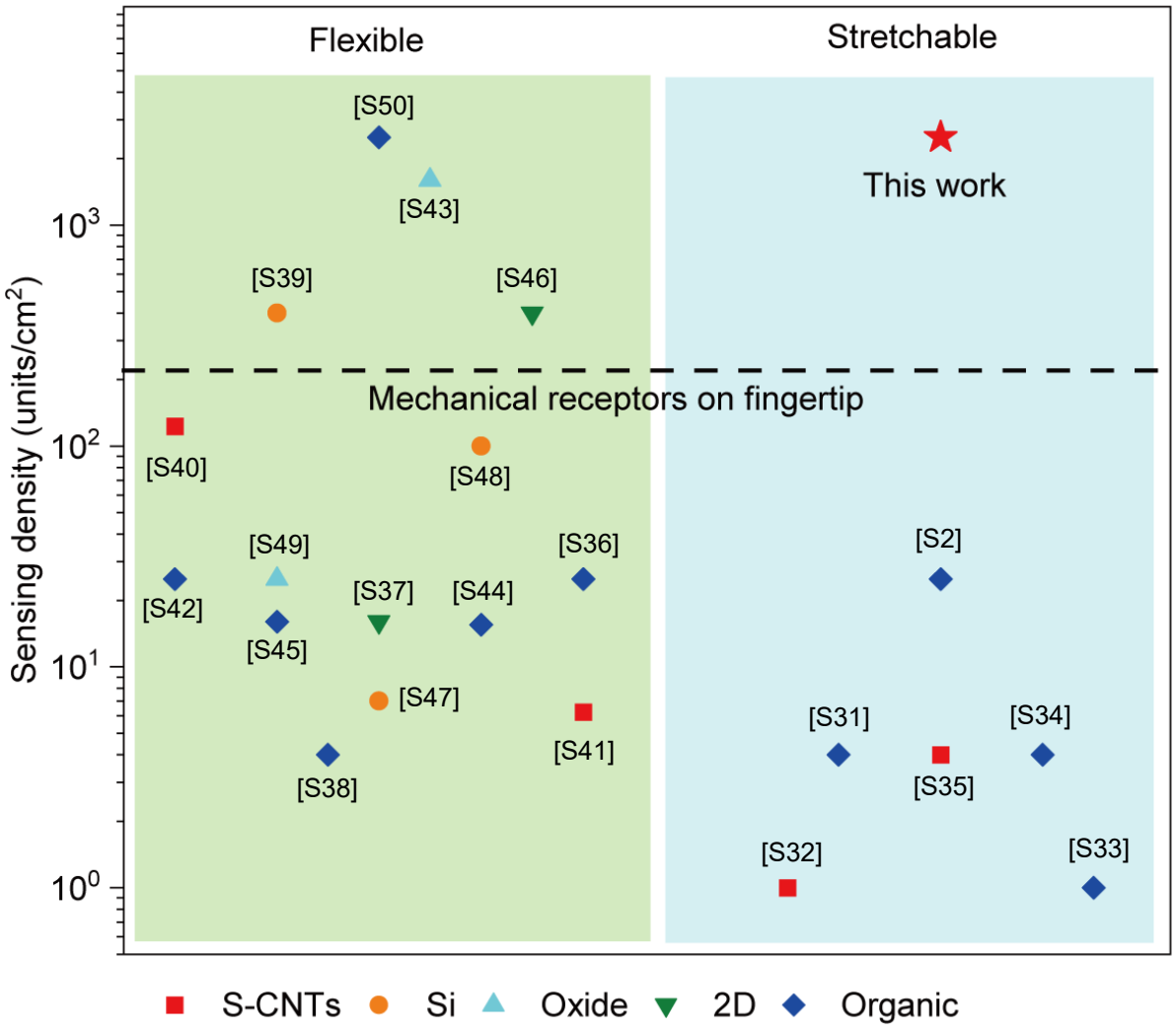
Supplementary Fig. 59. FFC bonding with interconnect on stretchable SEBS substrate. a, Cr/Au as interconnect. At the FFC/SEBS interface, large deformation during pressing caused the interconnects to crack, thus all interconnects showed an open circuit. **b**, EGaIn as interconnect. Because of its high stretchability, EGaIn can survive without forming any cracks after bonding.



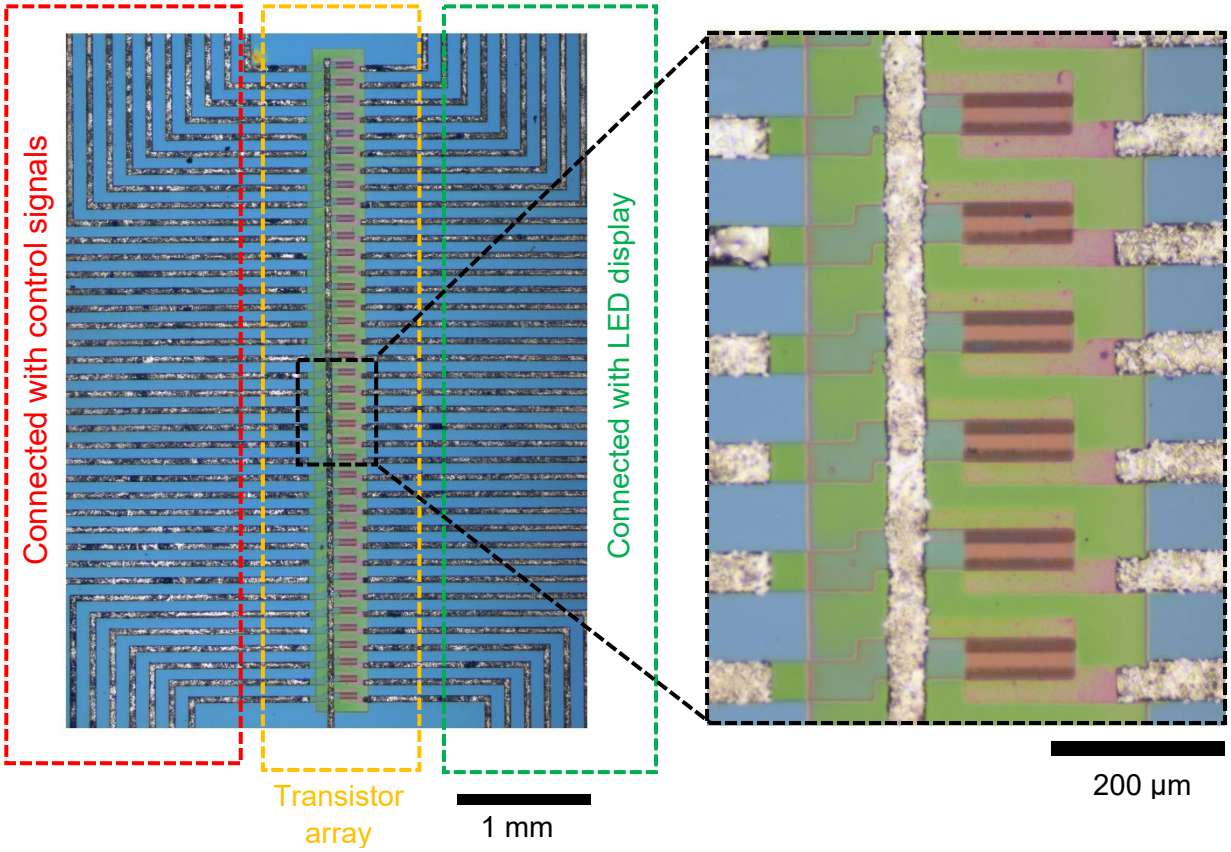
Supplementary Fig. 60. Our bonding methodology of bonding stretchable devices with non-stretchable substrates. a, Schematic diagram. **b**, Photography of an example under strain 0%. **c**, Photography of an example under strain ~50%. **d**, Resistance of bonding w/ or w/o strain.



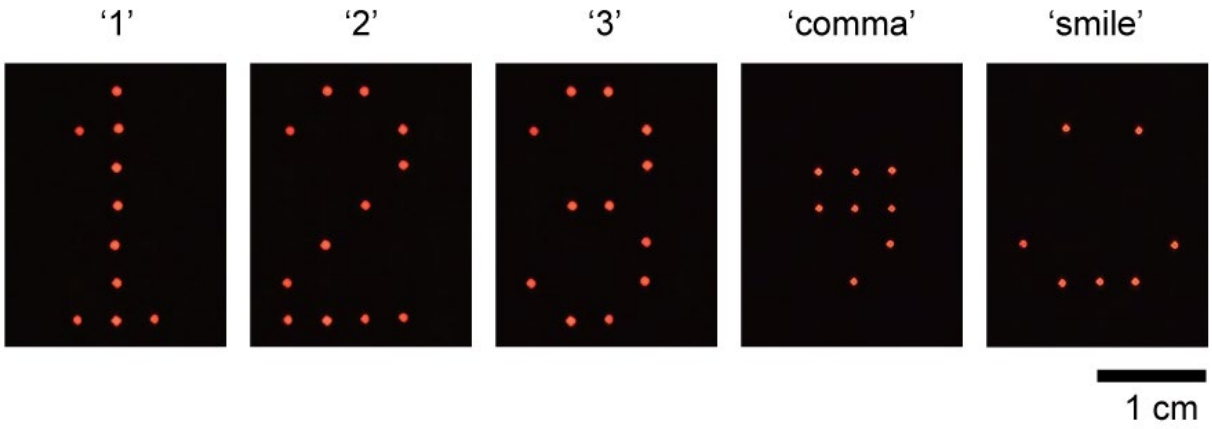
Supplementary Fig. 61. On-state current distribution of active matrix when pressing 3D objects. a, Photography of a breadboard jumper. **b**, On-state current distribution when gently pressing the breadboard jumper. **c**, On-state current distribution when hardly pressing the breadboard jumper. **d**, Photography of a probe needle. **e**, OM image of the probe needle. **f**, On-state current distribution when gently pressing the probe needle.



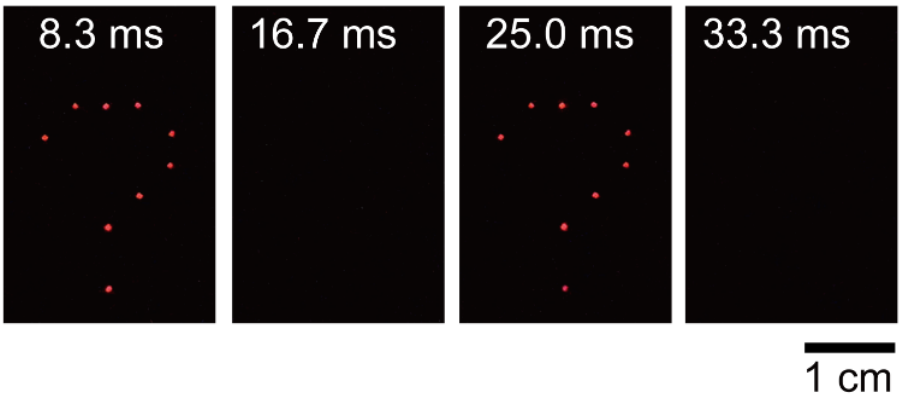
Supplementary Fig. 62. Benchmark of sensing density with other intrinsically stretchable or flexible active-matrix sensor arrays.



Supplementary Fig. 63. Intrinsically stretchable transistor array for LED display driving. Left interconnects are connected to the control signals from MCU/DACs, and right interconnects are connected to LED display.



Supplementary Fig. 64. Photos of intrinsically stretchable transistors-driven LED displays showing different numbers and symbols.



Supplementary Fig. 65. High frequency refreshing of the LED display driven by intrinsically stretchable transistors. These photos are four sequential frames in a recorded 120-fps video, which is the maximum frame rate of the used camera.

Supplementary Table 1 | Comparison of our work with other intrinsically stretchable transistors and flexible transistors reported in the past decade. Only transistors with hysteresis less than 0.5 V are included for the comparison.

Ref.	Technology	Channel material	Channel length (μm)	Device density (Tr/cm^2)	V_{ds} ,V_{gs} (V)	I_{on} density (μA/μm)	Transconductance (μS/μm)	Carrier mobility (cm^{2}V^{-1}s^{-1})	On/off ratio
S2	Stretchable	PSC:DPP	~70	~347	-30, -30	~9.3×10^{-3}	~5.0×10^{-4}	0.98	~10^4
S3	Stretchable	PSC:DPP	~2	~42, 000	-30, -30	~5.8×10^{-3}	~3.0×10^{-4}	0.27	~10^4
S6	Stretchable	PSC:DPP	~150	4	-60, -60	~1.0×10^{-2}	~1.0×10^{-3}	1.0	~10^4
S7	Stretchable	PSC: PII2T	~50	~50	-100, -100	~1.0×10^{-3}	~1.0×10^{-5}	0.56±0.17	~10^3
S8	Stretchable	PSC:DPP	~200	N/A	-40, -40	~5.0×10^{-3}	~3.0×10^{-4}	1.5	~10^5
S9	Stretchable	PSC:DPP	~70	~340	-30, -30	~7.1×10^{-3}	~5.0×10^{-4}	0.51±0.06	~10^4
S10	Stretchable	PSC:DPP	~100	~16	-60, -60	~2.7×10^{-3}	~2.0×10^{-5}	0.29±0.16	~10^5
S11	Stretchable	PSC:DPP	~80	~340	-3, -3	~5.0×10^{-3}	~4.0×10^{-3}	~2.0	~10^5
S12	Stretchable	S-CNTs	~50	~5	-50, -50	~5×10^{-2}	~1.5×10^{-3}	6.18±0.31	~10^4
S13	Stretchable	S-CNTs	~56	~2500	-10, -30	~4.7×10^{-2}	~1.2×10^{-3}	10.45	~10^3
This work	Stretchable	S-CNTs	~100	N/A	-10, -8	~0.39	N/A	20.3±1.6	~10^5
			~2	200, 000	-5, -5	2.0±0.4	~0.8	5.8±1.2	~10^4-10^5
S14	flexible	S-CNTs	2	N/A	-3, -3	8.1±1.4	~6	50	~10^6
S15	flexible	S-CNTs	2	N/A	-2, -3	~6	~5	23.4±2.2	~10^5
S16	flexible	S-CNTs	100	N/A	-5, -2	~0.14	~0.15	70	~10^3
S17	flexible	S-CNTs	20	N/A	-5, -10	~0.32	~0.17	13	~10^5-10^6
S18	flexible	S-CNTs	2	N/A	-2, -2	3.84±0.69	4.69	80	~10^5
S19	flexible	S-CNTs	4	N/A	-5, -5	11.7±3	~4	50	~400
S20	flexible	S-CNTs	50	N/A	-2, -2	~0.24	N/A	48.9	~10^6
S21	flexible	DNTT	1.5	N/A	-2, -3	~0.55	~1	3.7	~10^{10}
S22	flexible	DNTT	1	N/A	-3, -2	1.2	~1.2	1.2	~10^7
S23	flexible	C8-DNBDT-NW	3	N/A	-10, -10	~1.2	~0.33	10	~10^9
S24	flexible	IGZO	7.5	N/A	5, 5	~10	~3	~9.5	~10^8
S25	flexible	IGZO	10	N/A	20, 20	4.8	N/A	~32.3	~10^{10}
S26	flexible	IGZO	20	N/A	5, 10	0.6	~0.3	8	~10^7
S27	flexible	Poly-Si	10	N/A	15, 10	1.6	~0.4	50	~10^6
S28	flexible	Poly-Si	8	N/A	15, 20	~14	~2	88.8	~10^7
S29	flexible	Poly-Si	4	N/A	-1, -20	~5	N/A	62.26	~10^8

PSC: polymer semiconducting material. DNTT: Dinaphthothienothiophene, a small molecule organic semiconductor, C8-DNBDT: 3,11-dioctyldinaphtho[2,3-d:2',3'-d']benzo[1,2-b:4,5-b']dithiophene.

Supplementary Table 2 | Comparison of our work with other intrinsically stretchable integrated circuits.

Ref.	Channel material	Circuit	Logic type	Transistor count	logic gate count	Supply voltage (V)	Operation frequency (Hz)	Gate delay (s)
S2	PSC:DPP	NAND	Pseudo-E	6	1	±30	N/A	N/A
S3	PSC:DPP	Half adder	Pseudo-E	30	5	±20	~0.06	N/A
S9	PSC:DPP	RO	Pseudo-E	16	4	±30	~330	5.1×10^{-4}
S11	PSC:DPP	Neuromorphic circuit	Pseudo-E	54	14	±5	~80	$\sim1.3\times10^{-3}$
S12	CNTs	Temperature sensing	Diode-connected	5	2	10	N/A	N/A
S30	PSC:DPP	Inverter	Pseudo-E	4	1	±30	~5	$\sim2\times10^{-3}$
S31	PSC: P3HT-NFs	NAND	Zero-V_{gs}	3	1	1	N/A	N/A
This work	CNTs	RO	Pseudo-E	16	4	±10	1.9×10^{5}	8.8×10^{-7}
		RO	Zero-V_{gs}	1056	528	10	176	5.4×10^{-6}

Supplementary Table 3 | Material summary for intrinsically stretchable transistors and integrated circuits and comparison with other reported works.

Layer		Reference		
		Nature **555**, 83–88 (2018).	*Science* **373**, 88–94 (2021).	This work
Semiconductor	Materials	DPP	DPP	S-CNTs
	Mobility	~0.98 $cm^2V^{-1}s^{-1}$ @ L_{ch} = 70 μm	~0.26 $cm^2V^{-1}s^{-1}$ @ L_{ch} = 100 μm	~20.3 $cm^2V^{-1}s^{-1}$ @ L_{ch} = 100 μm
S/D electrode	Materials	M-CNTs	PEDOT:PSS	M-CNTs/Pd
	Contact resistance	N/A	~ 1 GΩ·μm	~ 460 kΩ·μm
Gate electrode	Materials	M-CNTs	PEDOT:PSS	PEDOT:PSS
	Sheet resistance	~ 1 kΩ/sq	~ 1 kΩ/sq	~ 1 kΩ/sq
Interconnect	Materials	M-CNTs	PEDOT:PSS	EGaIn
	Sheet resistance	~ 1 kΩ/sq	~ 1 kΩ/sq	<1 Ω/sq
Gate dielectric	Materials	SEBS	PMMA elastomer	NBR/SBES
	Dielectric constant	~2.4	~5.0	~15
	Thickness	~1.25 μm	~1.2 μm	~300 nm
Jumper dielectric	Materials	SEBS	PMMA elastomer	SBS
	Dielectric constant	~2.4	~5.0	~4.3
	Thickness	~1.25 μm	~1.2 μm	~1.9 μm
	Jumper/Gate capacitance ratio	1	1	~0.05
Encapsulation	Materials	N/A	N/A	SBS
Substrate	Materials	SEBS	PMMA elastomer	SEBS
Crosslinker	Semiconductor	N/A	Diazirine	N/A
	Insulators	Azide	Diazirine	NBR / Thiol SEBS / Azide SBS / Thiol
	Conductors	N/A	PEGDMA	M-CNTs/Pd / N/A PEDOT:PSS / PR-PEGMA EGaIn / N/A
Performance	Speed	< 1 kHz	< 1 kHz	>1 MHz
	Maximum transistor number in one circuit	6	30	1056
	Density w/o interconnect (Transistors/cm^2)	~340	~42,000	200,000
	Density w/ interconnect (Transistors/cm^2)	N/A	N/A	100,000

Supplementary Table 4 | Comparison of our work with other intrinsically stretchable and flexible active-matrix sensing technologies.

Ref.	Technology	Channel material	Dielectric material	Sensor type	Density (units/cm^2)
S2	Stretchable	PSC:DPP	SBES	Tactile	25
S31	Stretchable	P3HT-NFs/PDMS	Ion gel	Tactile	4
S32	Stretchable	S-CNTs	Poly(pyromellitic dianhydride-co-4,4′-oxydianiline)	Temperature	1
S33	Stretchable	P3HT-NFs/PDMS	Ion gel	Electrophysiological signal	1
S34	Stretchable	PSC:DPP	PDMS	Strain	4
S35	Stretchable	S-CNTs	$SiO_2/Al_2O_3/SiO_2$	Tactile	4
This work	Stretchable	S-CNTs	NBR/SEBS	Tactile	2,500
S36	flexible	Pentacene	Al_2O_3	Temperature	25
S37	flexible	MoS_2	Al_2O_3	Tactile	16
S38	flexible	DNTT	Al_2O_3	Tactile	4
S39	flexible	Si	SiO_2	Electrophysiological signal	400
S40	flexible	S-CNTs	Al_2O_3	Tactile	100
S41	flexible	S-CNTs	Al_2O_3/HfO_2	Tactile	6.25
S42	flexible	DPP-DTT	Parylene	Photosensor	25
S43	flexible	ITO	Al_2O_3	Tactile	1,600
S44	flexible	Pentacene	Polyimide	Tactile	15.5
S45	flexible	Pil2TS9	PDMS	Tactile	16
S46	flexible	MoS_2	Air	Tactile	400
S47	flexible	Si	Al_2O_3	Tactile	6.9
S48	flexible	Si	SiO_2	Pressure	100
S49	flexible	In_2O_3	SiO_2/Al_2O_3	Tactile	25
S50	flexible	Pentacene	SU-8	Imager	2,500

PSC: polymer semiconductor. DNTT: Dinaphthothienothiophene, a small molecule organic semiconductor. Pil2TS9: Polyisoindigobithiophene-siloxane. P3HT: Poly(3-hexylthiophene).

Supplementary Video 1

Intrinsically stretchable transistors drive a display system showing different numbers, letters and symbols.

Supplementary Video 2

Intrinsically stretchable transistors drive a display system with a refreshing rate of 60 Hz.

Supplementary References

S1. Andrews, J. B. *et al.* Patterned liquid metal contacts for printed carbon nanotube transistors. *ACS Nano* 12, 5482−5488, (2018).

S2. Wang, S. *et al.* Skin electronics from scalable fabrication of an intrinsically stretchable transistor array. *Nature* **555**, 83–88 (2018).

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S5. Zhong, D., Xiao, M., Zhang, Z. & Peng L. -M. Solution-processed carbon nanotubes based transistors with current density of 1.7 mA/μm and peak transconductance of 0.8 mS/μm. *IEEE Int. Electron Devices Meet*, 5.6.1-5.6.4 (2017).

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S7. Liang, J. J. *et al.* Intrinsically stretchable and transparent thin-film transistors based on printable silver nanowires, carbon nanotubes and an elastomeric dielectric. *Nat. Commun.* **6,** 7647 (2015).

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