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Supplementary information

Qubits made by advanced semiconductor manufacturing

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Supplementary Information - Qubits made by advanced semiconductor manufacturing

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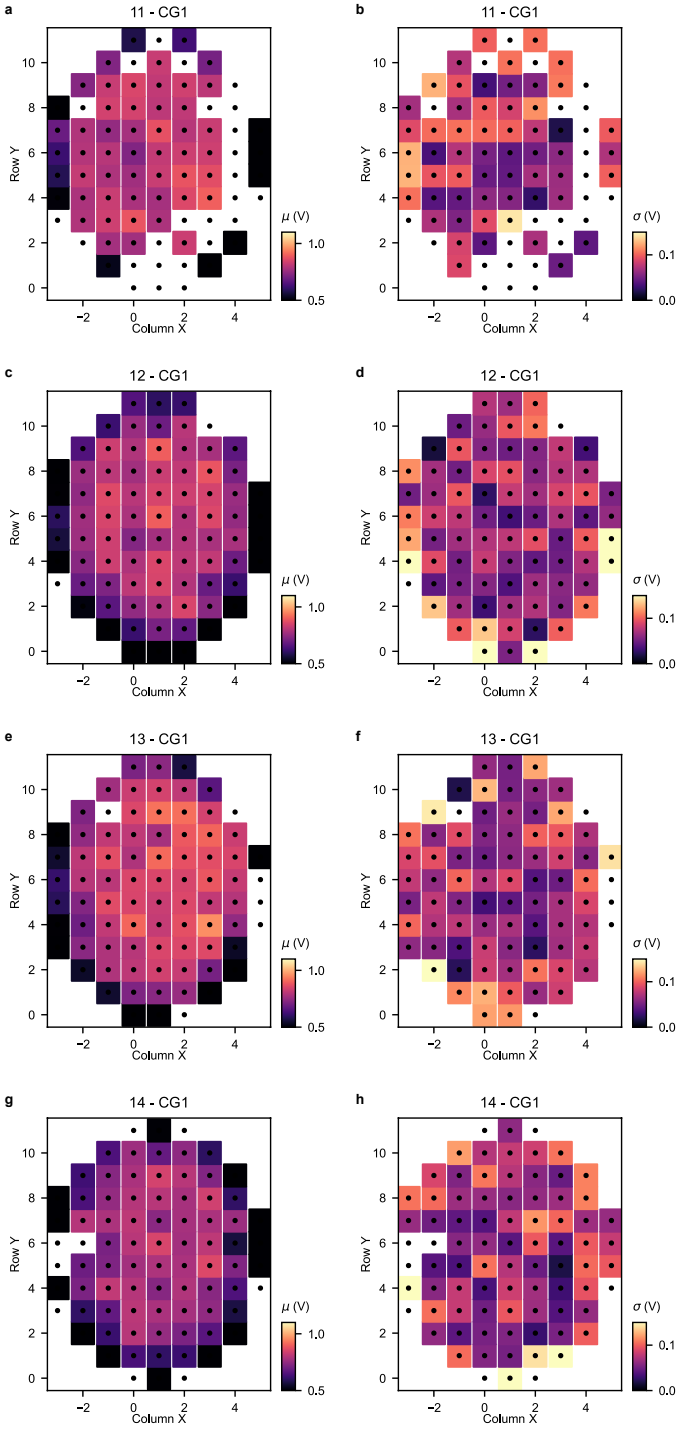
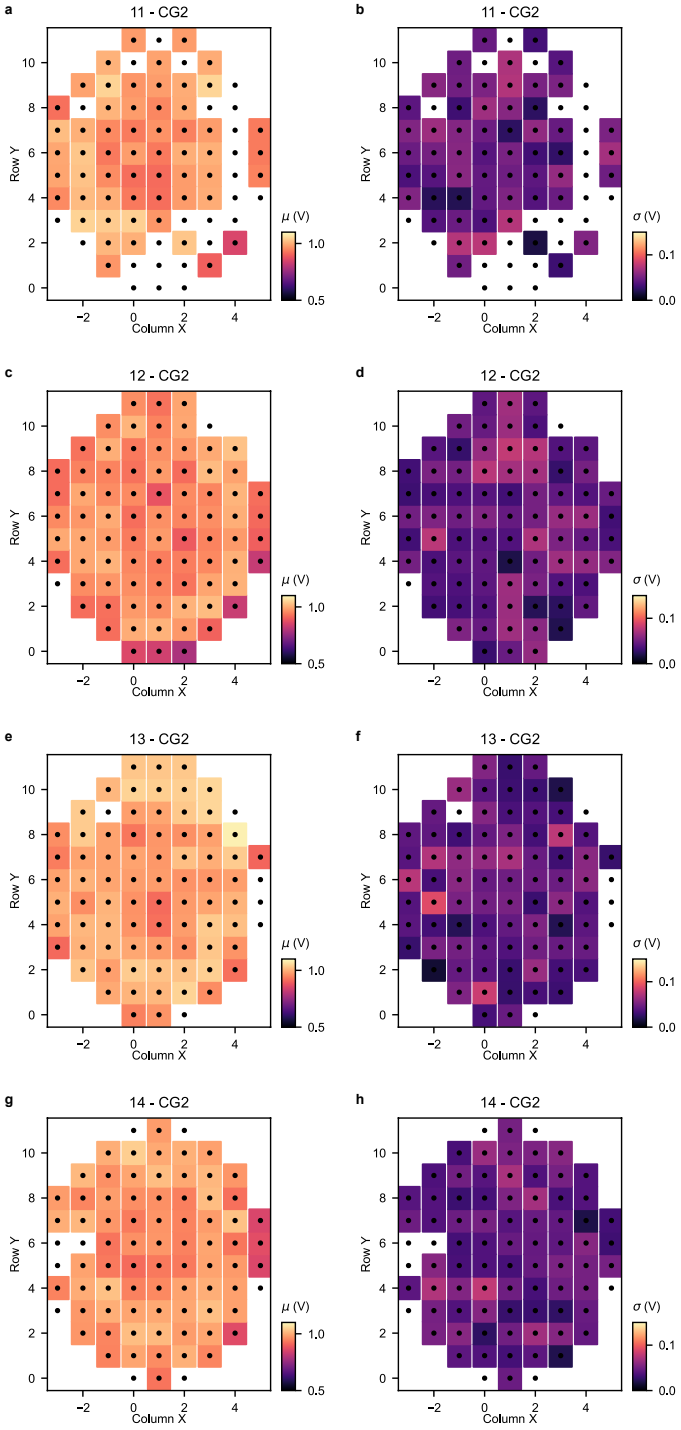
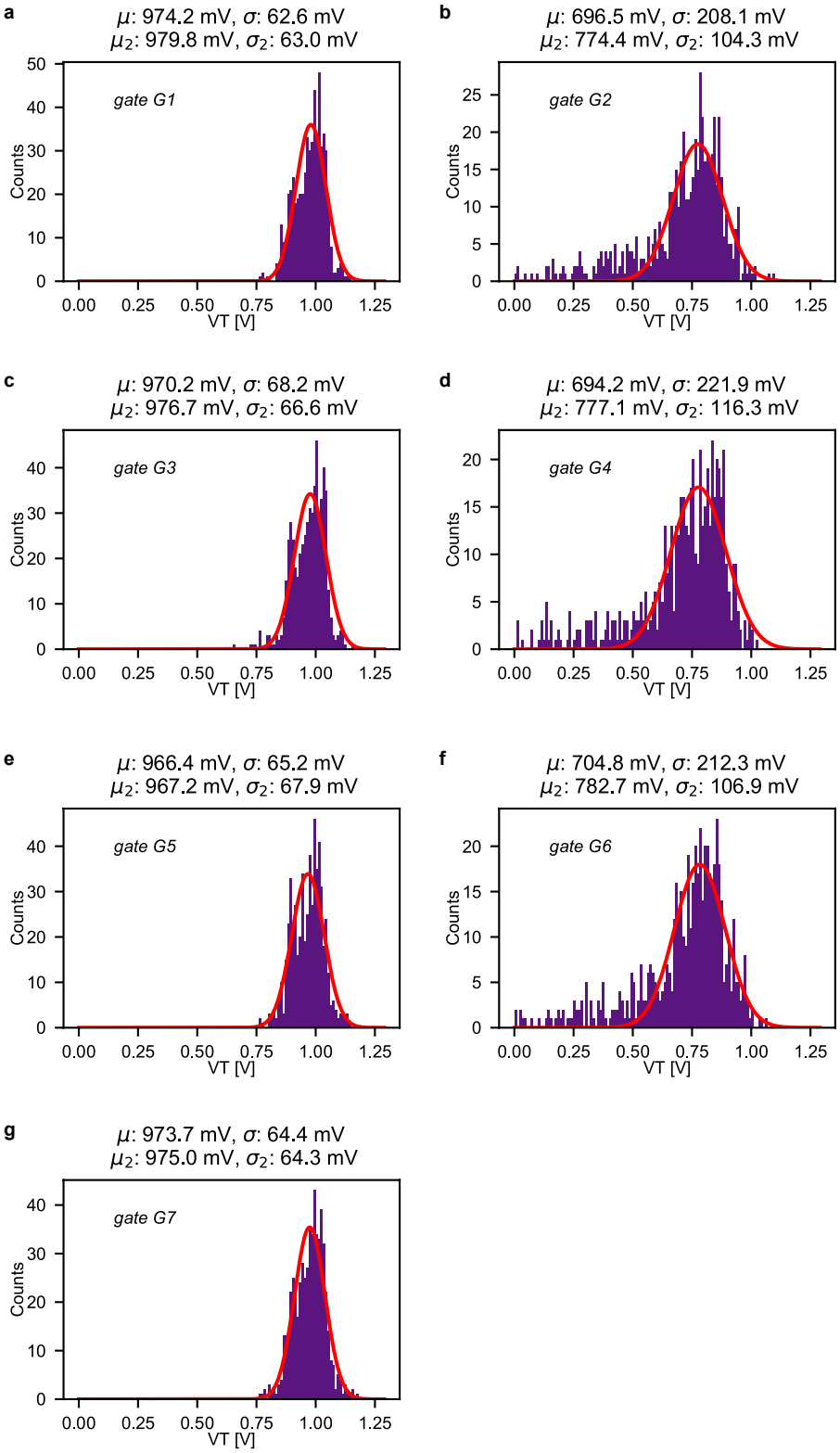


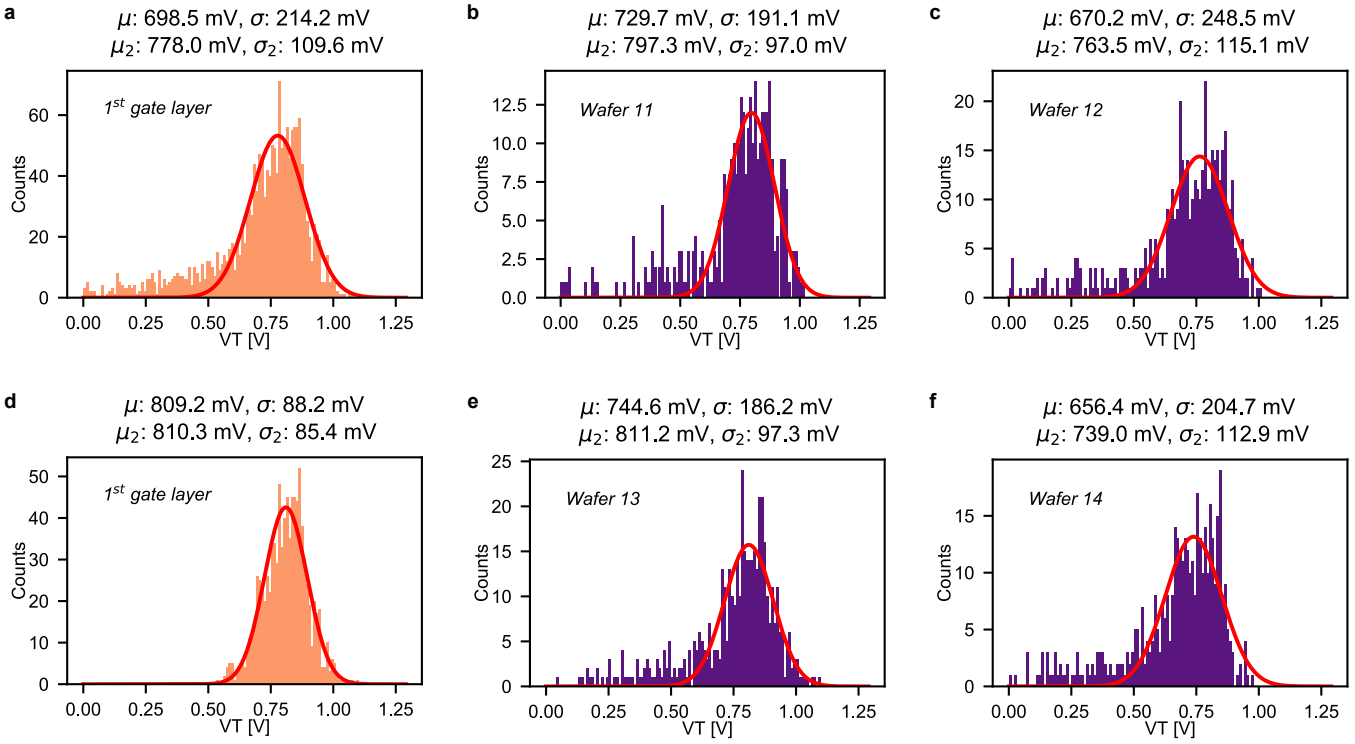
SUPPLEMENTARY FIG. 1. **Cross-wafer variation of threshold voltages of the first gate layer at room temperature.** For each yielding device on the almost identical wafers 11, 12, 13 and 14, the threshold voltage for the seven gates on both fins is analysed. Each device has two gate layers. Gate layer 1 contains gates G2, G4 and G6 and gate layer 2 contains gates G1, G3, G5 and G7. **a, c, e, g,** Mean threshold voltage per device of the three gates of the first gate layer (even-numbered) for the yielding devices on wafer 11 (**a**), 12 (**c**), 13 (**e**) and 14 (**g**). The samples at the edge of the wafer consistently have a lower threshold voltage than the samples at the center of the wafer. **b, d, f, h,** Standard deviation of the threshold voltages per device of the first gate layer for the yielding devices on wafer 11, 12, 13 and 14. Apart from a few outliers, the standard deviation of the threshold voltage per sample is always below 145 mV.



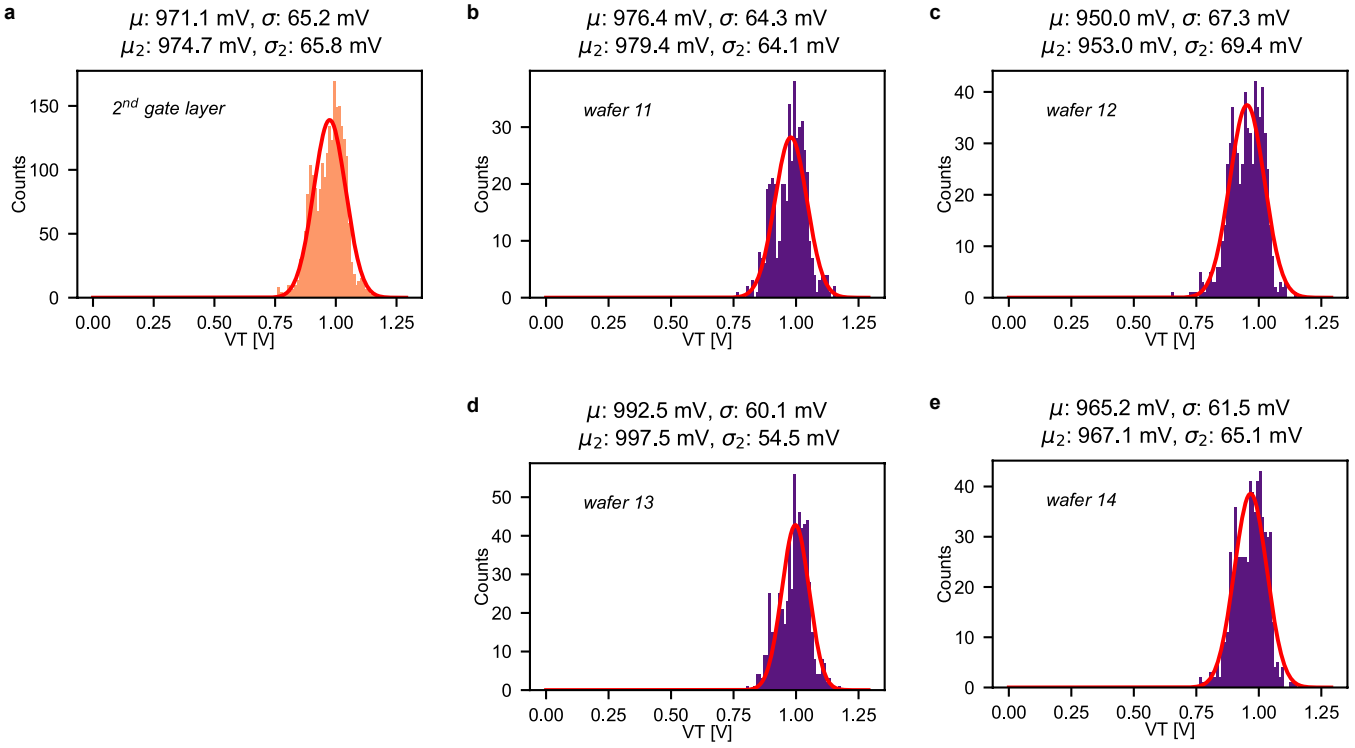
SUPPLEMENTARY FIG. 2. **Cross-wafer variation of threshold voltages of the second gate layer at room temperature.** For each yielding device on the almost identical wafers 11, 12, 13 and 14, the threshold voltage for the seven gates on both fins is analysed. Each device has two gate layers. Gate layer 1 contains gates G2, G4 and G6 and gate layer 2 contains gates G1, G3, G5 and G7. **a, c, e, g,** Mean threshold voltage per device of the four gates of the second gate layer (odd-numbered) for the yielding devices on wafer 11 (**a**), 12 (**c**), 13 (**e**) and 14 (**g**). **b, d, f, h,** Standard deviation of the threshold voltages per device of the second gate layer for the yielding devices on wafer 11, 12, 13 and 14. Apart from a few outliers, the standard deviation of the threshold voltage per sample is always below 70 mV.



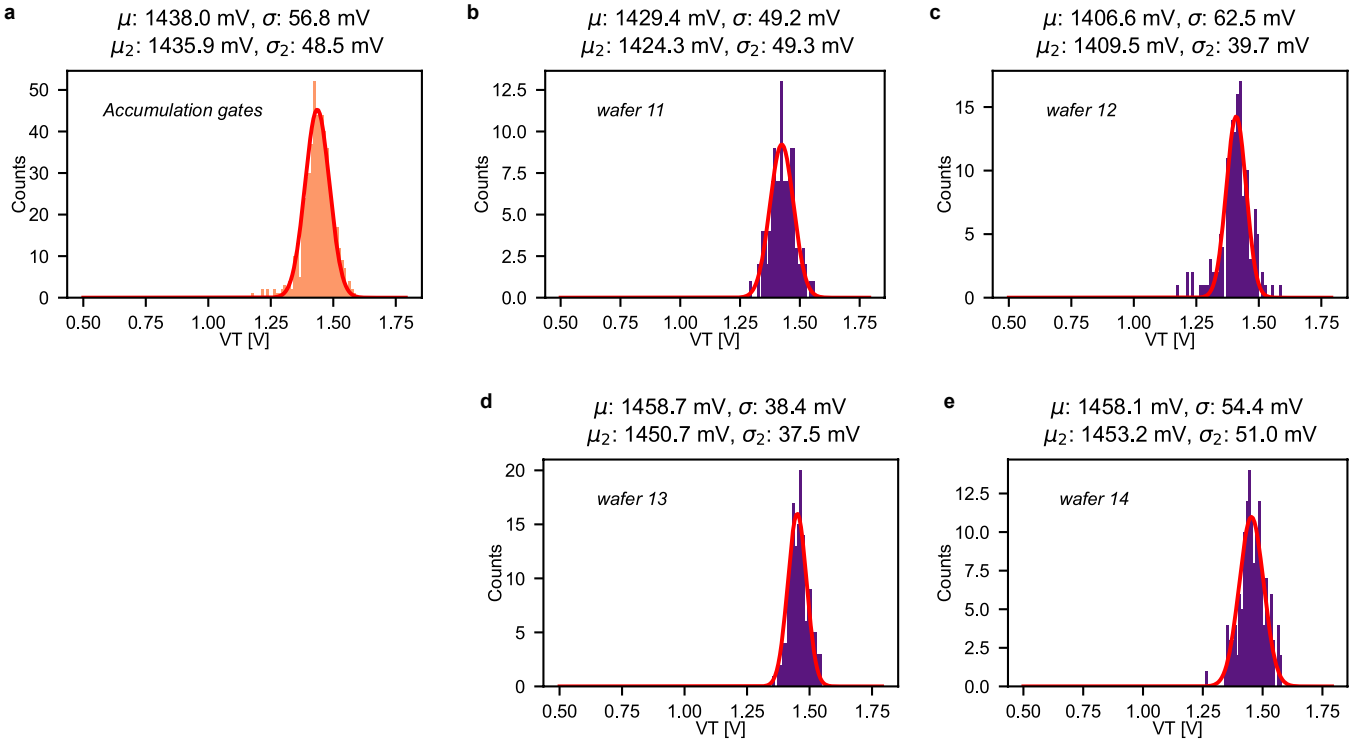
SUPPLEMENTARY FIG. 3. **Histograms of threshold voltage per gate at room temperature.** Histograms for the threshold voltage per gate (G1-G7) for all yielding samples on wafers 11-14. We see that the gates on gate layer 1, G2 (**b**), G4 (**d**) and G6 (**f**) have a wider spread in threshold voltage than the gates from gate layer 2 G1 (**a**), G3 (**c**), G5 (**e**) and G7 (**g**). This is mainly caused by the fact that the samples around the edges of the wafers consistently show significantly lower threshold voltages for the first gate layer than samples in the center of the wafer (see Extended Data Fig. 1). When we analyse each gate separately, we observe that the mean value and the standard deviation for all three gates in gate layer one is of similar order per gate, as are the mean and standard deviation for the four gates of gate layer 2. In addition to the mean and standard deviation of the individual threshold voltages, we provide above each panel in the second line the mean and the standard deviation of a Gaussian distribution fitted to the data (red line).



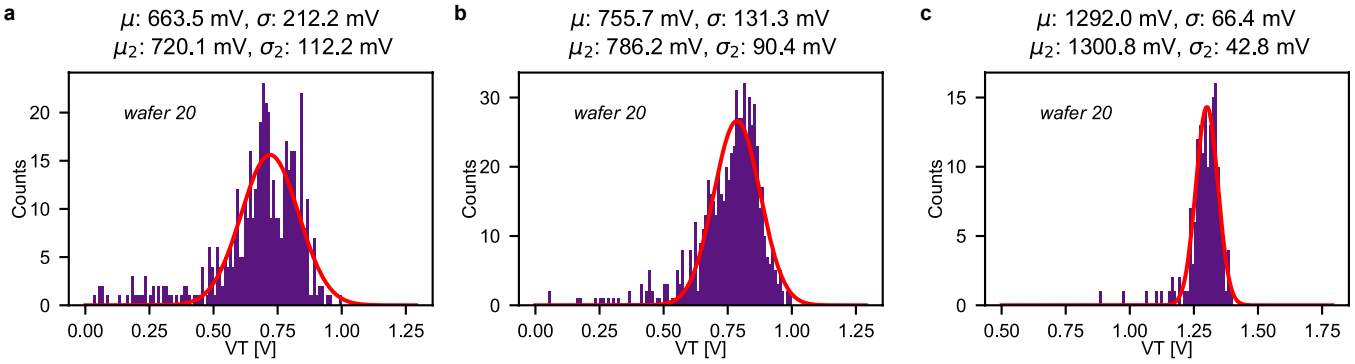
SUPPLEMENTARY FIG. 4. **Histograms of threshold voltage per wafer for the first gate layer at room temperature. a,** Histograms for the threshold voltage for all gates of the first gate layer of both fins for all yielding samples of wafers 11, 12, 13 and 14. **b, c, e, f** Histograms for the threshold voltage for all gates of the first gate layer of both fins for all yielding samples of wafer 11 (**b**), 12 (**c**), 13 (**e,**) and 14 (**f**). **d,** Histograms for the threshold voltage for all gates of the first gate layer of both fins for all yielding samples of wafers 11, 12, 13 and 14, while not taking into account the samples at the edge. We see that when only taking into account the samples at the center of the four wafers, the standard deviation approaches that for the second gate layer (Extended Data Fig 5), where this edge-effect is not apparent. The average threshold voltage is a bit lower for the first gate layer than for the second gate layer. This can be explained by the extra oxide layer between the second gate layer and the sample. In addition to the mean and standard deviation determined by the individual threshold voltages, we provide above each panel in the second line the mean and the standard deviation of a Gaussian distribution fitted to the data (red line).



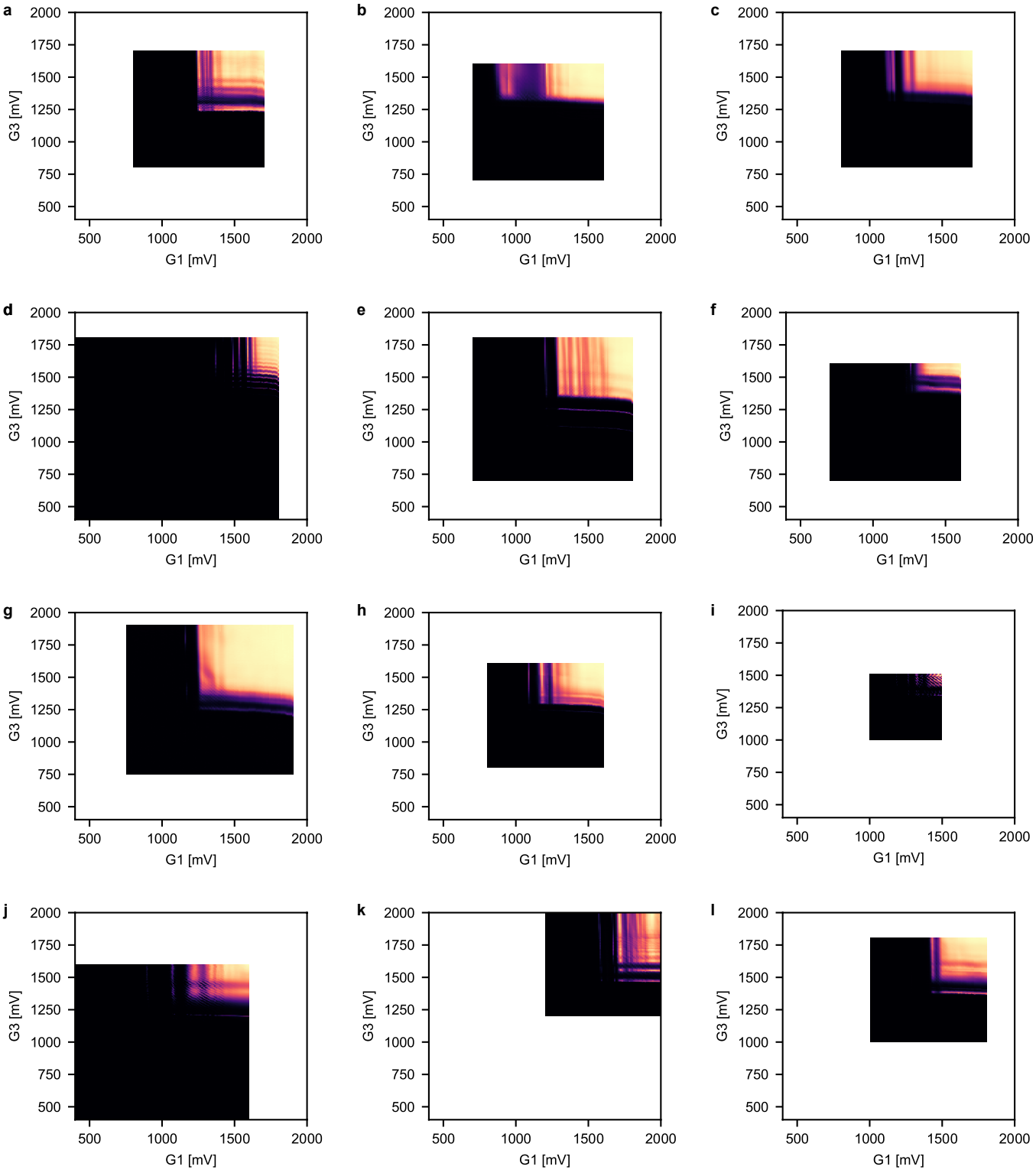
SUPPLEMENTARY FIG. 5. **Histograms of threshold voltage per wafer for the second gate layer at room temperature. a,** Histograms for the threshold voltage for all gates of the second gate layer of both fins for all yielding samples of wafers 11, 12, 13 and 14. **b, c, d, e** Histograms for the threshold voltage for all gates of the second gate layer of both fins for all yielding samples of wafer 11 (**b**), 12 (**c**), 13 (**d**) and 14 (**e**). In addition to the mean and standard deviation of the individual threshold voltages, we provide above each panel in the second line the mean and the standard deviation of a Gaussian distribution fitted to the data (red line).



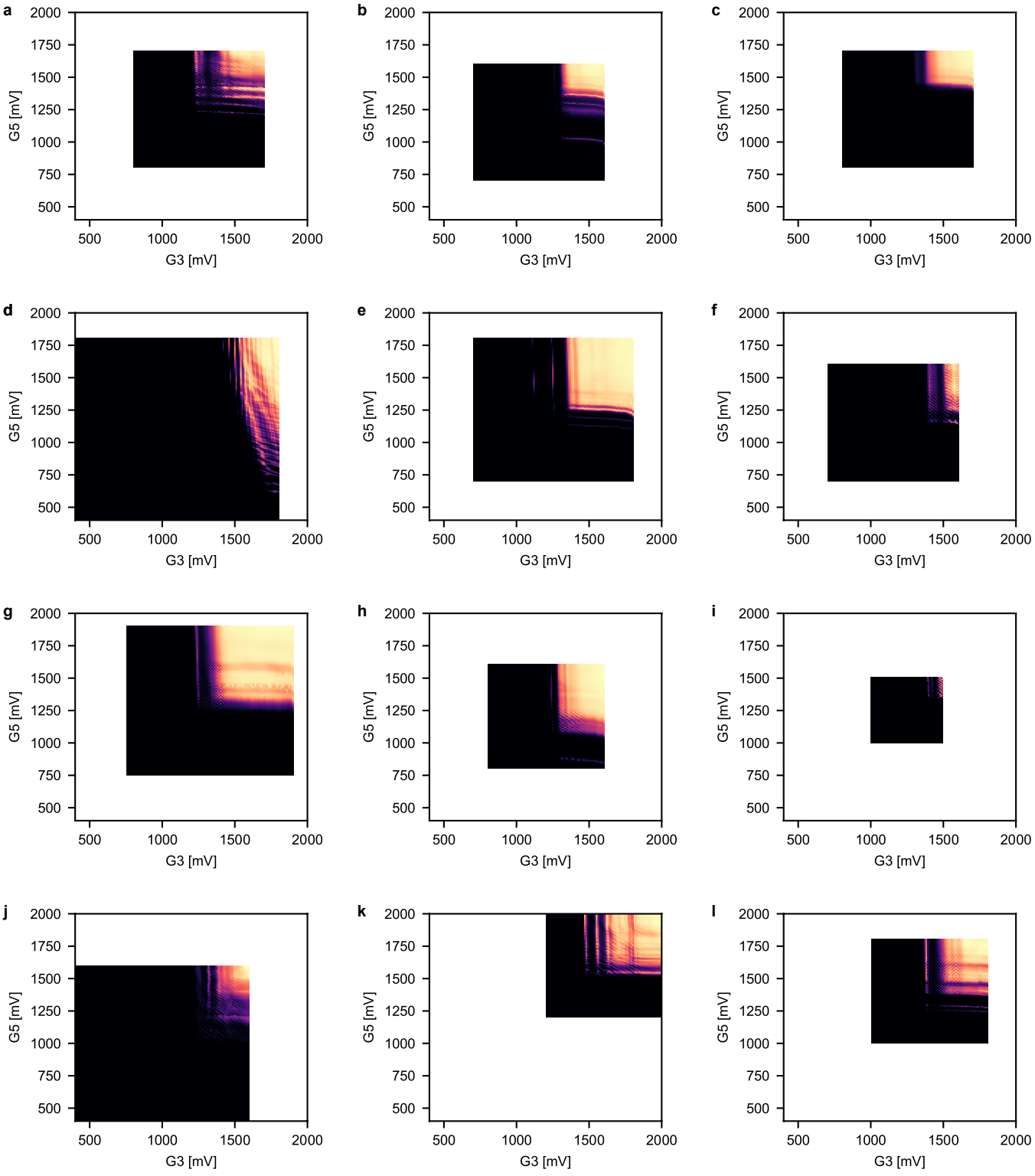
SUPPLEMENTARY FIG. 6. **Histograms of threshold voltage per wafer for the accumulation gates at room temperature. a,** Histograms for the threshold voltage for all accumulation gates of both fins for all yielding samples of wafers 11, 12, 13 and 14. **b, c, d, e,** Histograms for the threshold voltage for all accumulation gates of both fins for all yielding samples of wafer 11 (**b**), 12 (**c**), 13 (**d**) and 14 (**e**). The standard deviation of the accumulation gates per wafer is significantly smaller than the standard deviation of gate layer 1, the gate layer in which also the accumulation gates are fabricated. We expect this to be caused by the larger size of the accumulation gates compared to the finger gates in gate layer 1. The spread in threshold voltages for the accumulation gates is also smaller than the spread in threshold voltages of gate layer 2. In addition to the mean and standard deviation of the individual threshold voltages, we provide above each panel in the second line the mean and the standard deviation of a Gaussian distribution fitted to the data (red line).



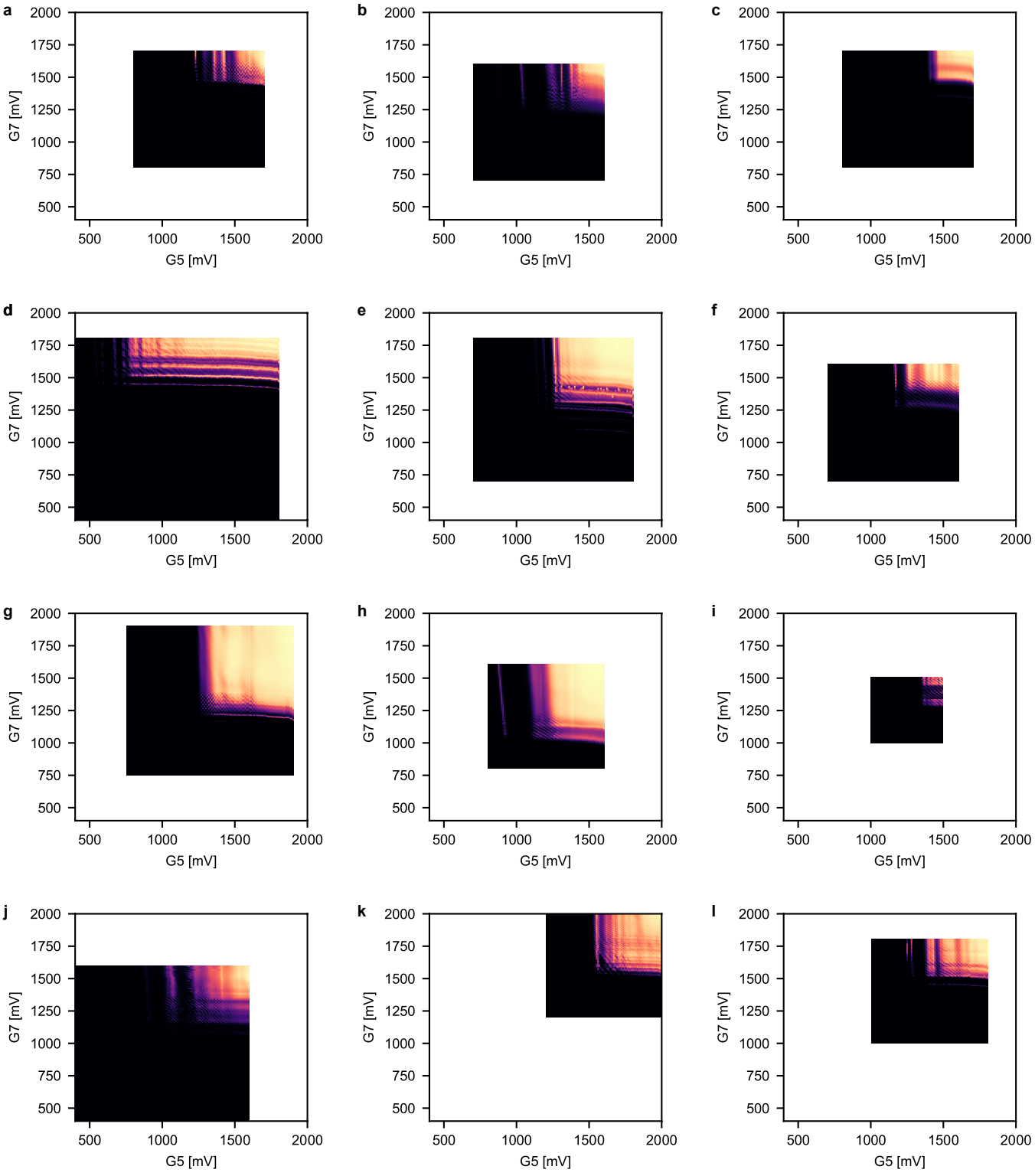
SUPPLEMENTARY FIG. 7. **Histograms of threshold voltage for the gates of wafer 20 at room temperature. a, b, c** Histograms for the threshold voltage for all gates of both fins for all yielding samples of gate layer 1 (**a**), gate layer 2 (**b**) and the accumulation gates (**c**) of wafer 20, the wafer containing the samples with the stripline.



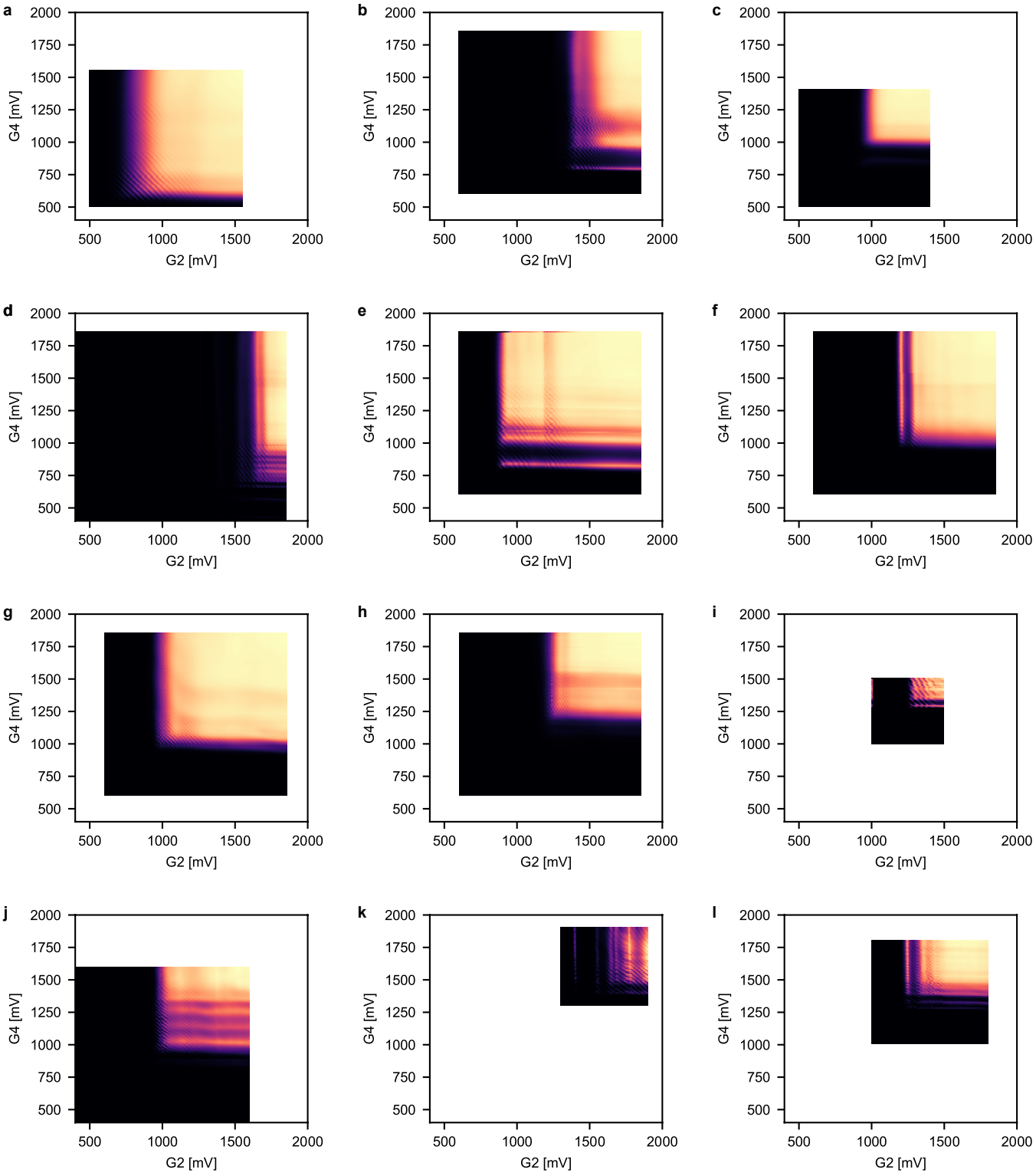
SUPPLEMENTARY FIG. 8. **Barrier-barrier maps for gates** $G1$**-**$G3$**.** Barrier-barrier maps for a quantum dot under gate $G2$ for 12 different samples, taken from yielding devices across wafers 11 (**a-c**), 12 (**d-f**), 13 (**g-i**) and 14 (**j-l**). For each sample, we are able to form a quantum dot.



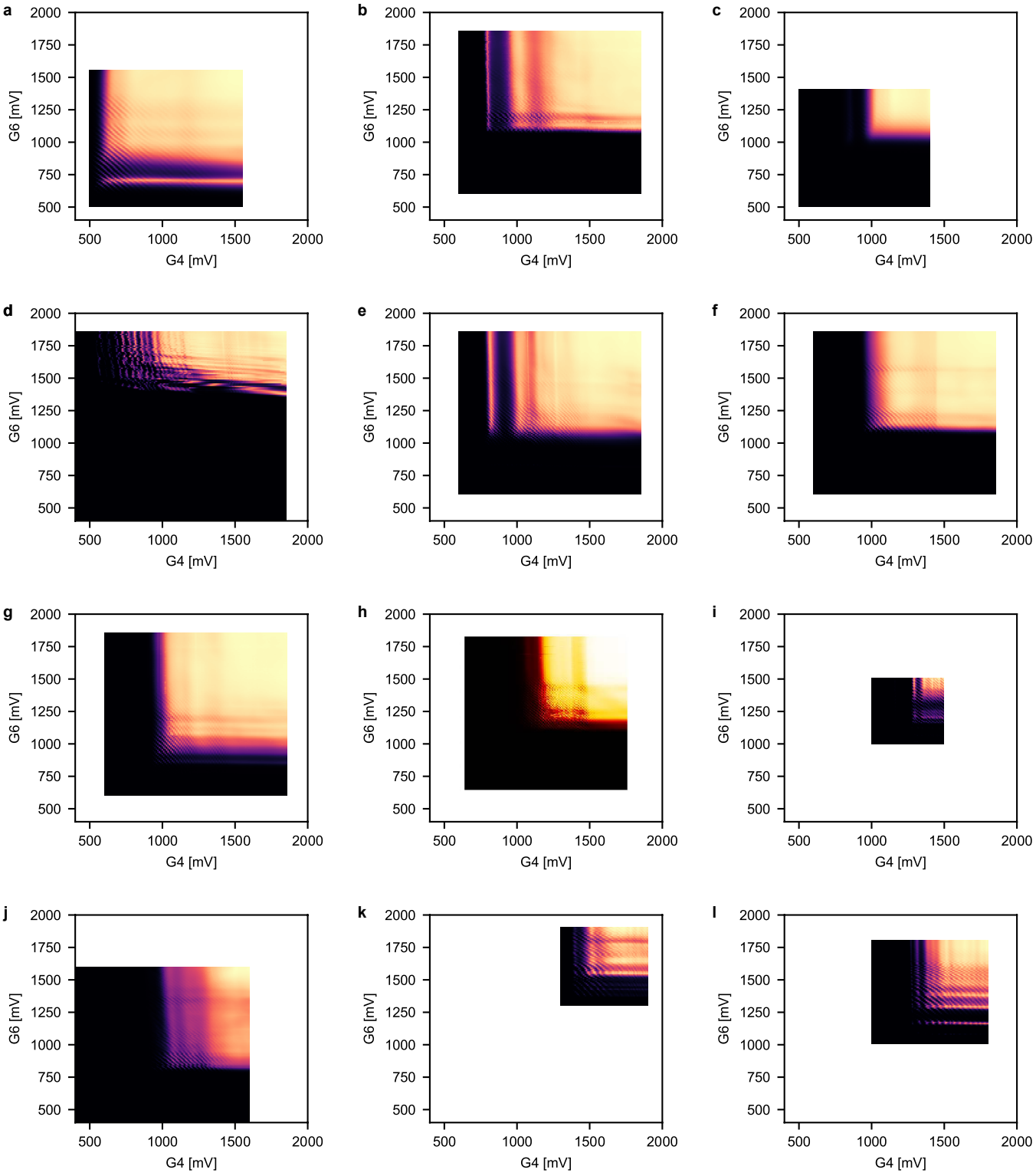
SUPPLEMENTARY FIG. 9. **Barrier-barrier maps for gates** $G3$**-**$G5$**.** Barrier-barrier maps for a quantum dot under gate $G4$ for 12 different samples, taken from yielding devices across wafers 11 (**a-c**), 12 (**d-f**), 13 (**g-i**) and 14 (**j-l**). For each sample, we are able to form a quantum dot.



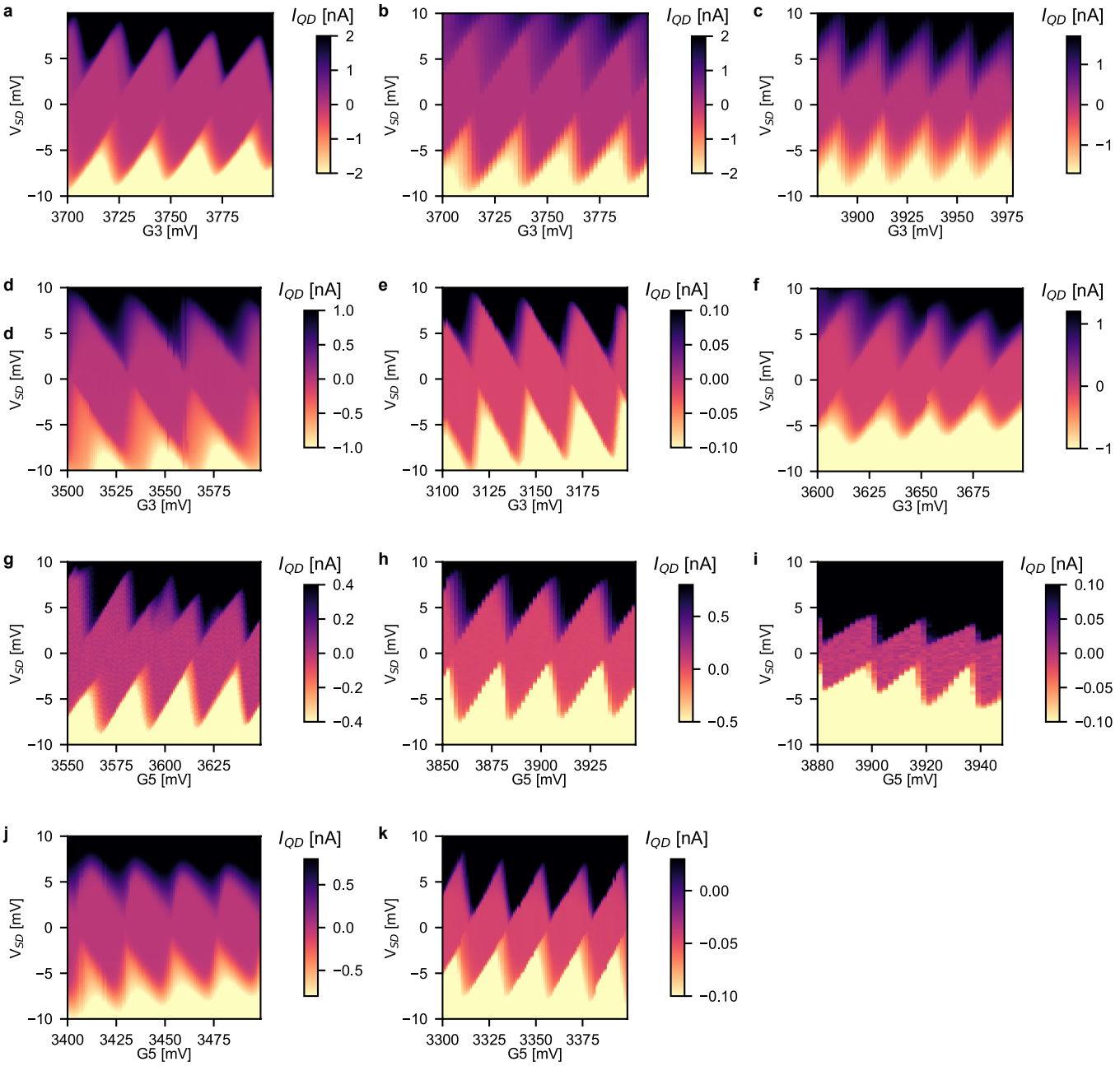
SUPPLEMENTARY FIG. 10. **Barrier-barrier maps for gates** $G5$-$G7$**.** Barrier-barrier maps for a quantum dot under gate $G6$ for 12 different samples, taken from yielding devices across wafers 11 (**a-c**), 12 (**d-f**), 13 (**g-i**) and 14 (**j-l**). For each sample, we are able to form a quantum dot.



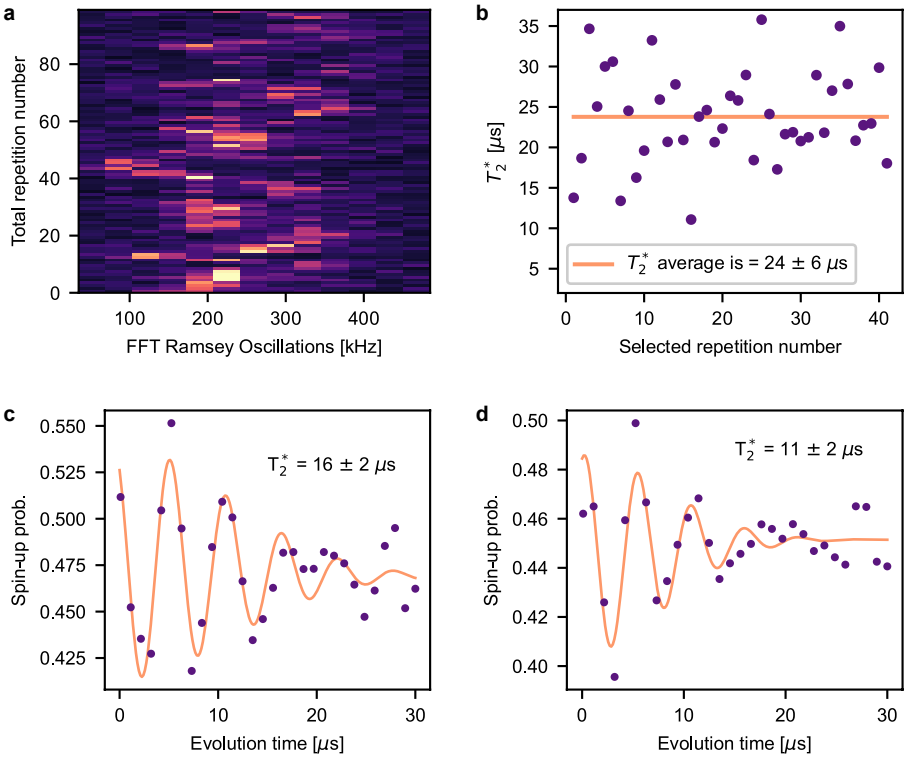
SUPPLEMENTARY FIG. 11. **Barrier-barrier maps for gates** $G2$-$G4$**.** Barrier-barrier maps for a quantum dot under gate $G3$ for 12 different samples, taken from yielding devices across wafers 11 (**a-c**), 12 (**d-f**), 13 (**g-i**) and 14 (**j-l**). For each sample, we are able to form a quantum dot.



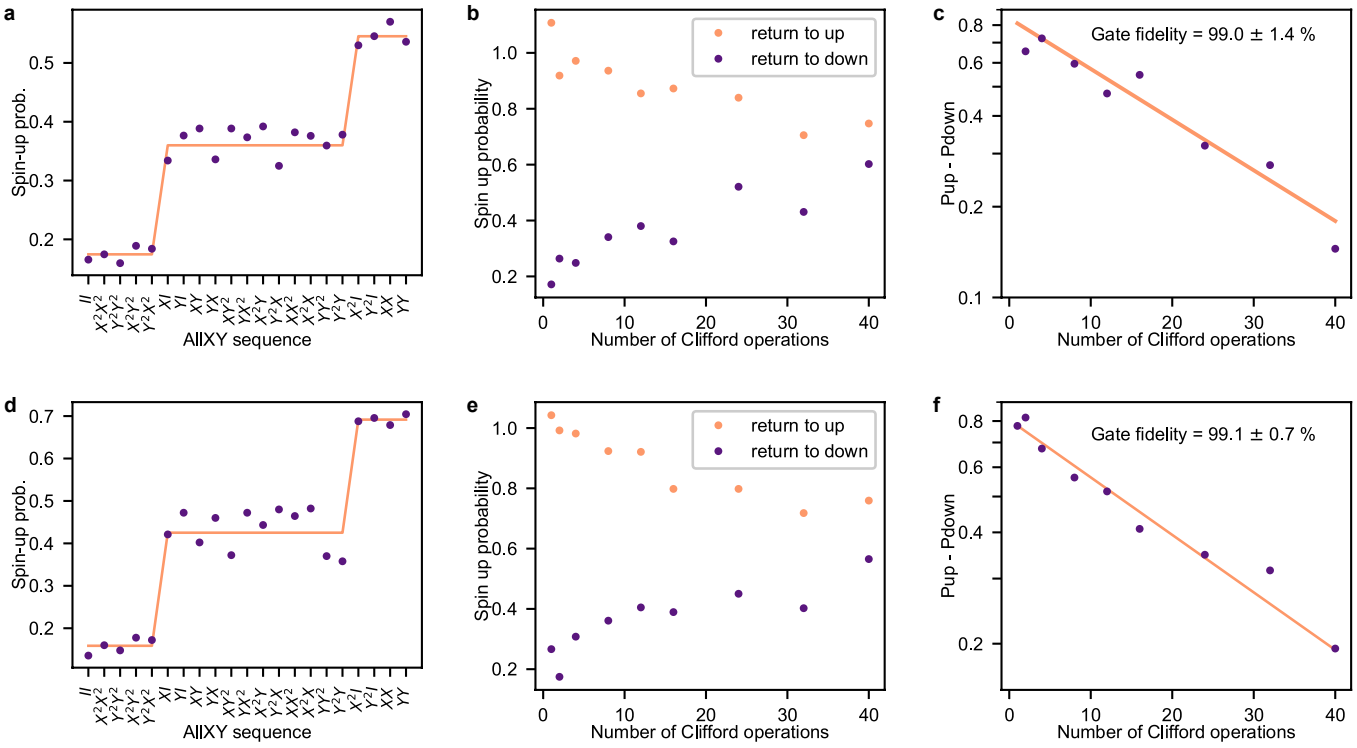
SUPPLEMENTARY FIG. 12. **Barrier-barrier maps for gates** *G*4-*G*6**.** Barrier-barrier maps for a quantum dot under gate *G*5 for 12 different samples, taken from yielding devices across wafers 11 (**a-c**), 12 (**d-f**), 13 (**g-i**) and 14 (**j-l**). For each sample, we are able to form a quantum dot. For the dot in **h**, the data was not stored properly, so the figure is reproduced from a screenshot.



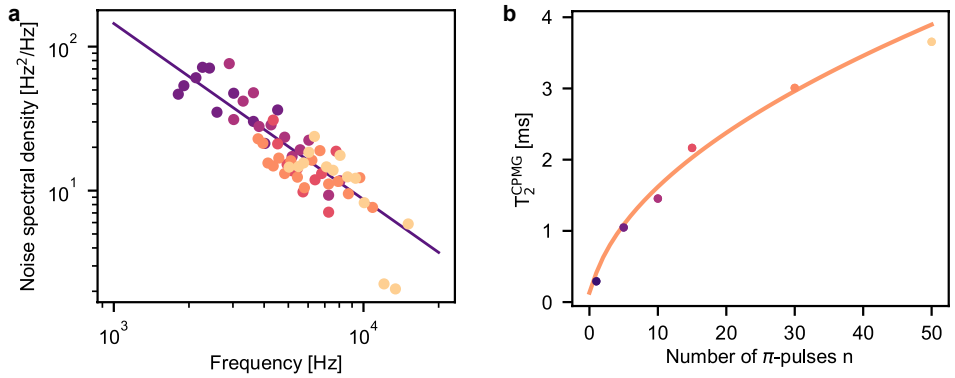
SUPPLEMENTARY FIG. 13. **Coulomb diamonds.** Typical Coulomb blockade diamonds measured in the multi-electron regime, taken on four different samples from the same wafer for dots under gate G3 (**a-f**) and under gate G5 (**g-k**). The dot in the main text, is the dot in **i**. From these diamonds, the quantum dot charging energy and the gate lever arms are determined. Coulomb diamonds are measured by scanning a gate voltage versus the bias voltage applied between the source and the drain contact. When the electrochemical potential of the quantum dot falls outside the bias window, the current through the quantum dot is blocked, i.e. the sample is in Coulomb blockade. Once the electrochemical potential of the quantum dot is aligned within the bias window, Coulomb blockade is lifted. The bias window increases along the vertical axis, hence Coulomb blockade is lifted over a wider gate voltage range. The regions of blockaded current have the characteristic diamond shape. Here, we extract an average charging energy of 8.9 ± 0.1 meV (lever arm: 0.37 ± 0.02 meV/mV) for the dot under G3 (**a**, **c**, **e**, **g**, **i**, **k**) and an average charging energy of 8.0 ± 1.4 meV for the dot under G5 (**b**, **d**, **f**, **h**, **j**). The larger standard deviation in the charging energy of the dot under G5 is mainly caused by the charging energy of the dot in **f** being 5.2 meV, as opposed to the other dots being between 8.7 and 9.0 meV. The average lever arm for G5 dot is 0.36 ± 0.1 meV/mV.



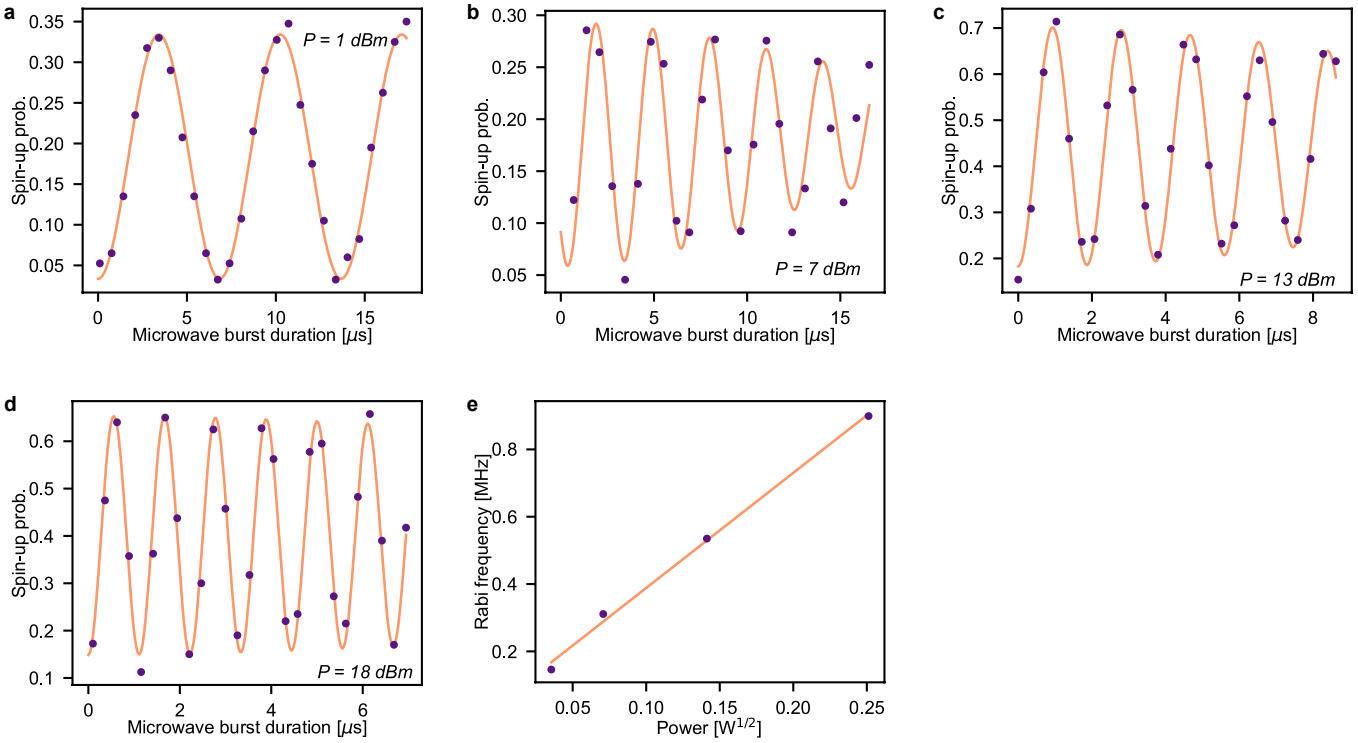
SUPPLEMENTARY FIG. 14. **Ramsey analysis over time. a,** Fast Fourier transform (FFT) of a Ramsey experiment. The data consists of 100 traces, each trace is an average of 200 repetitions. The entire measurement takes three hours in total. The FFT of the Ramsey fringes shows frequency jumps over the timescale of the measurement. Each trace is fitted individually with a decaying Gaussian curve and the fit is analysed by calculating the mean square error. We keep the 41 traces with mean square error below a given threshold. **b,** Extracted T_2^* for the selected traces (purple dots). The average of the $T2^*$ times of the selected traces is 24±6 μs (orange line). **c,** Ramsey decay curve. The data points are the averaged data of the 41 selected traces. The fit gives a T_2^* time of 16±2 μs. **d,** Ramsey decay curve. The data points are the average of all 100 traces of the two hour and 40 minute measurement. The fit gives a T_2^* time of 11±2 μs.



SUPPLEMENTARY FIG. 15. **AllXY and Randomised benchmarking. a, d,** To check the calibration of the single-qubit gates we perform an AllXY sequence [1] on **a,** qubit 1 and **d,** qubit 2. Each data point corresponds to the outcome after sequentially applying two gates from the set I, X, X^2, Y, Y^2, where X and Y indicate 90° rotations. The data points should ideally follow a staircase pattern (solid line) and deviations from this indicate calibration errors. **b, c, e, f,** To determine the single-qubit gate fidelity, we perform randomised benchmarking [2, 3]. In randomised benchmarking, we randomly select p gates from a set of 24 gates that form the Clifford group and apply them to the qubit. At the end of the sequence we apply an inverting gate from the Clifford group that ideally takes the qubit state back to either $|0\rangle$ or $|1\rangle$. In this experiment, the Clifford gates are decomposed to the set of primitive gates I, $\pm$X, $\pm X^2$, $\pm$Y, $\pm Y^2$. On average a Clifford gate contains 1.875 primitive gates. **b, e,** Normalised spin-up probability as a function of the number of Clifford operations applied for **b,** qubit 1 and **e,** qubit 2. The orange and purple data points correspond to sequences producing a net Clifford of X^2 or I, respectively, ideally taking the spin to either spin up or spin down. Each data point corresponds to 40 randomisations of the Clifford sequence and the normalisation is done by additional calibration experiments where we apply either just I or X^2 to the qubit. **c, f,** The difference between the purple and orange data points in **b, e,** is fitted with and exponential of the form VP_c^p. From this we derive an average Clifford-gate fidelity of $F_C = 1-(1-P_c)/2$ of $98.1\pm2.7\%$ and $98.2\pm1.4\%$ for qubit 1 and qubit 2 respectively. This translates to a primitive gate fidelity of $99.0 \pm 1.4\%$ and $99.1 \pm 0.7\%$ for Q1 and Q2.



SUPPLEMENTARY FIG. 16. **Noise analysis for qubit 1. a,** Dynamical decoupling pulses for which the time between two subsequent π-pulses is fixed, can act as a filter function for Gaussian noise [4, 5]. The filter function peaks at a frequency of $f_0 = \frac{n}{2t_{wait}}$, with n the number of π-pulses and t_{wait} the evolution time. When the filter is sufficiently narrow around the frequency f_0, the noise within the bandwidth can be regarded as constant. We can use this to relate the amplitude of the CPMG decay, A_{CPMG}, for each wait time and number of π pulses, to the dominant noise spectrum for the qubit: $S(f_0) = -\ln(A_{CPMG})/2\pi^2 t_{wait}$ [6, 7]. Here, we plot the noise spectrum, $S(f)$ as a function of frequency for the data shown in Fig. 4c of the main text. We only take data points into account for which $0.15 < A_{CPMG} < 0.85$. We assume that the noise spectrum dominating spin decoherence is described by a power law and use the fit function $Bf^{-\gamma}$. We obtain $\gamma = 1.2 \pm 0.1$ and a noise value at 1 Hz of $B = 820 \pm 750$ Hz$/\sqrt{\text{Hz}}$. This agrees well with the fitting of the individual CPMG curves and the $T_{2,CPMG}$ scaling in Fig. 4 of the main text. Using the susceptibility of the qubit resonance frequency to a voltage change of a nearby gate and the energy lever arm of that gate we can compare the noise value B to charge noise. With this conversion we obtain $B = 29 \pm 27$ μeV$/\sqrt{\text{Hz}}$. **b,** Following [4], we now use the filter function as described in **a** to estimate the noise decay and the noise level at 1 Hz that gives the given $T_{2,CPMG}$ for the number of π-pulses and fit this to our data. We obtain $\gamma = 1.06 \pm 0.13$ and $B = 30 \pm 18$ μeV$/\sqrt{\text{Hz}}$. This is comparable to the results obtained in **a**.



SUPPLEMENTARY FIG. 17. **Rabi oscillations for qubit 2. a-d,** Rabi oscillation of qubit 2 measured for different output powers of the microwave source. **e,** The extracted Rabi frequency is plotted versus the square root of the applied power, showing the expected linear dependence.

TABLE I. **Qubit metrics for single qubits in silicon.** The results obtained in this study compared to qubit poerformance in silicon of recent works. Data are either extracted from the publications directly, or by analysing the figures published in the work. The table respectively lists T_1 with the relevant magnetic field, T_2^* with the relevant integration time, $T_{2,Hahn}$, $T_{2,CPMG}$, the time it takes to do a π-rotation (T_π) and the single-qubit gate fidelity.

Paper		T_1 (B-field) [ms]	T_2^* [us] (int time)	$T_{2,\mathrm{Hahn}}$ [us]	$T_{2,\mathrm{CPMG}}$ (π) [us]	Tπ[us]	$F_{1Q_{\mathrm{gate}}}$ [%]	Substrate	Drive
Zwerver et al. (2021)	Q1	1600 (1)	24(100s)	292	3700 (50)	0.9	99.0	^{28}SiMOS	ESR
	Q2	-	–	140	1200 (20)	-	99.1	^{28}SiMOS	ESR
Veldhorst et al. (2014) [8, 9]	Q1	–	120	1200	28000 (500)	1.6	99.6	^{28}SiMOS	ESR
Chan et al. (2020) [9]	Q2	–	61	–	–	–	–	^{28}SiMOS	ESR
	Q3	–	30	–	–	–	–	^{28}SiMOS	ESR
Yang et al. (2019) [10]		$\sim$ 1000	33	400	6700 (122) [11]	-	99.9	^{28}SiMOS	ESR
Huang et al. (2019) [12]	Q1	-	24.3	290	-	1	99.3	^{28}SiMOS	ESR
	Q2		10.5	33.5	-	-	99.4	^{28}SiMOS	ESR
Yang et al. (2020) [13]	Q1	$\sim$ 500	12.3	200	-	$\sim$ 0.9	99.76	^{28}SiMOS	EDSR
Petit et al. (2020a) [14]	Q1	-	2.1	-	-	0.45	98.7	^{28}SiMOS	ESR
	Q2	-	2.7	-	-	0.45	99.3	^{28}SiMOS	ESR
Petit et al. (2020b) [15]	Q1	-	2.3	-	63 (15)	-	-	^{28}SiMOS	ESR
Measured above 1 K	Q2	-	2.9	-	44 (15)	-	-	^{28}SiMOS	ESR
Yang et al. (2013) [16]		2600 (1.25)	-	-	-	-	-	$^{\mathrm{Nat}}$SiMOS	-
Ciriano-Tejel et al. (2021) [17]	D1	280 (1)	-	-	-	-	-	^{28}SiMOS	-
	D2	9000 (1)	-	-	-	-	-	^{28}SiMOS	-
Petit et al. (2018) [18]		145	-	-	-	-	-	^{28}SiMOS	-
Maurand et al (2016) [19]		$>$ 0.175	0.06 (2s)	0.245	-	$\sim$ 0.01	-	$^{\mathrm{Nat}}$SiMOS	-
Xue et al. (2021) [20]	Q1	100.6 (0.43)	21.64	-	-	-	-	^{28}Si/SiGe	EDSR
	Q2	95.0 (0.43)	10.08	-	-	-	-	^{28}Si/SiGe	EDSR
Struck et al. (2020) [21]	Q1	–	21	-	128	-	-	^{28}Si/SiGe	EDSR
Yoneda et al. (2019) [7]		$>$ 100	20	99	3100 (2400)	0.12	99.9	^{28}Si/SiGe	EDSR
Sigillito et al. (2019) [22]	Q1	-	2.6	41	-	-	-	^{28}Si/SiGe	EDSR
	Q2	-	1.5	31	-	-	-	^{28}Si/SiGe	EDSR
	Q3	-	10.4	72	-	-	-	^{28}Si/SiGe	EDSR
	Q4	52	9.4	109	-	-	-	^{28}Si/SiGe	EDSR
Takeda et al. (2020) [23]	Q1	4.3	1.82	28.1	-	0.1	99.43	^{28}Si/SiGe	EDSR
	Q2	2.67	1.69	20.5	-	0.1	99.57	^{28}Si/SiGe	EDSR
	Q3	1.31	1.69	45.8	-	0.1	99.91	^{28}Si/SiGe	EDSR
Zajac et al. (2018) [24]	Q1	22	1.4	80	-	0.11	99.7	$^{\mathrm{Nat}}$Si/SiGe	EDSR
	Q2	-	1.2	22	-	$\sim$ 0.1	99.3	$^{\mathrm{Nat}}$Si/SiGe	EDSR
Watson et al. (2018) [25]	Q1	$>$ 50	1	19	-	0.25	99.3	$^{\mathrm{Nat}}$Si/SiGe	EDSR
	Q2	3.7	0.6	7	-	0.25	98.9	$^{\mathrm{Nat}}$Si/SiGe	EDSR
Kawakami et al. (2016) [6]		-	0.37	70	400	0.37	98.99	$^{\mathrm{Nat}}$Si/SiGe	EDSR
Borjans et al. (2018) [26]	D1, dot 1	65 (0.2)	-	-	-	-	-	$^{\mathrm{Nat}}$Si/SiGe	Micromagnet
	D1, dot 2	160 (0.2)	-	-	-	-	-	$^{\mathrm{Nat}}$Si/SiGe	Micromagnet
	D2, dot 2	5000 (0.4)	-	-	-	-	-	$^{\mathrm{Nat}}$Si/SiGe	-
	D2, dot 3	$\sim$ 500 (1)	-	-	-	-	-	$^{\mathrm{Nat}}$Si/SiGe	-
	D2, dot 5	$\sim$ 500 (1)	-	-	-	-	-	$^{\mathrm{Nat}}$Si/SiGe	-
	D2, dot 6	$\sim$ 2000 (1)	-	-	-	-	-	$^{\mathrm{Nat}}$Si/SiGe	-
Simmons et al. (2011) [27]		2800 (1.85)	-	-	-	-	-	$^{\mathrm{Nat}}$Si/SiGe	-
Hollmann et al. (2020) [28]		$\sim$ 1000 (1)	-	-	-	-	-	^{28}Si/SiGe	Nanomagnet

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