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Parallel in-memory wireless computing

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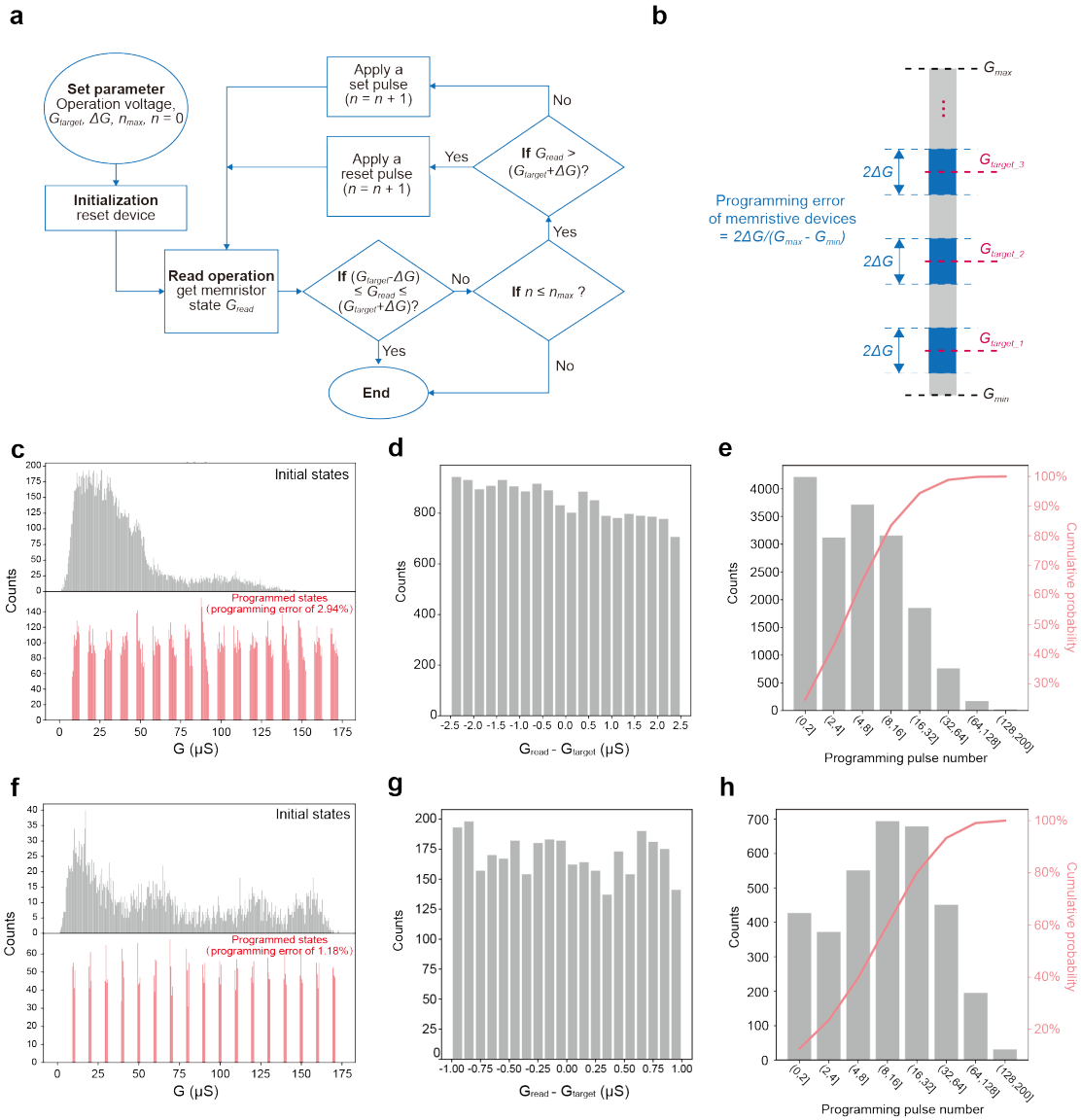
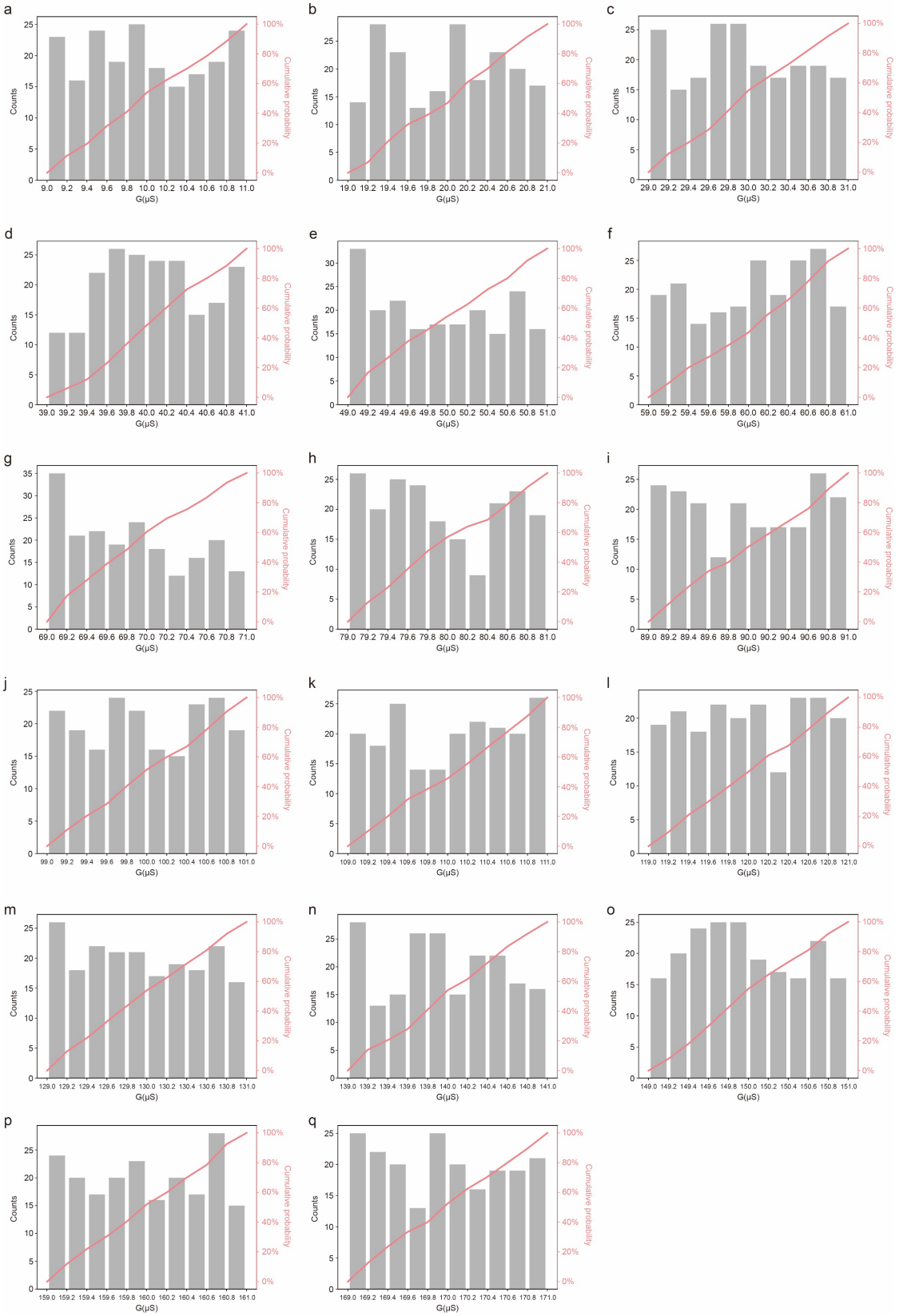
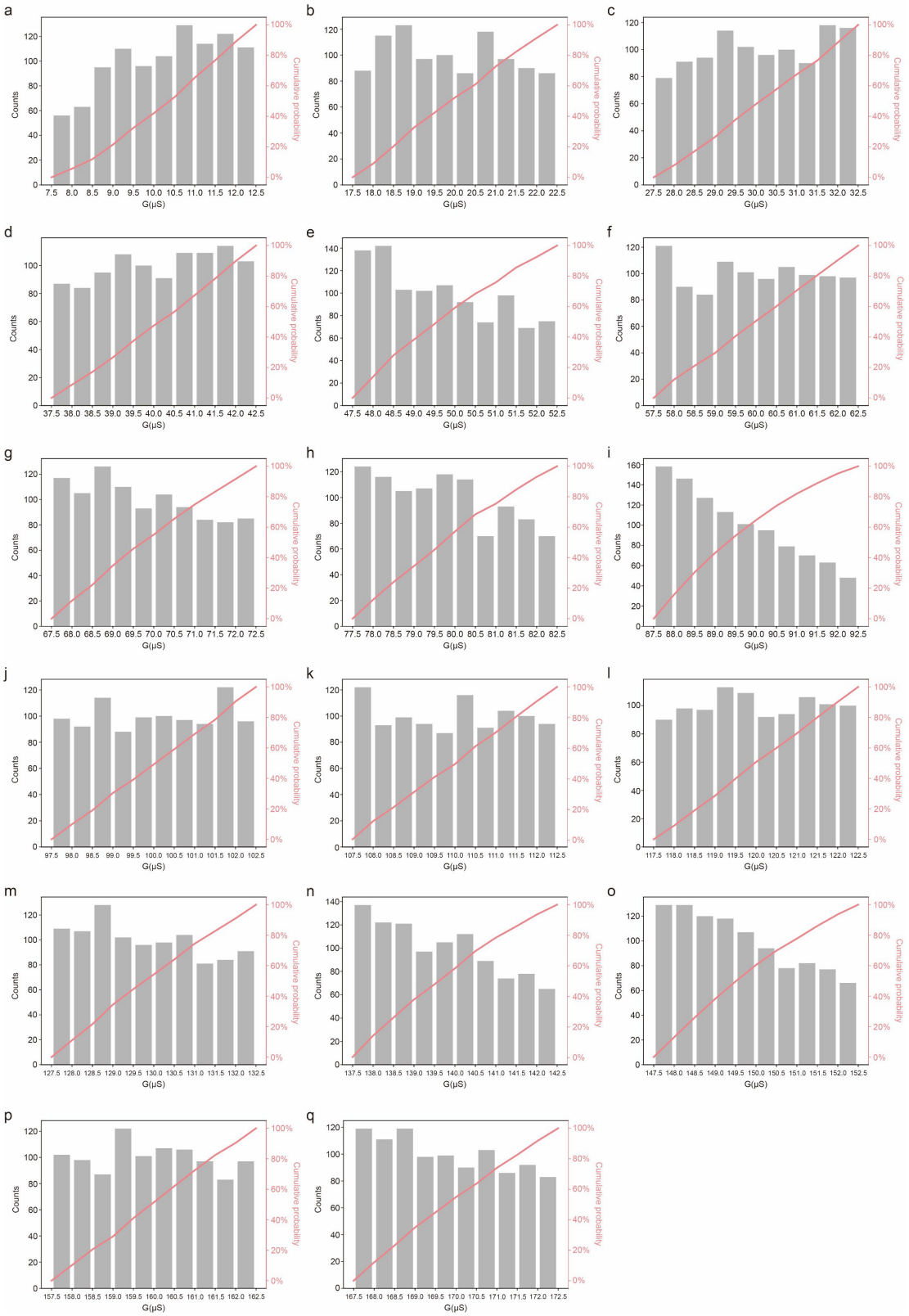


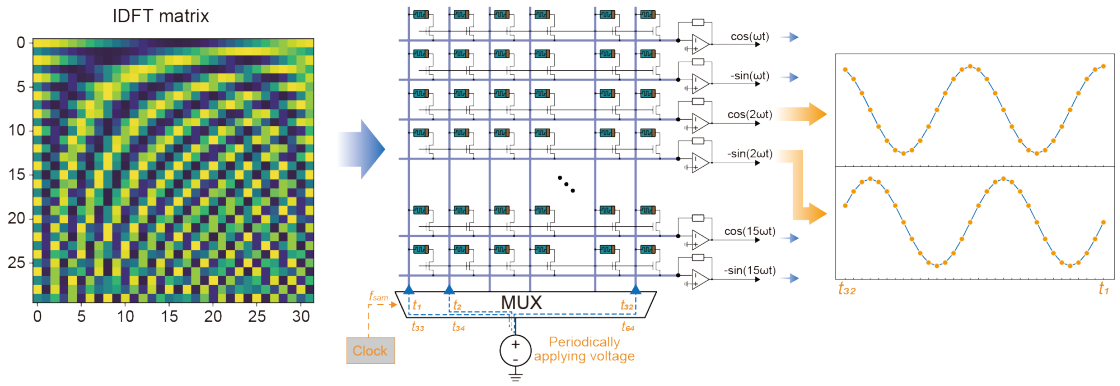
Supplementary Fig. 1 | Experimental results for programming conductance states of memristive devices. a, The flowchart of a closed-loop programming scheme, which was experimentally implemented with a LabVIEW program. **b,** The definition of the programming error, which is determined by $2\Delta G/(G_{max} - G_{min})$, where $2\Delta G$ represents the conductance variation; G_{max} and G_{min}, the maximum and minimum conductance values (175 and 5 μS for our devices) within a continuously tuned conductance range, respectively. **c,** Distributions of the conductance values before and after programming (with programming error of 2.94%), respectively. **d**, The deviations of programmed conductance values are uniformly distributed within the defined range (from -2.5 to 2.5 μS). **e**, The distribution of pulse number during programming operation (with programming error of 2.94%), which requires 10.08 pulses on average. **f,** Distributions of the conductance values before and after programming (with programming error of 1.18%), respectively. **g**, The deviations of programmed conductance values are uniformly distributed within the defined range (from -1 to 1 μS). **h**, The distribution of pulse number during programming operation (with programming error of 1.18%), which requires 21.06 pulses on average.



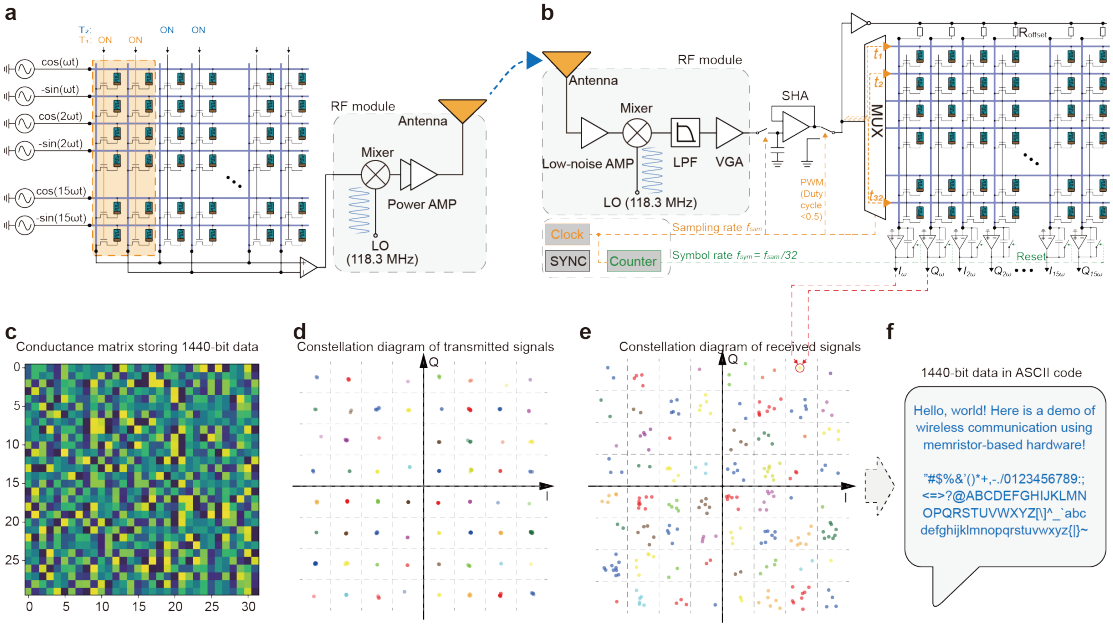
Supplementary Fig. 2 | Distributions of the conductance values after programming the memristive devices (with the programming error of 1.18%). a-q, The statistics histogram and cumulative probability of conductance values programmed with 17 differentiated levels. And the ΔG was set to 1 μS in the experiment.



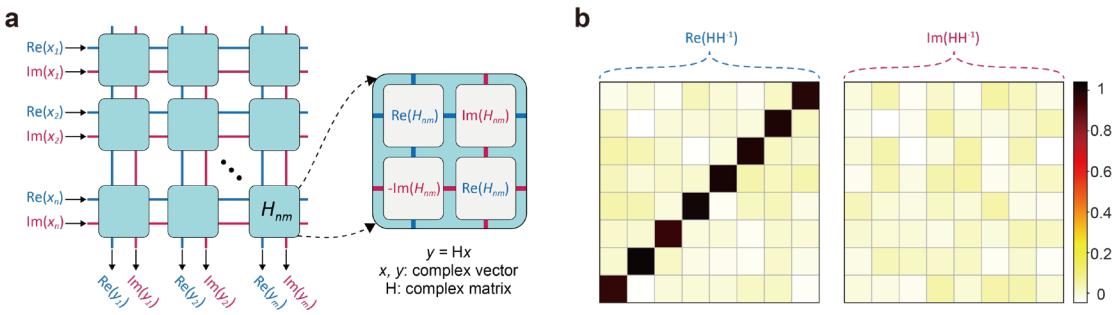
Supplementary Fig. 3 | Distributions of the conductance values after programming the memristive devices (with the programming error of 2.94%). a-q, The statistics histogram and cumulative probability of conductance values programmed with 17 differentiated levels. And the ΔG was set to 2.5 μS in the experiment.



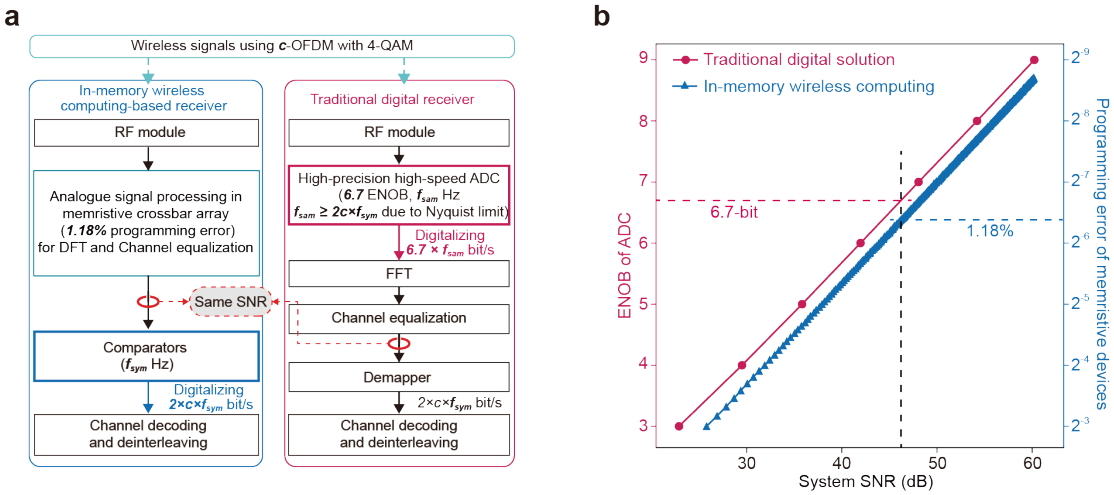
Supplementary Fig. 4 | Schematic of the memristor-based orthogonal sub-carrier generator. An IDFT matrix (left panel) is mapped onto the memristor crossbar array (middle panel). By periodically applying voltage on each input line of the crossbar array, orthogonal sub-carrier signals can be simultaneously generated from the different output lines (as shown in the right panel) of the memristive crossbar array.



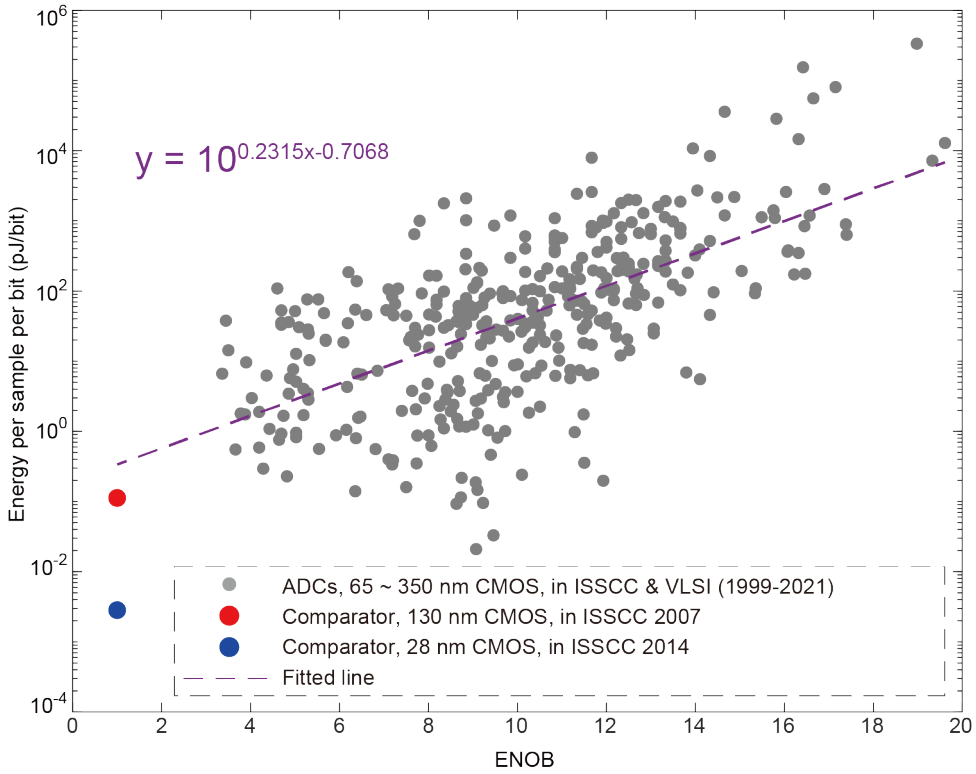
Supplementary Fig. 5 | Experimental implementation of the memristive device based wireless transmission using 64-QAM. a, The circuit schematic of the wireless transmitter based on the memristive crossbar array. LO, local oscillating frequency. AMP, amplifier. **b,** The circuit schematic of the memristive device based wireless receiver. LPF, low-pass filter. VGA, variable gain amplifier. SHA, sample-and-hold amplifier. **c,** The measured conductance matrix of memristive crossbar array shown in a, which is used to store 1440-bit data to be transmitted. **d,** The measured constellation diagram of all transmitted signals. **e,** The measured constellation diagram of all received signals. **f,** The 1440-bit data in ASCII code, indicating that the extracted message from received signals is the same as the original message.



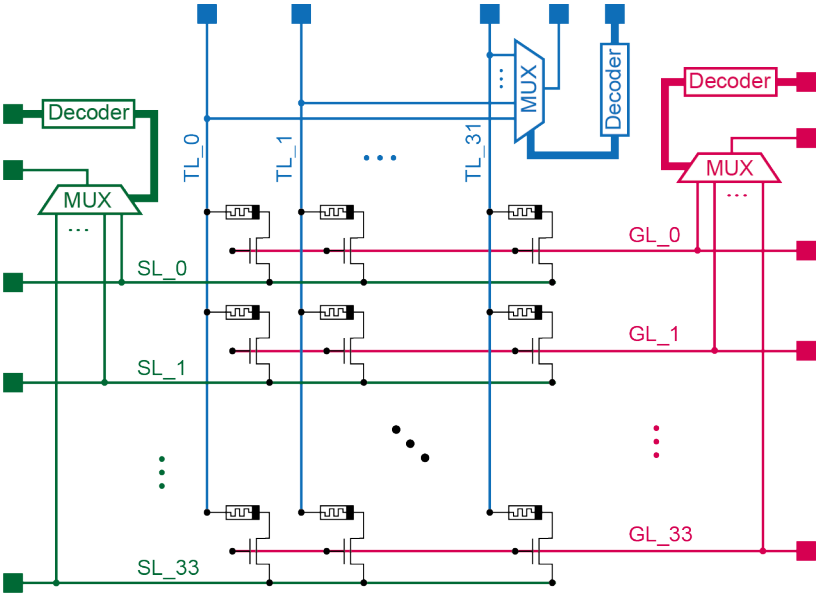
Supplementary Fig. 6 | Experimental implementation of parallel complex-valued matrix-vector multiplication. a, The complex-valued input and output are represented by a pair of voltages and currents, respectively, and complex-valued matrix can be represented by combination of memristors. **b,** Demonstration of the complex-valued MVM operation. In the experiment, a memristor-based complex-valued matrix H was multiplicated by eight voltage vectors, which can compose the inversed matrix of H. The output current vectors approximatively compose an identity matrix.



Supplementary Fig. 7 | Comparison between in-memory wireless computing-based receiver and traditional digital receiver. a, The flow chart of signal processing procedures with two solutions. In our scheme, the signal processing is realized by the memristive crossbar array and the digitalization process is shifted backwards after the signal processing. By contrast, the analogue signal is digitalized with HPHS ADC in traditional digital receiver and the resulting digital signal is processed with the digital signal processors. **b,** The systematic SNR from quantization noise of the ADC (magenta line) used in traditional solution and the programming error of the memristive crossbar array, respectively. The SNR (defined as ratio of signal power to the noise power) of in-memory wireless computing is estimated by modelling the memristive crossbar array with a given conductance states variability. Programming error of 1.18% corresponds to a SNR same as that of the ADC used in the digital receiver (6.7 ENOB).



Supplementary Fig. 8 | Exponential increase of the energy per sample per bit with ENOB of ADCs. This data collection[1] shows the published ADC designs using 65 nm ~ 350 nm CMOS in ISSCC and VLSI from 1999 to 2021, and two dynamic comparator designs[2,3] are also added into the figure. ENOB, the effective number of bits. The ENOB of comparators is equal to one. The energy consumption per sample step per bit is calculated by P/f_{snyq}/ENOB, in which P is the ADC power, and f_{snyq} is the Nyquist sampling rate of ADC. The result shows that the energy consumption per sample per bit increases exponentially with the ENOB of ADCs. The fitted equation is $y = 10^{0.2315x - 0.7068}$.



Supplementary Fig. 9 | Schematic of the 1T1R chip. On-chip multiplexers, decoders, transistor array and metal interconnections were fabricated in a standard CMOS foundry. The fabrication of memristive devices was completed in the laboratory.

References

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