Chapter 1.

Introduction and Overview

1.1. Motivation

Enabled by the ongoing advances in microelectronic technology and signal processing theory, increasingly complex communication solutions begin to emerge at an accelerated pace. With the wireless spectrum being such a scarce resource, scientists have always strived to achieve the highest possible data rates within a designated bandwidth, their stated goal being to reach the Shannon channel capacity limit. Engineers, however, are more often not that much interested in achieving the best possible performance, but rather the best trade-off between performance and cost. Such optimization is particularly crucial for consumer applications, which are driving the semiconductor market nowadays.

Figure 1.1 shows the classical structure of a communication chain, consisting of a transmitter and a receiver connected through a generic channel. In this thesis we consider only wireless radio channels. Like their wired counterparts, wireless channels also suffer from multipath effects, whereby multiple reflections of the original signal appear at the receiver with different delays and amplitudes.

Unlike wired channels, however, these delays and amplitudes are time variant due to the Doppler effect. Its cause is the movement of the receiver in the case of land-mobile channels or of the ionospheric layers in the case of HF short-wave channels. The channel properties impact the overall performance dramatically, therefore having a standardized and accurate channel simulator is essential for measuring the performance of a communication system consistently. It is one of the goals of this thesis to develop an efficient and highly flexible time-variant

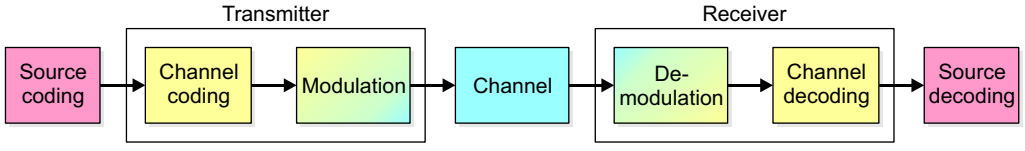

Figure 1.1.: Transmitter and receiver side of a communication chain

multipath channel simulator suitable for both hardware and software implementation.

In order to combat the effect of multipath reflections, various types of modulations have been proposed. Chronologically, single-carrier modulation schemes have been the first to be introduced for digital communications. As the multipath trail usually spans multiple symbols, the equalization can become very complex, especially for time-variant channels, where adaptive equalizers have to be used. Besides their inherent complexity, these have a negative feedback loop, which limits the maximum Doppler frequency that can be tracked.

A newer solution is the orthogonal frequency division multiplexing (OFDM), which is a multi-carrier modulation scheme. After years of slow progress since its introduction in 1971 [95], OFDM has finally become a mature technology [3] adopted by various international standards for wireless networks, such as IEEE 802.11a [38] and IEEE 802.16a [39], and digital broadcasting, like DAB [19], DVB-T [20] and DRM [21]. Experiments carried out by various researchers showed that with a well-designed receiver, the two modulations offer comparable performance. Nevertheless, the essential advantage of OFDM is that the channel equalizer has a much lower complexity for the same performance, thus allowing for lower-cost receivers.

The present doctoral thesis deals with the efficient design of digital OFDM receivers for wireless communications, for both fixed and mobile applications, with emphasis on digital broadcasting. As mobility and portability are playing an increasingly important role, this poses two additional constraints to digital receivers. On the one hand, mobility requires that the receiver can cope with the fast Doppler variations that occur at higher receiver velocities. On the other hand, portability requires that power consumption be minimized in order to save battery life. Thus, the main issues to be addressed from a designer's point of view are the performance vs. cost trade-off and power consumption minimization, all this while ensuring a predictable design time.

1.2. Research Scope

In our research we focus on various aspects of the design of digital OFDM receivers. Such a receiver, shown in **Figure 1.2**, consists of two distinct parts: an OFDM demodulator and a channel decoder. Whether the downconversion is performed in the analog or digital domain is irrelevant for our study. Of the two blocks, only the demodulator is OFDM specific. The channel decoder is independent of the modulation scheme and thus can be treated separately. In this thesis, we consider only convolutional coding with QAM mapping and interleaving, e.g. as employed by the DVB-T standard, with the channel decoding being performed non-iteratively using the Viterbi algorithm.

The scope of the present thesis includes the architectural exploration and optimization of several blocks of an OFDM receiver at the algorithmic and structural level: OFDM demodulator (Fast Fourier Transform), channel equalizer, QAM demapper, and Viterbi decoder, with emphasis

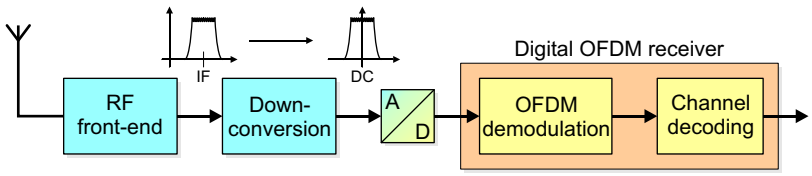

Figure 1.2.: Digital OFDM receiver

on **digital broadcasting receivers**. The channel equalizer and the Viterbi decoder are given preeminence and are treated in a separate chapter each.

Another important contribution of the present research is the hardware modeling of time-variant multipath channels, to which an entire chapter has been dedicated. The main result is a scalable **channel simulator** architecture that can be implemented very efficiently in both HW and SW. Especially innovative are the solutions proposed for **Gaussian noise generation** and **polyphase interpolation**, which are particularly efficient for HW implementation. A software implementation of this simulator has been used for measuring the performance of the entire receiver and especially that of the channel equalizer.

The **channel equalizer** is the block which affect the performance of an OFDM receiver the most and is also the most challenging to design, especially when the receiver operates in an environment with high Doppler spreads. The essential question is how high the performance of the equalizer should be so that the overall performance of the receiver is not impaired. We will show that increasing estimation performance beyond a certain threshold is no longer accompanied by an improvement of the receiver performance. It is one of the goals of this research to prove that this threshold performance can be achieved with relatively few computational resources, so that more complex solutions proposed in the literature are not justified from a practical implementation perspective. Moreover, the thesis proposes a low-area scalable channel estimation architecture together with the design of the optimal coefficients for various practical scenarios.

Further on, the thesis introduces two architectural solutions for the **Viterbi decoder**. The first solution is a high-throughput state-parallel architecture with dynamically adjustable trace-back depth. Depending on the performance requirements and the selected puncturing pattern, the depth can be adjusted by switching off the unused stages, which significantly reduces the power consumption. The second solution is a lower-throughput state-serial architecture which focuses on achieving the smallest area possible and thus the lowest implementation cost. Both architectures are presented with implementation results.

A low-area sequential solution is also proposed for the **Fast Fourier Transform**, with implementation results for FPGA. The reason we focused on low-area architectures is that they offer enough bandwidth for implementing most of the current standards at the lowest silicon cost. This fact has been proven by a comparative analysis of various FFT architectures. In addition, one pipelined architecture has been implemented alongside the sequential one. The

difference in area is significant, especially for large block sizes. In the context of simulation and implementation of OFDM receivers, we also present an approach for **SystemC functional modeling** of such systems, considering a IEEE 802.11a WLAN receiver as a case study .

It must be emphasized that the focus of this thesis is not the development of new algorithms for communications, but rather the selection, optimization, and architectural modeling of the most suitable solutions for an efficient low-area and low-power hardware realization.

1.3. Thesis Outline

Chapter 2 begins with a characterization of the mobile radio channels, with emphasis on their delay profiles and Doppler spreads, which result in frequency selectivity and time variance. The discretized wide-sense stationary with uncorrelated scattering (WSSUS) channel model presented here will subsequently be used throughout this thesis. We also enumerate the main delay profiles and Doppler power spectra introduced in the literature, which we use for our model. We then go on to introduce the principles of OFDM and discuss the influence of the multi-path wireless channel on OFDM reception, for both slow and fast fading. It is shown that these Doppler variations are the main performance limiting factor since they cause inter-carrier interferences (ICI), which cannot be corrected in the receiver. Moreover, we discuss how other channel and receiver impairments affect the OFDM reception.

Chapter 3 presents the specifics of OFDM for digital broadcasting, together with typical structures for the transmitter and receiver. Special attention is given to presenting the stream structure and the scattered reference pilots, as they are essential for understanding the channel estimation for broadcasting receivers. In this chapter we also present the QAM modulation as encountered in various standards and the corresponding demapping algorithm used in the remainder of this thesis, which uses the channel state information (CSI) from the channel estimator.

Chapter 4 proposes an efficient and scalable channel simulation architecture for WSSUS discrete baseband channels. The channel is modeled as a FIR filter with time-variant taps, the challenge being how to generate these taps with the desired statistics. We take the Gaussian noise filtering approach and propose hardware-efficient architectures for the three building blocks of such a generator: Gaussian noise generation, Doppler spectrum shaping, and interpolation with large factors. Area-efficient architectures are proposed for all these three blocks. Especially innovative are the architectures for Gaussian noise generation, based on the central limit theorem, and polyphase interpolation, which uses a phase accumulator and a variable delay element. Although optimized for low-area HW implementations, the proposed channel simulator has also been efficiently implemented in software and used for Matlab simulations throughout this thesis.

Chapter 5 deals with channel estimation for broadcasting receivers. It begins with a review of

previous contributions found in the literature, showing that most of them propose architectures which are unnecessarily complex. This claim is supported by an analysis of the performance required from a channel estimator so that it does not impair the overall performance of the receiver. The analysis is performed by simulating a complete DVB-T receiver chain with a realistic multi-path time-varying channel model. We thereafter show that the required performance can be easily achieved using our proposed architecture, provided that the estimator coefficients are carefully designed. The two essential advantages of the architecture are its efficiency in terms of multiplications per estimated sample and its scalability for various pilot patterns and OFDM symbol sizes.

Chapter 6 provides a background about the Viterbi algorithm for decoding convolutional codes and proposes two decoder architectures. The first one is a high-throughput state-parallel architecture with adjustable trace-back window length. Selecting the smallest necessary window length that does not degrade the performance allows for dynamic power consumption minimization. The second one is a lower-throughput state-serial architecture which focuses on achieving the lowest possible area and is also very suitable for FPGA implementation. These solutions are presented with synthesis results for ASIC and FPGA respectively.

Chapter 7 focuses on the modeling, simulation and design of OFDM receivers. As a case study for showing our modeling approach we considered the IEEE 802.11a wireless LAN standard. The simulation is confined to the algorithmic level, using untimed dataflow models. Inter-module communication refinement and high-level synthesis are outside the scope of the present thesis. As a case study for OFDM receiver design we chose the FFT, as it is the most computationally intensive and consumes the most area of all building blocks of an OFDM receiver. We compare and implement two different architectures, one pipelined and one sequential, and show that the sequential one has the smallest area, while ensuring sufficient performance for implementing all OFDM standards for broadcasting. FPGA synthesis results are provided for both architectures.