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Fast-scale bifurcation in single-stage PFC power supplies operating with DCM boost stage and CCM forward stage

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SUMMARY

This paper describes the fast-scale bifurcation phenomena of a single-stage single-switch power-factor-correction (PFC) regulator comprising a boost stage operating in discontinuous conduction mode (DCM) and a forward stage operating in continuous conduction mode (CCM). The two stages combine into a single stage by sharing one main switch and one control loop. Using 'exact' cycle-by-cycle computer simulations, the effects of various circuit parameters on fast-scale instabilities are studied. The results are qualitatively verified by experimental measurements. This work provides a clear picture of how the variation of certain practical parameters can render such a circuit fast-scale unstable. Copyright © 2006 John Wiley & Sons, Ltd.

KEY WORDS: dc–dc converter; power factor correction; single-stage converter; fast-scale instability; bifurcation

1. INTRODUCTION

The single-stage isolated power-factor-correction power supply (SSIPP) proposed by Redl *et al.* [1] is a cost-effective design solution for power supplies that are required to provide a high power factor and a well-regulated dc output voltage. The circuit typically takes the form of a cascade combination of a discontinuous conduction mode (DCM) boost converter and a dc–dc converter. Automatic power factor correction (PFC) is provided by virtue of the DCM operation of the boost stage. The dc–dc converter stage, operating in either mode, provides a regulated output voltage via a voltage feedback loop. Operating the dc–dc converter stage in DCM at constant frequency enjoys constant voltage stress of the storage capacitor irrespective of the magnitude of the output load [1, 2], but is generally

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less efficient due to higher current stress on the active switch. On the other hand, operating the dc–dc converter in continuous conduction mode (CCM), at the expense of a larger inductor, is usually more efficient and the current stress is lower. Furthermore, it allows the use of frequency modulation to eliminate harmonic distortion of the PFC converter because the CCM converter is insensitive to frequency variation [3]. Due to its practical versatility for low-to-medium output power applications, this circuit has received a great deal of attention in the past decade [3–5]. However, previous studies have mainly focused on the steady-state design and control aspects of this circuit, and the detailed dynamical behaviour and the stability boundaries have not been thoroughly pursued.

Recently, studies of the dynamical behaviour of switching power converter circuits have revealed the possibilities of various kinds of bifurcation behaviour, e.g. in pulse-width-modulated (PWM) dc–dc converters [6–11], current-mode controlled dc–dc converters [12–14], thyristor and diode circuits [15, 16], free-running dc–dc converters [17], parallel-connected dc–dc converters [18, 19], general switching circuits [20, 21], etc. For the boost PFC preregulators operating in CCM, it has been found that both fast-scale and slow-scale instabilities are possible [22–24]. However, similar problems in the DCM counterparts are known by practitioners but are not systematically explained and studied. Clearly, the slow-scale instability problem may worsen the harmonic distortion of the input current, whereas the fast-scale instability problem may impose higher current stresses on the switching devices. It has been observed that the peak current can increase by 10–20% when fast-scale instabilities occur in some intervals of the mains cycle [23, 24]. Thus, the study of such instability problems has a practical motivation. See also References [25, 26] for some surveys of the recent research in this area.

In this paper, we report fast-scale period-doubling bifurcation observed in the complete single-stage PFC power supply, in which the particular PFC regulator and the forward output regulator are designed to operate in DCM and CCM, respectively. Our focus is on the effects of variation of a few chosen system parameters. In this paper, we will show that, with improper choice of system parameters, the converter can suffer from fast-scale instability for some intervals of time during the line cycle. Computer simulations based upon exact cycle-by-cycle system equations, as well as experimental measurements, are presented in this paper. The extents to which fast-scale instability may occur are quantitatively measured and the parameters that affect fast-scale instability are identified. This study provides clear directions for identifying the cause of fast-scale instability in a single-stage PFC power supply.

2. SYSTEM DESCRIPTION

The single-stage isolated PFC converter under study is shown in its original form in Figure 1 [1]. It can be modelled as a cascade connection of a boost converter and a buck converter, which are *driven synchronously* under one switching pulse-width-modulation (PWM) signal, as shown in Figure 2 [27]. The control uses a simple PWM scheme, in which a control voltage v_{con} is compared with a sawtooth signal to generate a PWM signal to drive the switches. The sawtooth signal is given by

$$V_{\text{ramp}} = V_{\text{L}} + (V_{\text{U}} - V_{\text{L}})\frac{t \bmod T}{T} \tag{1}$$

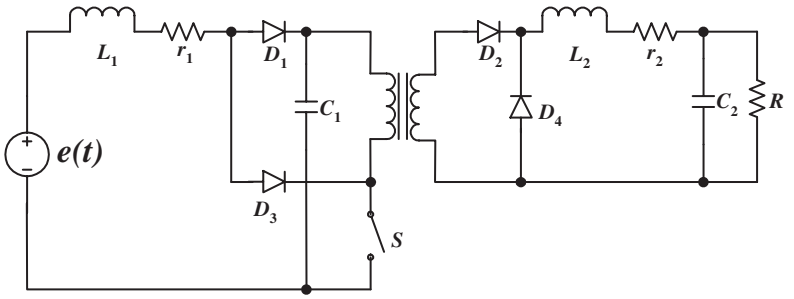

Figure 1. The single-stage isolated PFC power supply (SSIPP) [1].

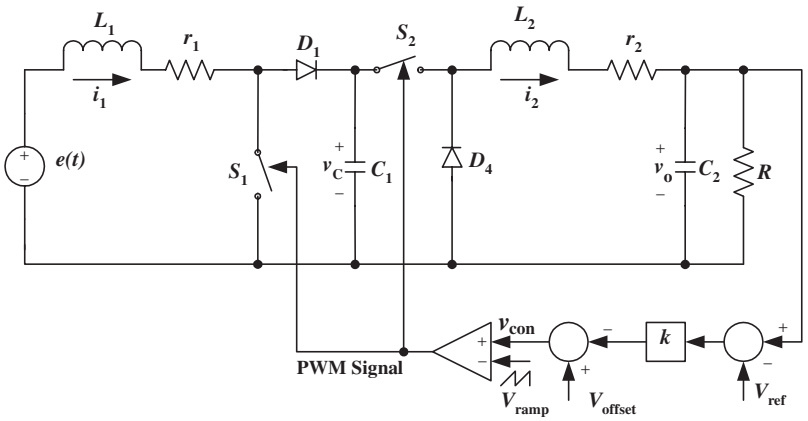

Figure 2. Equivalent circuit model of the single-stage PFC power supply.

where V_L and V_U are the lower and upper voltage limits of V_{ramp}, and T is the switching period. The PWM signal is 'high' when $v_{con} > V_{ramp}$, and is 'low' otherwise. The control voltage v_{con} is derived from a voltage feedback loop, i.e.

$$v_{con} = V_{offset} - k(v_o - V_{ref}) \tag{2}$$

where V_{offset} is a dc voltage that gives the steady-state duty cycle , V_{ref} is the reference output voltage, and k is the feedback gain.

When the boost stage is working in DCM and the buck stage is working in CCM, three switch states are possible during a switching cycle:

State A: S_1 and S_2 are on, D_1 and D_2 are off;
State B: S_1 and S_2 are off, D_1 and D_2 are on;
State C: S_1 and S_2 are off, D_1 is off and D_2 is on.

Moreover, during the off-time of D_1, the circuit state is constrained to lie in the space defined by the zero value of current i_1. Thus, i_1 can be ignored for State C. Then, according

to the circuit topology in each state, we can write the state equations as follows:

$$\begin{aligned} \dot{x} &= A_1 x + Be(t) \quad \text{for State A} \\ \dot{x} &= A_2 x + Be(t) \quad \text{for State B} \\ \dot{y} &= A_3 y \qquad\quad \text{for State C} \end{aligned} \tag{3}$$

where $e(t) = \hat{E}|\sin(\omega t)|$ is the input voltage and $\hat{E}$ is the amplitude of the input voltage, the state vectors are defined as $x = [i_1 \ v_C \ i_2 \ v_o]^T$ and $y = [v_C \ i_2 \ v_o]^T$. The system matrices for this converter are

$$A_1 = \begin{bmatrix} -\frac{r_1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_1} & 0 \\ 0 & \frac{1}{L_2} & -\frac{r_2}{L_2} & -\frac{1}{L_2} \\ 0 & 0 & \frac{1}{C_2} & -d\frac{1}{C_2 R} \end{bmatrix} \tag{4}$$

$$A_2 = \begin{bmatrix} -\frac{r_1}{L_1} & -\frac{1}{L_1} & 0 & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & -\frac{r_2}{L_2} & -\frac{1}{L_2} \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{C_2 R} \end{bmatrix} \tag{5}$$

$$A_3 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & -\frac{r_2}{L_2} & -\frac{1}{L_2} \\ 0 & \frac{1}{C_2} & -\frac{1}{C_2 R} \end{bmatrix} \tag{6}$$

$$B = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{7}$$

where all component symbols are as defined in the circuit diagram shown in Figure 2.

3. COMPUTER SIMULATION STUDY

In this section, we begin with a series of computer simulations to identify possible bifurcation phenomena. Our simulation is based on the state equations derived in the foregoing section. Essentially, for each set of parameter values, time-domain cycle-by-cycle waveforms are generated by solving the appropriate linear equation in a subinterval of time, according to different switching states. After the transient period, we capture the steady-state time-domain waveforms. The circuit component values used are listed in Table I. Note that, having made no simplifying assumptions in the simulating model, the results from such cycle-by-cycle simulations are considered viable and can adequately reflect the salient dynamical behaviour of the system.

For a certain range of parameters, fast-scale instability may occur within a line cycle. Such instability manifests itself as a period-doubling bifurcation at the switching frequency.

We generally observe that fast-scale instability occurs near the two ends of a half-line cycle, as shown in Figure 3 for different values of the feedback gain k for $C_1 = 100\,\mu\text{F}$

Table I. Component values used in simulations.

Circuit components	Values
Switching period T	50 μs
Input voltage $e(t)$	110 V rms, 50 Hz
Reference output voltage V_{ref}	20–160 V
Inductance L_1, ESR r_1	200 μH, 0.01 Ω
Inductance L_2, ESR r_2	2 mH, 0.01 Ω
Load resistance R	30 Ω
Capacitance C_1	10–200 μF
Capacitance C_2	10 μF (high output voltage due to absence of transformer isolation)

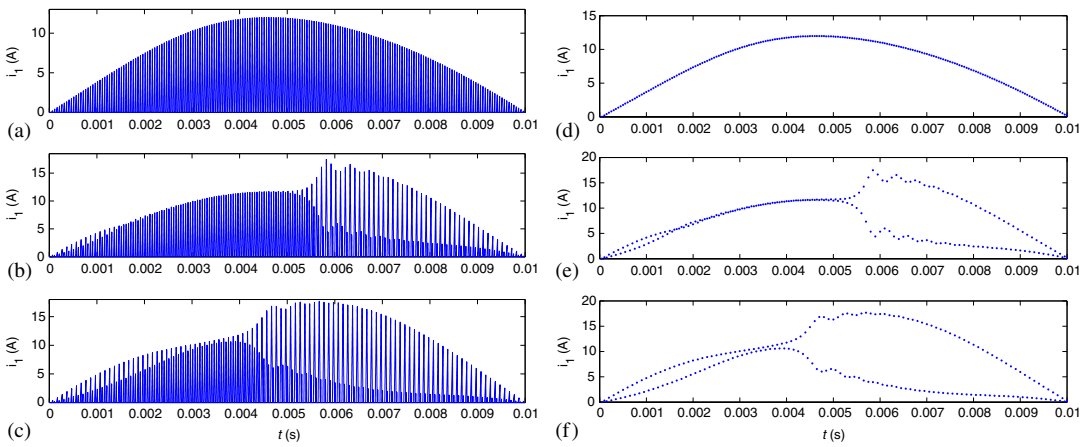

Figure 3. (a)–(c) Time-domain waveforms; and (d)–(f) sampled-data waveforms of i_1 for $C_1 = 100\,\mu\text{F}$ and $V_{\text{ref}} = 90\,\text{V}$.

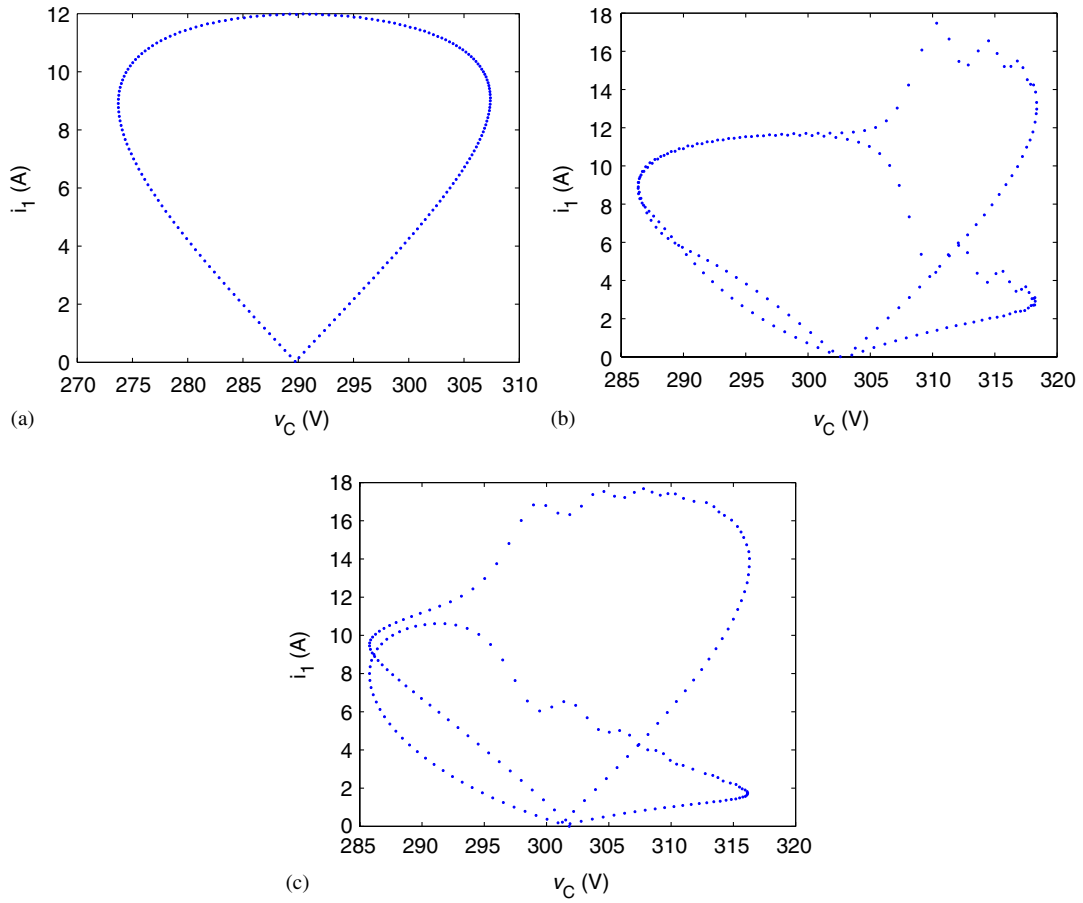

Figure 4. Phase portraits of sampled i_1 versus v_C for $C_1 = 100\,\mu\text{F}$ and $V_{\text{ref}} = 90\,\text{V}$.

and $V_{\text{ref}} = 90\,\text{V}$. Figure 3(a) shows the stable operation with $k = 0.17$. Figure 3(b) shows bifurcation in some intervals of the line cycle with $k = 0.185$. Figure 3(c) shows fast-scale instability in the whole line cycle with $k = 0.188$. Specifically, period doubling at the switching period occurs at some phase angle of the line cycle and instability grows towards the zero-crossings of the line cycle. In order to observe the change in dynamical behaviour clearly, we collect the sampled peak values for i_1 and i_2 during each switching period in the steady state, and the corresponding sampled values for v_C and v_o. Figures 3(d)–(f) show the corresponding sampled-data waveforms of Figures 3(a)–(c). Period-doubling bifurcations are clearly observed. Figure 4 shows the corresponding phase portraits of the sampled input current i_1 and voltage v_C.

Of engineering importance is the existence (and location) of the critical bifurcation points along the line cycle as it affects the peak current value of the input current and hence the current stress on the switch. We denote the two critical points in terms of phase angle $\theta_{c1} = \omega t_1$

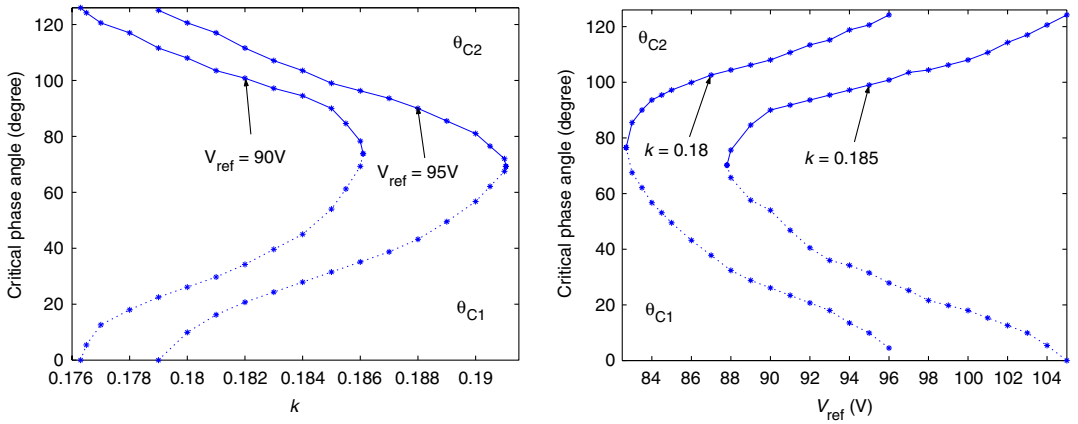

Figure 5. Left: critical phase angles in line cycle versus feedback gain k; right: critical phase angles in line cycle versus V_{ref}, both for $C_1 = 100\,\mu\text{F}$. θ_{c1} and θ_{c2} are the critical phase angles at which period-doubling bifurcation begins to occur. Fast-scale stable regions correspond to $\theta_{c1} < \theta < \theta_{c2}$.

and $\theta_{c2} = \omega t_2$, where ω is the line angular frequency. As we observe in the simulations, the converter fails to maintain the expected stability operation in intervals corresponding to $\theta < \theta_{c1}$ and $\theta > \theta_{c2}$.

3.1. *Effects of varying feedback gain and reference output voltage*

Figure 5 plots the two critical phase angles θ_{c1} and θ_{c2} as functions of the feedback gain k and V_{ref}. We can obtain from the simulation results that the width of the stable region $[\theta_{c1}, \theta_{c2}]$ decreases as k increases while it increases as V_{ref} increases.

Furthermore, for a certain reference output voltage V_{ref}, there is a critical value of feedback gain k_c, above which the operation has regions of fast-scale instability. Likewise, for a given feedback gain k, there is a critical reference output voltage V_{ref_c}, below which the operation has regions of fast-scale instability. Consequently, these critical parameter values define a stability boundary dividing the parameter space of the feedback gain and the reference output voltage, as shown in Figure 6. In brief, *fast-scale instability develops as the feedback gain increases*; *and likewise as the output voltage level decreases.*

3.2. *Effects of varying input voltage*

Figure 7 plots the two critical phase angles θ_{c1} and θ_{c2} as functions of the rms value E of input voltage $e(t)$ for $C_1 = 100\,\mu\text{F}$ and $k = 0.18$. As can be seen from the results, the width of the stable region decreases as E increases. Furthermore, when E reaches a certain value, the system operates in full-bifurcation and the stable interval is replaced completely by period-doublings and chaos. Thus, we observe that *fast-scale instability develops as the input voltage increases.*

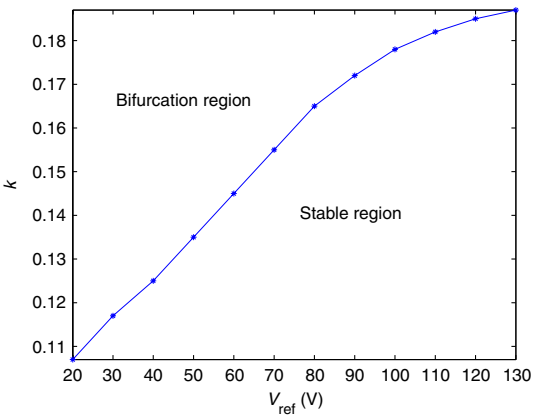

Figure 6. Stability boundary in the parameter space of feedback gain versus output reference voltage for $C_1 = 100\,\mu\text{F}$.

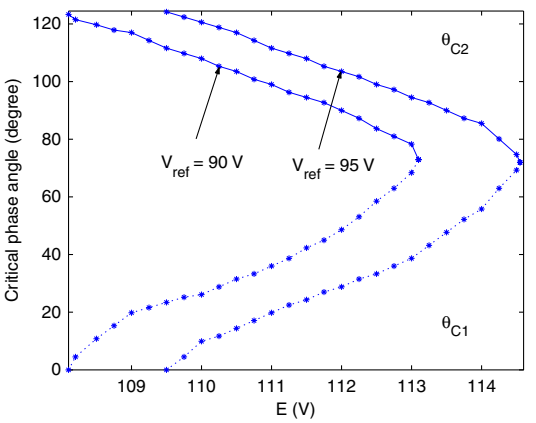

Figure 7. Critical phase angles in line cycle versus rms value E of input voltage for $C_1 = 100\,\mu\text{F}$ and $k = 0.18$. Fast-scale stable regions correspond to $\theta_{c1} < \theta < \theta_{c2}$.

3.3. Effects of varying load resistance

Figure 8 plots the two critical phase angles θ_{c1} and θ_{c2} as functions of load resistance R for $C_1 = 100\,\mu\text{F}$ and $V_{\text{ref}} = 90\,\text{V}$. The width of the stable region decreases as R increases. In other words, *fast-scale instability generally occurs and deteriorates as output power decreases.*

Furthermore, when the system is under normal operation (for a relatively smaller k), for a given reference output voltage V_{ref}, if we increase the load resistance R, the operation mode of the single-stage PFC converter will change. That is, for smaller R, the converter operates in DCM-CCM, when R reaches a certain value, the converter operates in DCM-DCM. Figure 9

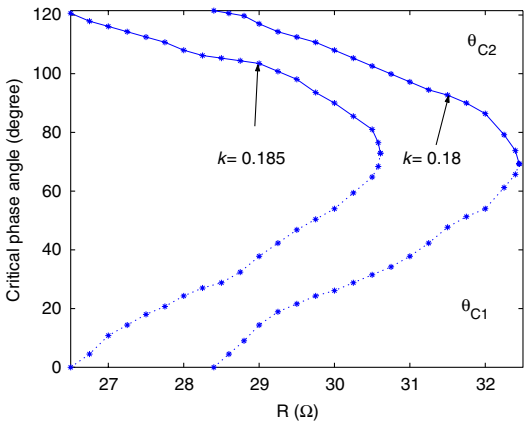

Figure 8. Critical phase angles in line cycle versus load resistance R, both for $C_1 = 100\,\mu\text{F}$ and $V_{\text{ref}} = 90\,\text{V}$. Fast-scale stable regions correspond to $\theta_{c1} < \theta < \theta_{c2}$.

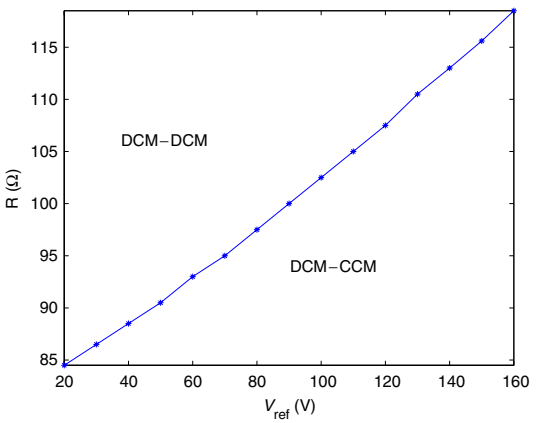

Figure 9. The stability boundary in the parameter space of load R and output reference voltage V_{ref} for different switching modes, with $C_1 = 100\,\mu\text{F}$ and $k = 0.01$.

shows the boundary in the parameter space of load R and output reference voltage V_{ref} for different operating modes.

3.4. Simulation results for a different storage capacitor

We now examine the system when the capacitance $C_1 = 20\,\mu\text{F}$ and the feedback gain k is smaller. We observe that, unlike in the case for $C_1 = 100\,\mu\text{F}$, fast-scale instability grows in the middle of a half-line cycle, i.e. the regions near the zero-crossings being fast-scale stable. Figure 10 shows various scenarios with different values of the feedback gain k for $C_1 = 20\,\mu\text{F}$. Figure 10(a) shows the stable operation with $k = 0.148$. Figure 10(b) shows fast-scale period-doubling bifurcation in some interval of the line cycle with $k = 0.155$. Figure 10(c) shows the

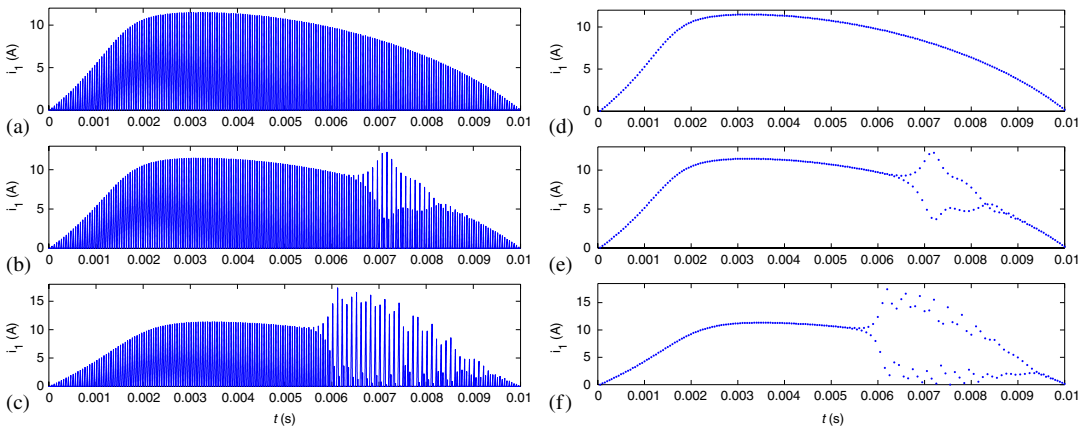

Figure 10. (a)–(c) Time-domain waveforms; and (d)–(f) sampled-data waveforms of i_1 for $C_1 = 20\,\mu\text{F}$ and $V_{\text{ref}} = 90\,\text{V}$.

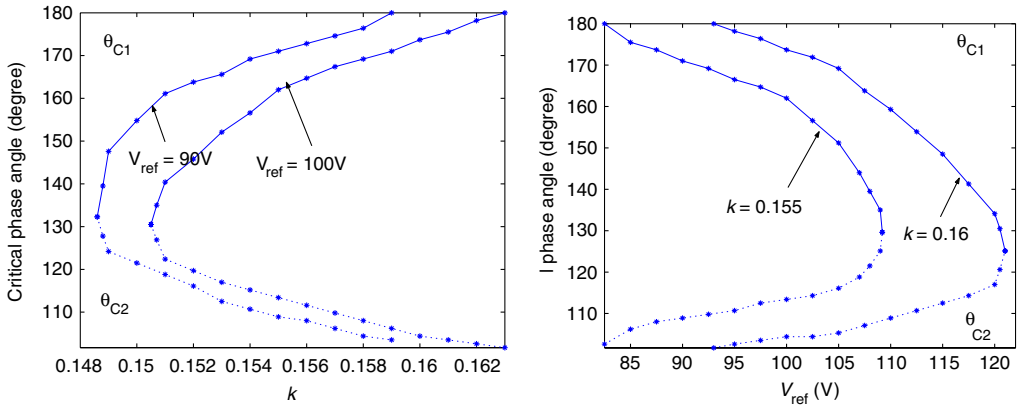

Figure 11. Left: critical phase angles in line cycle versus feedback gain k; right: critical phase angles in line cycle versus V_{ref}, both for $C_1 = 20\,\mu\text{F}$. θ_{c1} and θ_{c2} are the critical phase angles at which period-doubling bifurcation begins to occur. Fast-scale unstable regions correspond to $\theta_{c2} < \theta < \theta_{c1}$.

growth into chaos in some interval of the line cycle with $k = 0.159$. Figures 10(d)–(f) shows the corresponding sampled-data waveforms.

Similarly, we denote the two critical points in terms of phase angle as θ_{c2} and θ_{c1} and the corresponding unstable region is $[\theta_{c2}, \theta_{c1}]$. Figure 11 plots the two critical phase angles θ_{c1} and θ_{c2} as functions of the feedback gain k and V_{ref}. Here, we observe that the converter fails to maintain the desired stable operation in the interval $\theta_{c2} < \theta < \theta_{c1}$. We can also obtain from the simulation results that the width of the bifurcation region $[\theta_{c2}, \theta_{c1}]$ increases as k increases while it decreases as V_{ref} increases.

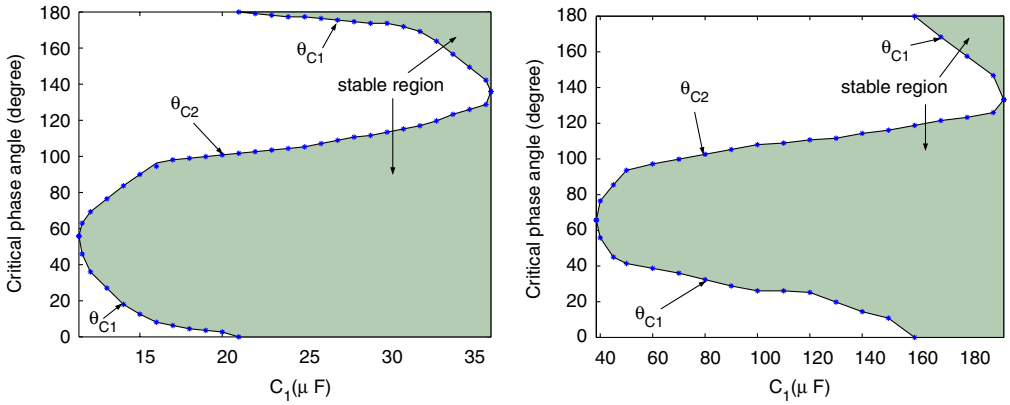

Figure 12. Left: critical phase angles versus C_1, with $V_{\text{ref}} = 90\,\text{V}$ and $k = 0.16$; right: critical phase angles versus C_1, with $V_{\text{ref}} = 90\,\text{V}$ and $k = 0.18$.

3.5. *Effects of storage capacitance on fast-scale instability*

In the foregoing, we observe apparently different instability manifestations. Specifically, when the feedback gain k is fixed, for $C_1 = 100\,\mu\text{F}$, the growth of fast-scale instability takes place near zero-crossings of the line cycle, whereas for $C_1 = 20\,\mu\text{F}$, such fast-scale instability occurs near the high input-voltage regions of the line cycle. In this subsection, we present a detailed inspection of the effect of the size of the storage capacitance. Extensive simulations have been performed to track the values of the critical phase angles as C_1 increases. The results are shown in Figure 12. There is no sudden jump of the critical phase angles as the storage capacitance varies. Instead, a continuous transition has taken place, as clearly illustrated in Figure 12. This general transition, giving rise to the different locations of stability regions observed for different values of storage capacitance, are due to the phase shift of the storage capacitor voltage. Such a trend is generally observed for different values of feedback gain k. Furthermore, the width of the stable region increases as C increases.

Remarks on practical design applications. The usefulness of the foregoing analysis lies in the systematic identification of the parameter regions within which the system operates without being fast-scale unstable. However, as for any practical non-linear system, the above analysis has been carried out by numerical computation and no general closed form expressions can be derived for the parameter regions. Nonetheless, the approach we have derived in the foregoing can be used to find the operating parameter regions for any given set of circuit parameters. Specifically, we have identified several important parameters that affect fast-scale instability and how fast-scale instability occurs relative to variations of these parameters. Thus, there are two general approaches one may take when designing such PFC voltage regulators. First, the above results have clearly provided the behaviour trends in terms of the directions in which parameter changes may cause fast-scale instability. Thus, when fast-scale instability occurs, engineers would have a clear idea as to which operating parameters are relevant to the problem and how (in which directions) they should be adjusted in order to prevent the system from being fast-scale unstable. Second, more formally, we may derive the operating parameter regions numerically using the aforedescribed procedure. Based on the computed

stable regions, we may select the set of operating parameters to guarantee fast-scale stability of the system.

4. EXPERIMENTAL VERIFICATIONS

A circuit prototype of the SSIPP under study has been constructed for verification purposes, as shown in Figure 13. Our emphasis here is the qualitative behaviour and the effects of parameter variations. We stress that absolute verification of a particular set of simulation results

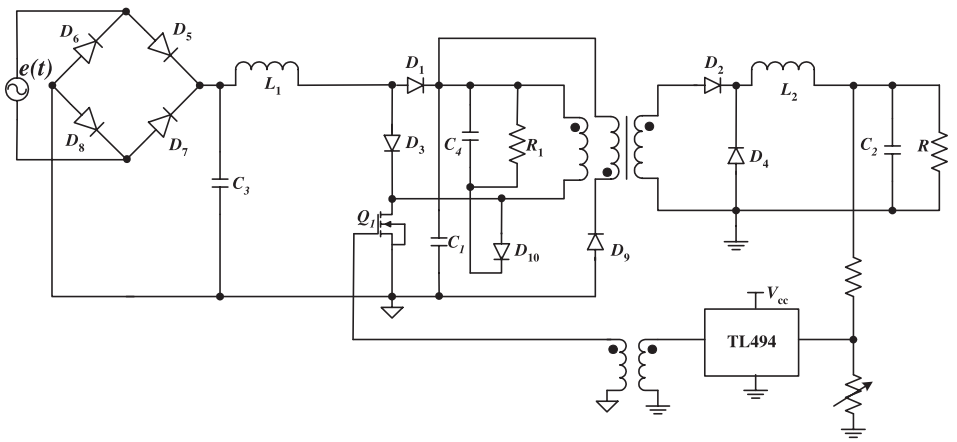

Figure 13. Schematic of experimental circuit. All diodes on the primary side are MUR1560 and those on secondary side are MBR20100. Transistor Q_1 is IRF840. $L_1 = 100\,\mu\text{H}$, $L_2 = 600\,\mu\text{H}$, $C_3 = 0.1\,\mu\text{F}$. Core reset $C_4 = 4.7\,\text{nF}$, $R_1 = 10\,\text{k}\Omega$. Transformer turns ratio is 4:4:1, with $L_{\text{prim}} = 12\,\text{mH}$, $L_{\text{reset}} = 12\,\text{mH}$, $L_{\text{sec}} = 3\,\text{mH}$. Details of control circuit and driver omitted.

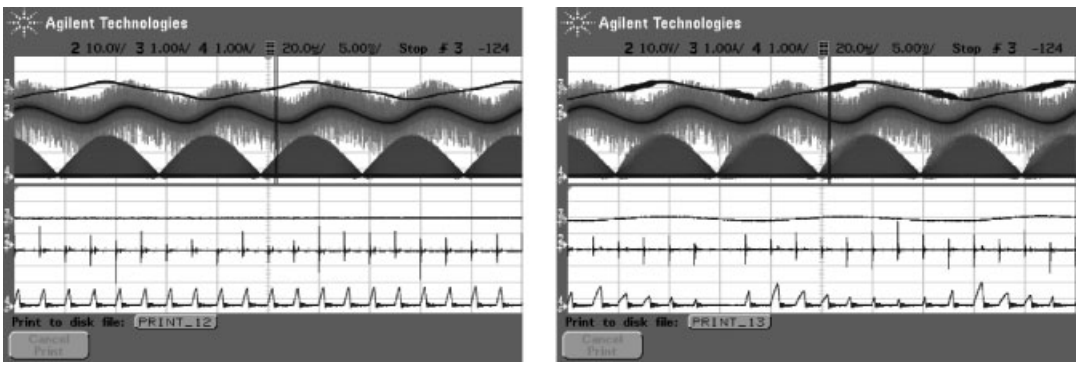

Figure 14. Measured waveforms for $V_{\text{in}} = 90\,\text{V}$ (rms), $C_1 = 60\,\mu\text{F}$; $V_{\text{o}} = 17\,\text{V}$, $R = 14\,\Omega$ and $f_s = 100\,\text{kHz}$. Top three traces are i_2, v_{C1}, and i_1 with timebase set at 5 ms/div, and bottom three traces correspond to the same waveforms with timebase set at 10 μs/div. Left: relatively small feedback gain; right: relatively large feedback gain.

is meaningless for this kind of qualitative study. Also, for reasons of practical feasibility, our experimental circuit has a transformer isolation, which also steps down the output voltage, thus necessitating the use of a larger output capacitor for achieving the same output ripple content. The values of the basic components used are $L_1 = 100\,\mu\text{H}$, $L_2 = 600\,\mu\text{H}$, $C_2 = 1000\,\mu\text{F}$, which ensure the converter operates in the expected mode at 100 kHz. The others are varied in the experiments and will be reported individually. We will henceforth focus on examining the effects of varying the various parameters and verify the general stability trends reported in the previous section.

Figure 14 shows the measured waveforms of output current, storage capacitor voltage and input current for two feedback gains. The waveforms on the right clearly show substantial fast-scale instability, verifying that fast instability develops when the feedback gain increases. Figure 15 shows the waveforms for two input-voltage values. Here, we verify that fast-scale instability becomes more severe (with larger part of the line cycle being

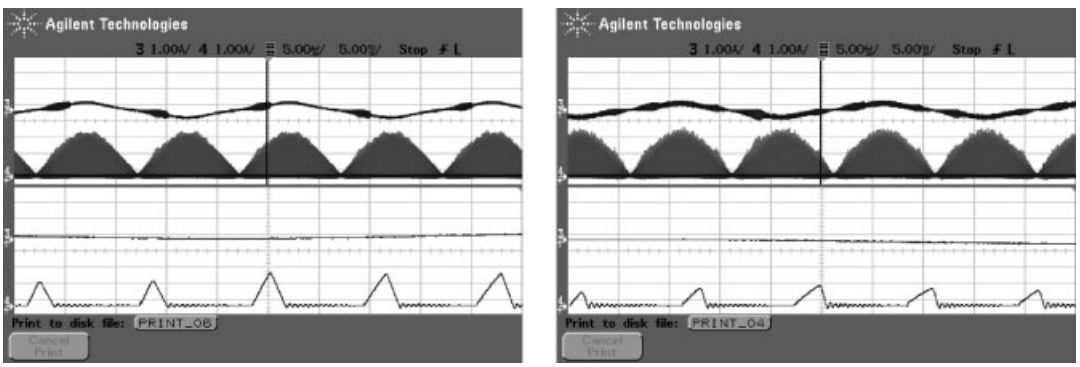

Figure 15. Measured waveforms for $C_1 = 520\,\mu\text{F}$; $V_o = 17\,\text{V}$, $R = 17\,\Omega$ and $f_s = 100\,\text{kHz}$. Top three traces are i_2 and i_1 with timebase set at 5 ms/div, and bottom three traces correspond to the same waveforms with timebase set at 5 μs/div. Left: $V_{in} = 100\,\text{V}$ (rms); right: $V_{in} = 110\,\text{V}$ (rms).

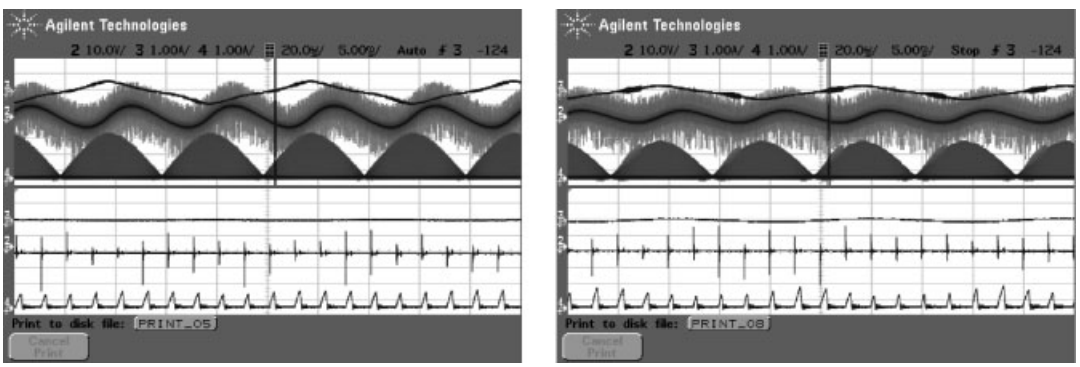

Figure 16. Measured waveforms for $V_{in} = 90\,\text{V}$ (rms), $C_1 = 60\,\mu\text{F}$, $V_o = 17\,\text{V}$ and $f_s = 100\,\text{kHz}$. Top three traces are i_2, v_{C1}, and i_1 with timebase set at 10 ms/div, and bottom three traces correspond to the same waveforms with timebase set at 5 μs/div. Left: output current = 1.6 A ($R = 10.6\,\Omega$); right: output current = 0.8 A ($R = 21.25\,\Omega$).

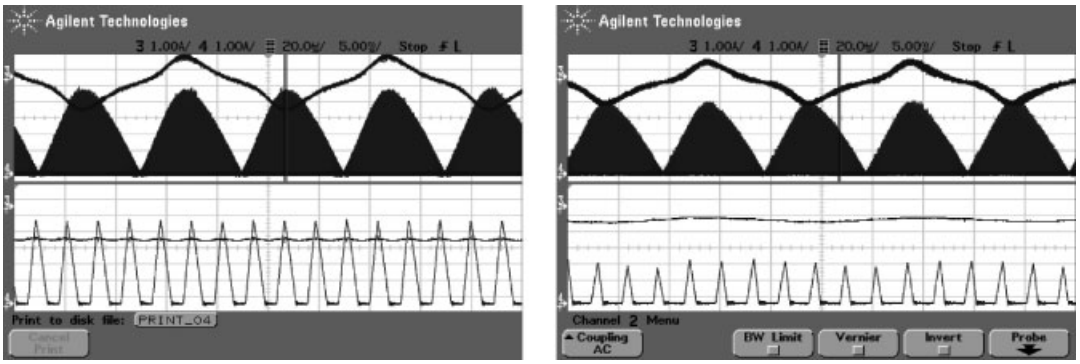

Figure 17. Measured waveforms for $V_{in} = 90\,V$ (rms), $C_1 = 60\,\mu F$, output current $= 3\,A$ and $f_s = 100\,kHz$. Top three traces are i_2 and i_1 with timebase set at 5 ms/div, and bottom three traces correspond to the same waveforms with timebase set at 10 μs/div. Left: $V_o = 23\,V$; right: $V_o = 17\,V$.

fast-scale unstable) when the input voltage increases. Furthermore, Figure 16 shows the relevant waveforms for two output power levels, and we verify that fast-scale instability develops when the power decreases. Finally, Figure 17 shows the same waveforms for two output voltage. Closer inspection of the waveforms shows that fast-scale instability is more severe (with larger part of the line cycle being fast-scale unstable) when the output voltage decreases.

5. CONCLUSION

Power factor correction has become an important design consideration for switching power supplies. For low-power applications (below 200 W), a cost-effective solution is to use a single-stage design in which the power-factor-correction stage is integrated with the dc–dc power stage [1]. Such a design utilizes discontinuous conduction mode of operation of the boost stage to simplify the power-factor-correction control. In this paper we have performed a detailed study of the fast-scale bifurcation behaviour of this converter when the boost stage is operating in discontinuous conduction mode and the forward stage in continuous conduction mode. We have investigated into the effects of various parameters on the stability of the system. Such fast-scale stability problems are important as they affect the peak current stresses imposed on the switching devices. The results obtained here will help engineers diagnose the causes of fast-scale instability when it occurs in single-stage PFC power supplies.

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