

Overload Robust IGBT Design for SSCB Application

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Abstract

This paper presents an optimised power semiconductor architecture based on the CIGBT approach to be used in solid-state circuit breaker (SSCB) applications where the conduction losses have to be as low as possible without compromising the forward voltage blocking capability. Indeed, a high overcurrent turn-off and short-circuit withstand capabilities have to be ensured. Starting from a standard NPT-IGBT design for switching applications, the results show that the proposed device, which is optimised by the application of the individual clustered concept, offers a reduction in conduction losses of 13%, without compromise on voltage blocking capability. An original design solution is implemented to further ensure short-circuit and overload turn-off capabilities at maximum ambient temperature and twice the nominal rated current.

1. Introduction

Fault detection and prompt removal is a critical enabler for the development of advanced electrical power transmission and distribution systems. Therefore, reliable circuit breakers as protection devices to prevent system damage and ensure reliability are essential. The performance and ratings of traditional electro-mechanical circuit breakers cannot meet the demands of upcoming distribution systems (e.g., Energy Internet [1]) (Figure 1). Hence, circuit breakers based on solid-state technology (SSCB) are a promising alternative, as they can bring along several advantages compared to traditional electro-mechanical solutions, such as improved voltage quality during short circuit and reduced short circuit current levels [2-5].

Presently, commercially available IGCTs are the best power devices for SSCB applications. However, SSCB oriented high voltage IGBTs [6-7] would be extremely attractive as they offer many advantages

(Table 1) such as reduced switching losses, simpler and more efficient gate driver, competitive price and mature process technology. Particularly for non-punch-through IGBTs the thermal stability is another attractive feature. This paper presents the design and optimisation of bespoke 3.3 kV IGBTs for SSCB applications, based on numerical 2D electro-thermal TCAD simulations and addresses fabrication aspects of optimised final architecture.

2. SSCB Bespoke Optimization

The typical situation in SSCB applications is for the IGBT to be in the on-state most of the time. The IGBT is turned-off when faults or overloads happen in the system. So, the reduction of the conduction losses is the key parameter during the optimisation phase of a bespoke power semiconductor device. Assuming that many power devices need to be connected in series to meet the typical voltage levels of transmission and even distribution networks

(Figure 2), it is important that optimisation of the on-state performance does not degrade the blocking capability of the device which would require a higher number of series connected switches (eg. an 11kV network needs at least four 3.3kV IGBTs or seven 1.7kV IGBTs). Taking into account the SSCB requirements, the most important features when optimising a power semiconductor device are the maximum overload (current and temperature) turn-off capability, as well as the short circuit withstand capability. The robust handling capability against the two situations is essential for devices in SSCB because overload caused by excessive electric consumption and overcurrent caused by short circuit are fault conditions that likely occur in power transmission/distribution lines.

Table 1 Summary of benchmark performance comparison of the different power device

Feature	IGBT	GTO	IGCT
Conduction losses	High	Low	Low
Switching losses	Low	High	Medium
Failure mode	Open/Short circuit	Short circuit	Short circuit
Gate driver	Simple, compact	Complex, separated	Complex, Integrated
Gate driver power consumption	Low	High	Medium

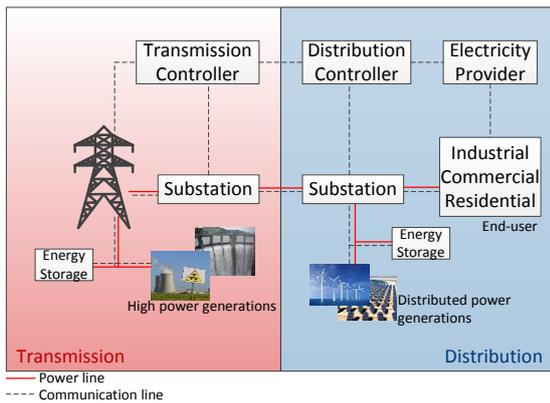


Figure 1: Smart grid power distribution system

The IGBT optimisation starts from a selected reference device with an NPT-planar architecture (core cross-section plotted in Figure 3a), typically designed for switching applications and rated at 3.3kV-100A. The device high voltage drop

(indicated by 4.25V at 50 A/cm²) hints the possibility of device conduction losses improvement. The device is fabricated on a 500 μm thick wafer with a doping profile shown in Figure 3b. A new proposed structure is inspired by the clustered IGBT (CIGBT) concept, schematically illustrated in Figure 4, which is promoted in reducing conduction losses with a simple application of two additional deep diffusions [8-11]. Regarding these two additional layers there are four optimization parameters: doping concentration and thickness of the two new layers.

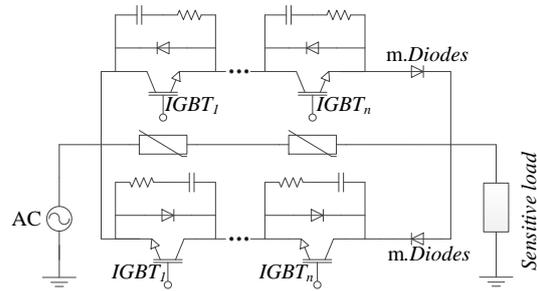


Figure 2: Schematic circuit of SSCB for ac based on IGBTs and diodes.

The doping profile of the proposed architecture is shown in Figure 4b including the tuning parameters. Two approaches have been considered, depending on the thickness of the P-base layer. The first case is based on a narrow P-base layer where the P-base junction ($J_{P,base}$) is set at 2μm (opt-1 case), while the second case (opt-2 case) is contemplates the use of the same P-body characteristics as those of the reference IGBT (7 μm junction depth). The optimisation of the four relevant parameters is divided into two groups, depending on the final target. The concentration and thickness of the additional P-layer ($C_{Add,P}$ and $t_{Add,P}$) are optimised to sustain the required breakdown voltage while the additional N-layer ($C_{Add,N}$ and $t_{Add,N}$) is optimised to get the minimum conduction losses. The starting point and the optimisation methodology are depicted in Figure 5.

The global target for the proposed architecture is to obtain the minimum conduction losses at 50 A/cm² current density while maintaining the 3.3 kV blocking capability. In order to be able to detect a fault event with the subsequent safe turn-of of the SSCB, two constraint parameters are set: the 100 A/cm² overcurrent and the 10 μs short circuit withstand capabilities, both at an ambient temperature (T_{AMB}) of 125 °C.

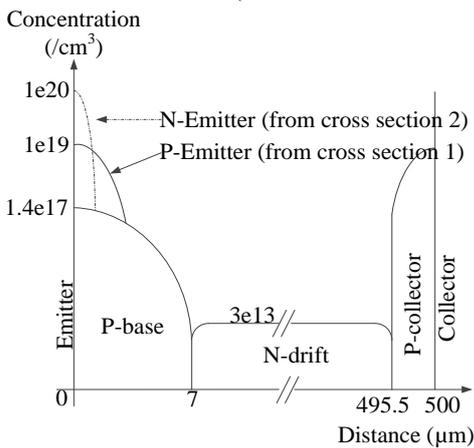
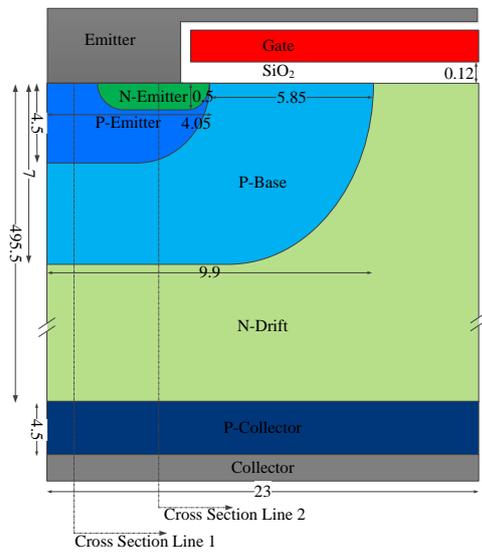


Figure 3: Reference 3.3 kV IGBT structure. Core cross-section (a) and doping profile (b).

The IGBT and the proposed structures are implemented and simulated with Silvaco™Atlas® [12]. Isothermal conditions are used for the steady-state analysis (on-state vs. blocking voltage performance), while fully coupled mixedmode electrothermal simulations are performed for the transient analysis (turn-off and short-circuit capability). The self-heating effect model includes an estimated $4 \text{ cm}^2\text{K/kW}$ thermal resistance between the collector electrode (device backside) and the thermal ground (ambient temperature of 125°C).

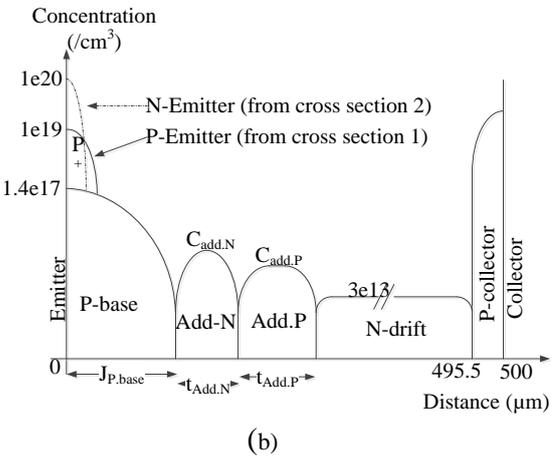
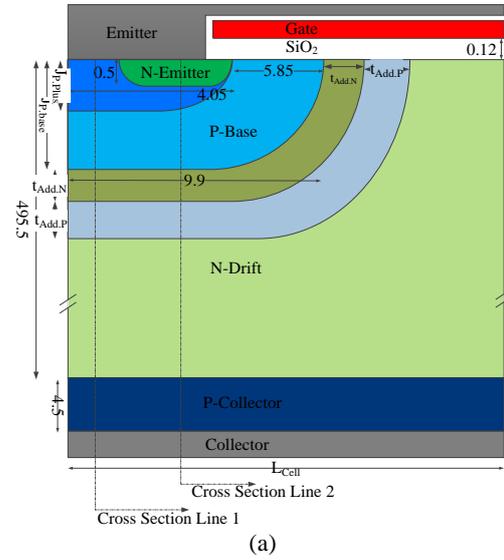


Figure 4: Optimized SSCB structure with schematic core cross-section (a) and parameterized doping profile (b).

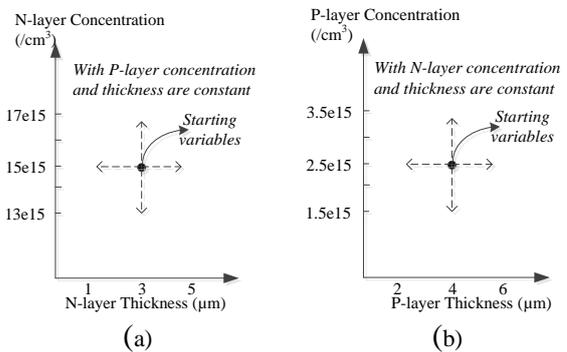


Figure 5: Optimization methodology.

3. Simulation results and design optimisation

The optimised additional P-layer for the opt-1 case corresponds to a maximum doping concentration ($C_{\text{add.N}}$) of $3 \times 10^{15} \text{ cm}^{-3}$ and a thickness ($t_{\text{Add.N}}$) of $5 \mu\text{m}$, leading to a forward blocking capability of 3460 V. The simulated output characteristics revealed that the optimum additional N-layer has to be implemented with a maximum doping concentration ($C_{\text{add.P}}$) of $1.58 \times 10^{16} \text{ cm}^{-3}$ and a thickness ($t_{\text{Add.P}}$) of $3.8 \mu\text{m}$ in order to reach the maximum improvement of the conduction losses (13% lower when compared to the reference IGBT losses of 60.26 W).

The simulated type-1 short-circuit test (Figure 6a) has corroborated that the proposed architecture withstands 10 μs short circuit at 1800 V input voltage. However the simulation of the overcurrent capability test encountered a latch-up event that makes the optimized structure failed to reach the targeted 100 A overcurrent capability. The overcurrent capability test is based on the double pulse circuit plotted in Figure 6b [13] with which the turn-on and turn-off processes at the nominal current (50 A) and the turn-off at overcurrent can be obtained.

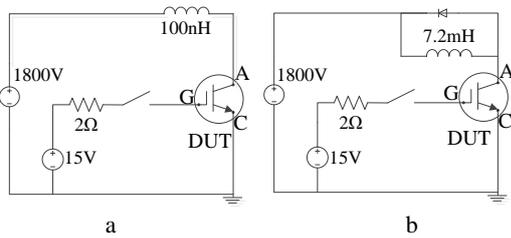


Figure 6: a. Switching test circuit; b. Short-circuit test circuit

The simulated current density during the turn-off process of the proposed architecture are shown in Figure 7, corroborating the latch-up of the parasitic $\text{N}^+/\text{P-base}/\text{N}/\text{P}$ thyristor. The conduction current density corresponding to 1 μs before turn-off clearly show the inversion channel on top of the P-base layer (Figure 7a). The inversion channel is completely removed 1 μs after the gate voltage is ramped to zero (Figure 7b). However, a high current density is still flowing through the structure due to the activation of the parasitic thyristor structure (Figure 7b). In this situation, electrons are injected from the narrow N^+ layer into the P-base and holes are therefore injected from the additional P-layer into the additional N-layer, as shown in Figure 8.

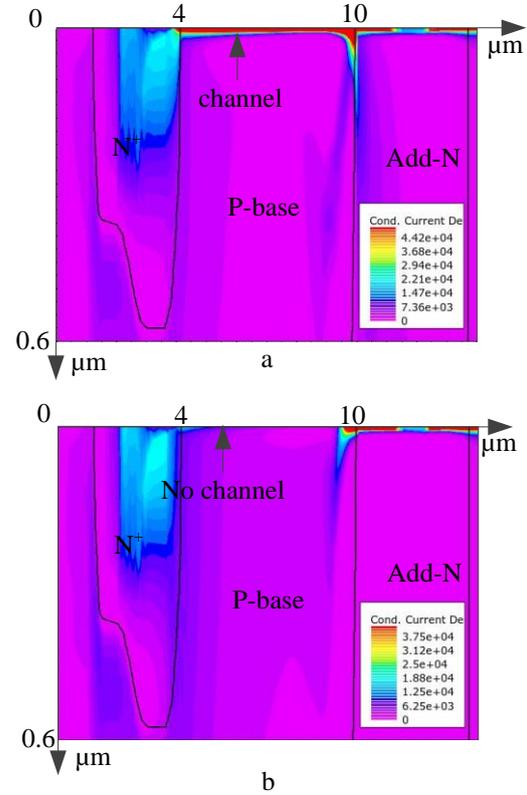


Figure 7: Simulated conduction current density at (a) 1 μs before turn-off and (b) 1 μs after turn-off.

The activation of the parasitic thyristor structure can be overcome by enlarging the thickness of the P-base layer from 2 μm (in the opt-1 case) to 7 μm (for the opt-2 case). As a consequence, the turn-off current capability reaches the targeted 100 A at the cost of an increase of the conduction losses. To reinstate to the initial on-state performance, the additional N-layer has to be set to a maximum doping concentration of $2.35 \times 10^{16} \text{ cm}^{-3}$ and a thickness of 4.78 μm . The simulated double pulse test for the opt-1 and opt-2 cases is reported in Figure 9, where the latch event can be clearly envisaged in the opt-1 case while opt-2 case is able to turn-off a 100 A current. The simulated short-circuit test (Figure 10) pictured the ability of both proposed structure in withstanding 10 μs short-circuit condition.

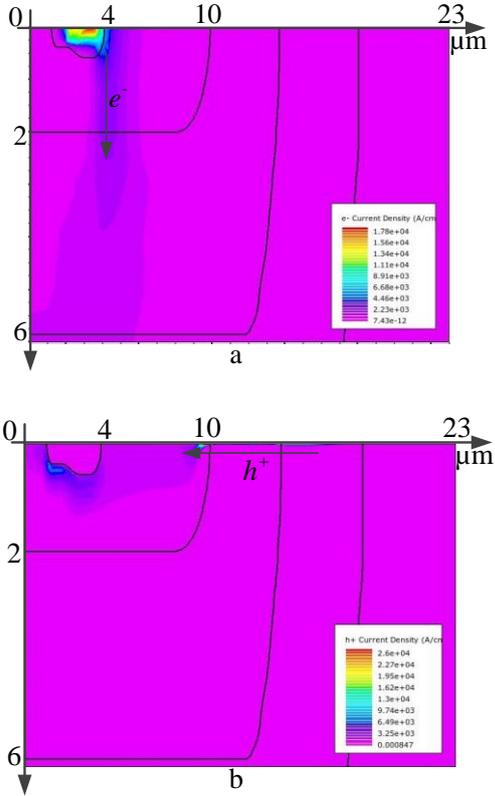


Figure 8: Simulated conduction current density at 1 μs after turn-off due to the latch-up event (a) electron concentration and (b) hole concentration.

The relevant electrical characteristics of the reference IGBT structure and the two cases of the proposed architecture are listed in Table 2.

In addition, as a first approximation, a fabrication process has been simulated (SilvacoTMAthena[®]) in order to get an idea about its feasibility. From these simulations, we can conclude that the additional P and N wells (Figure 4b) can be achieved if high energy implantations (around 500 MeV) are performed and the later diffusions are carried out at 1200°C. Both implantations to form the P and N additional wells can be done within the same window implantation, therefore, just one additional mask level must be included.

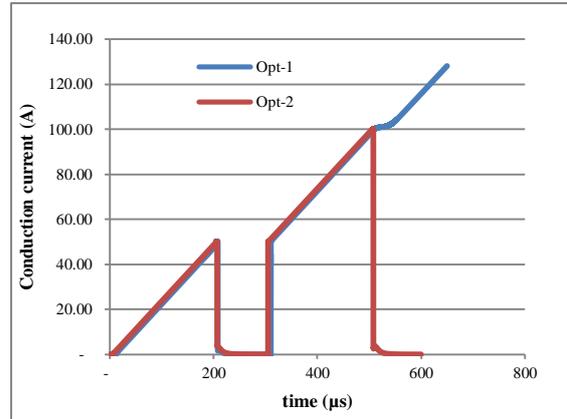


Figure 9: Turn-off performance of the two cases of the proposed architecture at normal conduction (50 A) and overcurrent (100 A) conditions.

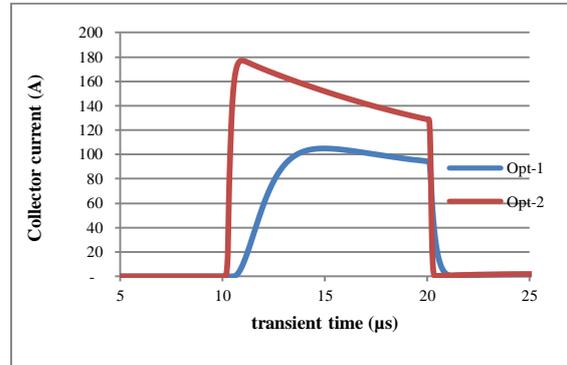


Figure 10: Short-circuit performance of the two cases of the proposed architecture

Table 2: optimized structure performance comparison

Characteristics	Reference	Opt-1	Opt-2
Conduction loss (W)	60.26	52.48	50.89
Forward blocking (V)	3460	3460	3460
Overcurrent turn-off capability	✓	x	✓
10 μs short circuit capability	✓	✓	✓

4. Conclusion

In conclusion, performed simulation results show that the additional N and P layers beneath the conventional P-base diffusion of an IGBT structure exhibit an improved on-state performance with no significant degradation of the forward blocking capability. Moreover, the improved maximum overload turn-off capability due to the thickened P-base diffusion is crucial to design a robust power

switch for SSCB applications. Hence, the proposed architecture is a promising candidate for high-performing SSCBs.

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