

Optimization of Quantum Circuit Mapping using Gate Transformation and Commutation

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Abstract

This paper addresses quantum circuit mapping for Noisy Intermediate-Scale Quantum (NISQ) computers. Since NISQ computers constraint two-qubit operations on limited couplings, an input circuit must be transformed into an equivalent output circuit obeying the constraints. The transformation often requires additional gates that can affect the accuracy of running the circuit. Based upon a previous work of quantum circuit mapping that leverages gate commutation rules, this paper shows algorithms that utilize both transformation and commutation rules. Experiments on a standard benchmark dataset confirm the algorithms with more rules can find even better circuit mappings compared with the previously-known best algorithms.

1 Introduction

Despite the limitation on the number of qubits, types of operations, and the operation time, Noisy Intermediate-Scale Quantum (NISQ) computers are expected to be useful in the near future for many applications of quantum chemistry, machine learning, optimization, and sampling [1]. To be able to run a quantum algorithm on NISQ devices for such applications, the quantum algorithm is first transformed into a series of quantum operations (or quantum gates) on the quantum bits (or qubits). A set of quantum gates that consists of arbitrary one-qubit rotation gates and two-qubit controlled-NOT (or CNOT) gates is universal, i.e., any quantum operation can be realized by a combination of such basic gates. However, because CNOT gates cannot be applied on all pairs of qubits of a NISQ device, an input circuit must be transformed into an output circuit that obeys the limitation of the device. The transformation can further limit the usability of the device, and therefore, a better compiler is one of the most essential elements to utilize a NISQ device.

In this paper, we address the task on how to *compile* a given quantum circuit (i.e., transform it into an equivalent circuit) so that it can be run on NISQ devices. We call such a task *quantum circuit mapping* as it deals with mapping qubits in the given quantum circuit to the actual qubits of NISQ devices with necessary additional gates to obey the two-qubit operational constraints.

Figure 1a is an example of an input circuit that uses a single-qubit gate, called the phase-shift gate (denoted as R_z), and CNOT gates (depicted with vertical lines whose ends are \bullet and \oplus denoting the control and target qubits, respectively). These gates act on qubits each represented by a horizontal line in the figure, and are applied from left to right. Figure 1b is an example of a *coupling graph*, which is a graph representing which pairs of qubits can be coupled, i.e., be used by two-qubit CNOT gates. Currently available NISQ devices, such as IBM Q systems [2], are limited by their coupling architecture in the sense that not all pairs of qubits can be directly employed due to hardware issues. If we map the qubit b_i (as numbered in the circuit) in Fig. 1a to q_i (as numbered in the hardware)

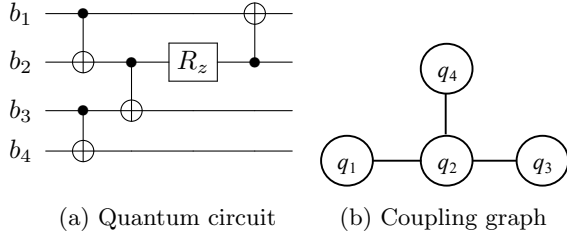


Figure 1: Quantum circuit (left), and coupling graph of a NISQ device that limits two-qubit operations (right). The problem is finding a mapping of $\{b_i\}$ to $\{q_j\}$ and additional gates so that the circuit can be run in the NISQ device with minimum cost.

for $i = 1, \dots, 4$, the CNOT gate from b_3 to b_4 is not directly possible. This can be resolved by swapping control and/or target qubits with their neighboring qubits until they are adjacent in the coupling graph. Such swapping can be carried out by so-called SWAP gates (Fig. 2a). Another way to run a CNOT gate between non-adjacent qubits is replacing it with a sequence of CNOT gates. This composite gate is called a Bridge gate and is composed of four CNOT gates as shown in Fig. 2b. In both cases, we need to add supplementary gates to the original circuit, resulting in more noise and computational time since CNOT gates are noisy and take significantly more time for computation than single-qubit gates. Thus, minimizing additional gates in the circuit mapping is important as it translates into minimizing the increase of time and noise cost to run the circuit. Indeed, there has been a large body of work addressing the quantum circuit mapping (see Section 2 for details). However, most of those circuit mappings are not optimal because they add supplementary gates layer by layer in the given quantum circuit.

In our recent paper [3], we discussed the drawback of resolving the two-qubit operations layer by layer in many existing approaches and showed the importance of taking into account gate commutation rules. We demonstrated how four simple commutation rules, which consists of commuting CNOT gates and/or single-qubit gates, can lead to quantum circuit

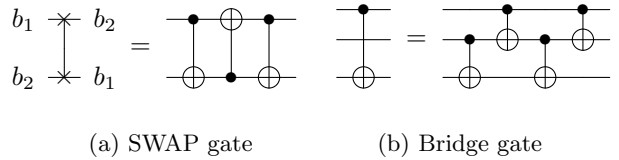


Figure 2: Supplementary gates to be used in circuit mapping

mapping with significantly fewer additional SWAP gates.

In this paper, we further extend the formulation with commutation rules and transformation rules of running CNOT gates on non-adjacent qubits by choice of replacing with Bridge gates or inserting SWAP gates. Although SWAP and Bridge gates seem to require different numbers of CNOT gates (three as in Fig. 2a, and four as in Fig. 2b), a Bridge gate results in running the CNOT gate, whereas a SWAP gate only swaps its two qubits. Thus, the total number of additional CNOT gates to run a CNOT gate between an unconnected qubit pair is the same for both SWAP and Bridge gates. However, the SWAP gate permutes the ordering of the logical qubits, whereas the Bridge gate does not. Depending on the sequence of gates afterwards, the selection of SWAP and Bridge gates can affect the possibility of further reducing the additional CNOT gates in the mapping.

Experiments on a well-known benchmark dataset show that the new transformation rules can lead to even better cost of mapping than with known approaches: 14.2% fewer additional CNOT gates on average than those without the new rules. Hence, this paper demonstrates the generality and the high potential of the formulation of quantum circuit mapping that takes into account transformation and commutation rules for quantum gates.

2 Motivation and Related Work

The main contribution of this paper is proposing algorithms using both gate commutation and trans-

formation rules (i.e., the Bridge and SWAP gates) that result in better circuit mappings for existing benchmark circuits. There have been many studies of quantum circuit mapping, e.g., those dealing with the circuit mapping on 1D-chain (known as linear nearest neighbor (LNN)) topology [4, 5, 6, 7, 8, 9, 10], those on 2D-grid nearest neighbor topology [11, 12, 13, 14], and, like ours, those on the general topology of NISQ devices [15, 16, 17, 18, 19, 20, 21]. A recent study [22] discussed the complexity of circuit compilers on NISQ devices and their search-space structure. However, to the best of our knowledge, those studies either did not fully consider the gate commutation rules or did not consider transformation rules other than SWAP gates.

With regard to gate commutation rules, many previous studies assumed a *fixed-layer formulation*, where the layers of a quantum circuit are given as input and all gates in a layer must be mapped, and when necessary resolved with SWAP gates, before any gate in the next layer. A *layer* is defined as a set of CNOT gates that can be executed in parallel (see the top part of Fig. 3). Previously, we pointed out that the fixed-layer formulation may lead to suboptimal solutions, and proposed a formulation of circuit mapping that uses the commutation rules to avoid suboptimal solutions [3].

The drawback of the fixed-layer approach can be seen from the circuit in Fig. 1a when the coupling graph is as shown in Fig. 1b. The number of additional SWAP gates by the fixed-layer formulation is two, but it is one if we allow to be changed the order of gates by applying the standard commutation rules of quantum gates illustrated in Fig. 4. The reason is as follows.

For the circuit in Fig. 3, by the R_z -control rule (Fig. 4a), we can move the CNOT gate CX_4 to the left so that it precedes R_z . Now, the CNOT gates CX_3 and CX_4 share the control qubit, and by the control-control rule (Fig. 4b) we can move CX_4 to the left. As a result, when b_i is mapped to q_i , CX_1 and CX_4 can be applied before swapping b_2 and b_3 to run CX_2 , CX_3 , and CX_5 . This is not possible for the circuit *with fixed layers* in Fig. 3 because CX_4 in layer 3 cannot precede CX_2 in layer 2.

Because the partial order of gates in a circuit is naturally modeled with a directed acyclic graph (DAG),

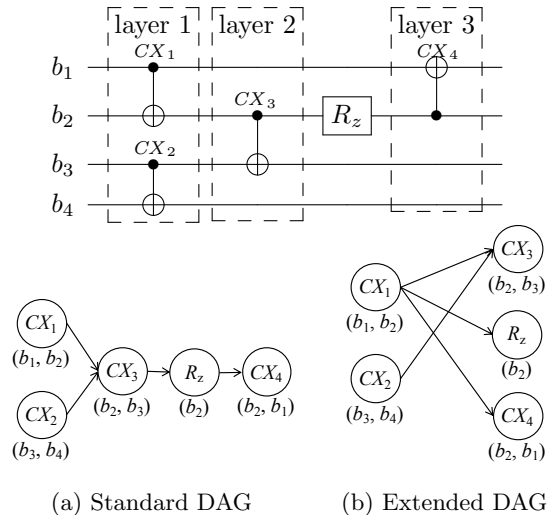


Figure 3: Quantum circuit with 3 layers (top) and its dependency graphs (bottom)

some studies [19, 23] have considered trivial commutation between consecutive gates that do not share qubits. For example, Fig. 3a is a DAG representation of the circuit in the top part of Fig. 3. We call this *the standard-DAG formulation*. Although it is more flexible than the fixed-layer one, it still may fall into suboptimal solutions: it leads to two additional SWAP gates for the circuit in Fig. 3.

To overcome the suboptimality problem, Itoko et al. [3] proposed a novel formulation taking into account gate commutation rules in combination with the concept *dependency graph* that extends the standard-DAG. The dependency graph depicts the true partial order of gates as imposed by the commutation rules. For example, the dependency graph of the circuit in Fig. 3 is shown in Fig. 3b. The dependency graphs with fewer commutation rules than those in the work of Itoko et al. [3] were first considered by Matsuo et al. [4]. Venturelli et al. [18] considered commutation rules specific to their circuits of interest and proposed a solution based on a temporal planner; however, they did not provide systematic methods exploiting the rules, unlike our approaches. Recently, Li et al. [19] independently proposed a heuristic algorithm very similar to ours. To be precise, although they do not

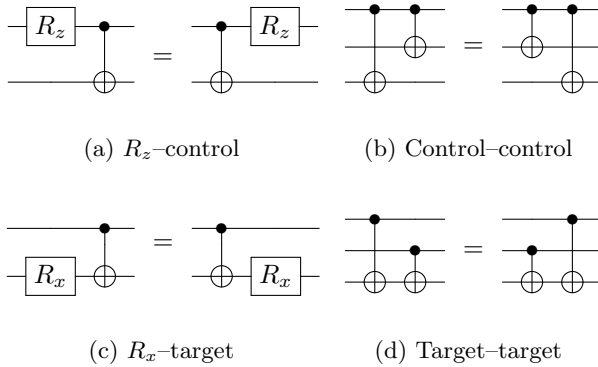


Figure 4: Standard commutation rules of quantum gates

explicitly consider commutation rules in their heuristic, it is easy to modify their algorithm to take into account our proposed dependency graph. However, like other mappings, they only use SWAP gates to map two-qubit gates to NISQ devices.

In this paper, we consider Bridge gate as well as SWAP gate as a transformation rule used in mapping. There are only a few studies considering Bridge gate (aka, chain template), e.g. [17, 24]. Although their main purpose was for the synthesis of quantum circuit from a unitary matrix, Shende et al. [24] hinted that quantum circuit mapping can be solved with only chain templates. Siraichi et al. [17] provided exact and heuristic algorithms using both SWAP and Bridge gates, but they reported the implementation of their heuristic in Qiskit [23] did not perform well for non-synthetic circuits, which may be caused by not using the dependency graph.

3 Problem Formulation

We propose a formulation of quantum circuit mapping that takes into account gate commutation and transformation rules to minimize the number of additional CNOT gates. We first describe the notations used hereafter.

We use the term *logical qubits* to represent the qubits in the original quantum circuit (denoted by B).

This is not to be confused with the term logical qubits in the context of quantum error correction. We use the term *physical qubits* to represent the qubits of the quantum hardware (denoted by Q). For example, $B = \{b_i\}$ and $Q = \{q_j\}$ denote logical qubits and physical qubits in Fig. 1a and 1b, respectively. Similarly, we call the input circuit the *logical (quantum) circuit* and its corresponding output of quantum circuit mapping the *physical (quantum) circuit*. The physical circuit is equivalent to its logical circuit in terms of computation but may contain additional gates due to coupling constraints. A coupling graph $C = (V_C, E_C)$ is a graph with physical qubits as nodes $V_C (= Q)$ and coupled physical qubits as edges E_C . We assume that $|B| = |Q|$ by adding ancillary qubits to B if $|B| < |Q|$.

A mapping of logical qubits to physical qubits can be seen as a permutation function $B \rightarrow Q$, which we call a *layout*. A logical/physical circuit can be seen as a list of gates acting on logical/physical qubits. We say a physical circuit \hat{L} *complies* with a coupling graph C if, for any CNOT gate in \hat{L} , its control and target qubits are adjacent in C . A mapping of a logical circuit L to a quantum computer with a coupling graph C can be represented by an *initial layout* l_0 of qubits and a physical circuit \hat{L} that complies with C .

The objective of quantum circuit mapping is to find a cost-optimal physical circuit of a logical circuit. In this paper, we consider the number of additional CNOT gates as the cost of mapping because they are usually much noisier and slower to run than single-qubit gates.

The problem of finding a corresponding physical circuit of a logical circuit with the minimum number of CNOT gates is formalized as follows.

Minimum CNOT Gate Mapping (MCGM)

Given a logical circuit L , the coupling graph C of a quantum hardware, and a set of commutation rules \mathcal{R} , find an initial layout l_0 and an equivalent physical circuit \hat{L} with the fewest CNOT gates that complies with C .

Note that fixed-layer and standard-DAG formulations in many previous work can be regarded as special cases of MCGM: the former with $\mathcal{R} = \emptyset$, and the latter with \mathcal{R} containing trivial commutation between

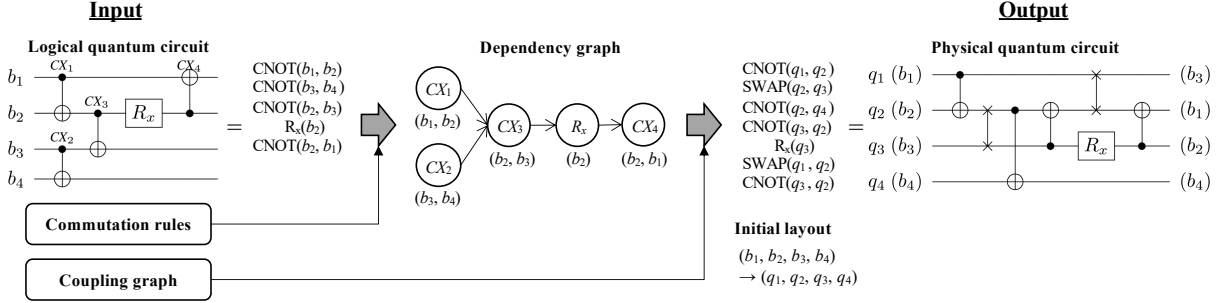


Figure 5: Overview of our circuit mapping based on Minimum CNOT Gate Mapping (MCGM) formulation

consecutive gates that do not share qubits. In the next section, we propose algorithms that utilize the commutation rules in Fig. 4 for \mathcal{R} in MCGM because they are complete for rules involving two consecutive gates from the universal gate set $\{R_x, R_z, \text{CNOT}\}$, and the transformation rules of CNOT gates with SWAP or Bridge gates. Here R_x and R_z denote single-qubit rotation (respectively, around the x -axis and z -axis) gates. Without loss of generality, we assume any input circuit is composed of gates from the universal gate set.

4 Algorithms

We show how to solve the Minimum CNOT Gate Mapping (MCGM) with an exact algorithm based on dynamic programming (DP), and a heuristic algorithm based on a look-ahead scheme. To minimize the number of additional CNOT gates, both algorithms resort to minimizing the number of additional SWAP and Bridge gates, each of which requires three additional CNOT gates. Note that a Bridge gate can only be applied to run a CNOT gate when the distance between control and target qubits of the CNOT gate is exactly two. Both algorithms are extensions of algorithms minimizing SWAP gates introduced in [3]. The exact algorithm can obtain optimal solutions but can only be used for small circuits because of its long computational time. The heuristic algorithm can obtain good solutions for a larger circuit within a reasonable amount of computational time. The building blocks

of the algorithms are dependency graphs and blocking gates, as explained below. Figure 5 shows an overview of our circuit mapping algorithms.

Dependency Graph A dependency graph $D = (V_D, E_D)$ is a DAG that represents the precedence relation of the gates in an input circuit taking commutation rules into account. The nodes V_D correspond to the gates in the logical circuit, and the edges E_D to the dependencies in the order of gates. A gate g_i must precede g_j under the commutation rules if and only if there exists a path from g_i to g_j on D . See Fig. 3 for examples of dependency graphs: one for trivial commutation rules of gates that do not share qubits, and the other for commutation rules in Fig. 4. The labels below a gate (node) in the dependency graphs represent the logical qubits that the gate acts on, e.g., CX_1 acts on (b_1, b_2) .

We can construct a dependency graph D from a given logical quantum circuit, as in Fig. 1a, straightforwardly as follows (see A for the details). We check all pairs of the gates V_D in the circuit, and include an edge (g_i, g_j) in E_D if the following conditions are satisfied: (1) g_i and g_j share at least one logical qubit b , and (2) the set of gate symbols from g_i to g_j on each shared b in the logical quantum circuit is not a subset of R_z, \bullet (i.e., R_z gate and control of CNOT gate) or a subset of R_x, \oplus (i.e., R_x gate and target of CNOT gate).

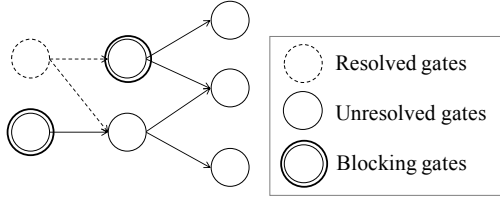


Figure 6: Blocking gates in dependency graph

Blocking Gates Both exact and heuristic algorithms take the same strategy by resolving the gates in the dependency graph D one by one. They maintain the progress by recording *blocking gates*, which are defined as leading unresolved gates in D as shown in Fig. 6. For given gates G (usually blocking gates), we define *blocking gates from G for l* by blocking gates after running leading gates that comply with the coupling graph C repeatedly starting from G under the layout l . At the beginning of mapping, the gates with no in-edges in D , say G_0 , can be seen as blocking gates. For a given initial layout l , we define the *initial blocking gates for l* (denoted by $K_0(l)$) to be the blocking gates from G_0 for l .

4.1 Exact algorithm

We design an exact algorithm to solve MCGM based on DP. To achieve this, we define a *state* similar to DP by (l, K) , a pair of a layout l and blocking gates K .

A transition between a pair of states occurs when a SWAP or Bridge gate is inserted. For example, let us consider the logical circuit and dependency graph as in Fig. 5 and the coupling graph as in Fig. 1b. Then, the blocking gates from $\{CX_1, CX_2\}$ for an initial layout $l_0 : (b_1, b_2, b_3, b_4) \mapsto (q_1, q_2, q_3, q_4)$ is $\{CX_2\}$. This is because the leading CX_1 can be run, but CX_2 blocks the rest of the gates. If we choose the SWAP gate between b_2 and b_3 , $\text{SWAP}(b_2, b_3)$, (or equivalently $\text{SWAP}(q_2, q_3)$ under l_0), it changes the state $(l_0, \{CX_2\})$ to another state $((b_1, b_2, b_3, b_4) \mapsto (q_1, q_3, q_2, q_4), \{CX_4\})$. Alternately, we can choose the Bridge gate from $q_3 = l_0(b_3)$ to $q_4 = l_0(b_4)$ via q_2 to run $CX_2 = \text{CNOT}(b_3, b_4)$, where for simplicity we denote the mapping of a logical

Algorithm 1 DP-based exact algorithm for MCGM

IN: A dependency graph $D = (V_D, E_D)$ with logical qubits B , a coupling graph $C = (V_C, E_C)$ with physical qubits Q

OUT: The minimum number of SWAP and Bridge gates in mapping of D to C

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1:  $S \leftarrow \{(l, K_0(l)) \mid \text{layout } l \text{ from } B \text{ to } Q\}$  // active states
2:  $f(l, K) \leftarrow 0$  for all initial state  $(l, K) \in S$ 
3: while True do
4:    $S' \leftarrow \emptyset$  // next active states
5:   for all state  $(l, K)$  in  $S$  do
6:     for all edge  $e$  in  $E_C$  do
7:        $l' \leftarrow$  layout after swapping  $e$  of  $l$ 
8:        $K' \leftarrow$  blocking gates from  $K$  for  $l'$ 
9:       if  $f(l', K')$  is not yet defined then
10:         $f(l', K') \leftarrow 1 + f(l, K)$ 
11:         $S' \leftarrow S' \cup \{(l', K')\}$ 
12:       end if
13:       if  $K' = \emptyset$  then return  $f(l', K')$ 
14:     end for
15:   for all CNOT gate  $g$  (acting on  $(b_i, b_j)$ ) in  $K$  do
16:     if distance between  $l(b_i)$  and  $l(b_j)$  on  $C = 2$  then
17:        $l' \leftarrow l$  // no change in layout
18:        $K' \leftarrow$  blocking gates from  $K \setminus \{g\}$  for  $l$ 
19:       Do the same procedure between line 9 and 13
20:     end if
21:   end for
22: end for
23:  $S \leftarrow S'$ 
24: end while

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qubit b_i to a physical qubit q_j under layout l_0 as $q_j = l_0(b_i)$. The transformation of CNOT into a Bridge gate changes the state $(l_0, \{CX_2\})$ to another state (l_0, \emptyset) . That is, the transformation does not change the layout but updates the blocking gates $\{CX_2\}$ to \emptyset . After CX_2 is run as the Bridge gate, all the remaining gates can be run under the same layout l_0 . This example shows how Bridge gates are important to realize better mapping algorithms.

Let $f(l, K)$ denote the minimum number of additional SWAP and Bridge gates required to reach a state (l, K) starting from any initial state. Here an

initial state is a state defined by $(l, K_0(l))$ for an initial layout l . The minimum number of SWAP and Bridge gates in a mapping is thus the minimum value of $f(l, \emptyset)$ for all possible l s. This can be computed as follows. The algorithm first sets 0 to f of the initial states then checks the states that can be reached with one SWAP or Bridge gate (and set 1 to f s of the states that have not yet seen), those reached with two SWAP and/or Bridge gates (and set 2 to the newly checked states), and so on. The algorithm terminates when it reaches a state whose set of blocking gates is empty. Note that each state is activated at most once because of the minimality of f . See Algorithm 1 for details. The optimal gate list \hat{L} can be obtained by recording the gates resolved by each of the swaps that update f at line 10 and traversing from the last state in the opposite direction.

4.2 Heuristic algorithm

We first review the original heuristic algorithm [3] and then describe how to extend it to handle both SWAP and Bridge gates.

The original *look-ahead* heuristic algorithm takes into account not only the blocking gates but also the other unresolved gates in the selection of a qubit pair to be swapped. The look-ahead algorithm is different from those based on the fixed-layer formulation [13, 15] in the sense that it does not require any definition of layers. The idea of the look-ahead mechanism is as follows. With regards to a layout l , for each unresolved two-qubit gate g we can compute the length of the shortest path between the two qubits of g as the minimal number of SWAP gates required to apply g . Thus, the number of SWAP gates of the layout l is proportional to the total length of the shortest paths of all unresolved two-qubit gates. Slightly modifying the layout l with swapping (q_i, q_j) , denoted as $\tilde{l}(q_i, q_j)$, may decrease the length of the shortest paths at some unresolved two-qubit gates; but it may also increase those at other unresolved gates. The look-ahead heuristic prefers modifying the layout so that the total length of the shortest paths is reduced.

The pseudocode of the look-ahead heuristic algorithm is shown in Algorithm 2, where the lines from

Algorithm 2 Look-ahead heuristic algorithm for MCGM

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1:  $C$ : a coupling graph,  $D$ : a dependency graph
2: Initialize blocking gates  $K$  as the gates with no in-edges in  $D$  and layout  $l$  as the given initial layout.

3: loop
4:   Run the gates complying with  $C$  and update  $K$ .
5:   if  $K = \emptyset$  then terminate
6:   Compute the swap score for each edge in  $C$ .
7:   Let  $(q_s, q_t)$  be the edge with the highest swap score.

8:   Let  $(b_{s'}, b_{t'}) \mapsto (q_s, q_t)$  be the current mapping in  $l$ .

9:   Let  $S \subseteq K$  be CNOT gates whose acting qubits has distance two in  $C$  for  $l$ .
10:  if  $S$  is not empty and the highest swap score  $< 1$  then
11:    Transform some  $g \in S$  acting on  $(q_s, q_t)$  in  $l$  into Bridge gate between  $(q_s, q_t)$ .
12:    continue
13:  end if
14:  if the swap of the mapping at  $(q_s, q_t)$  in  $l$  decreases  $\sum_{g \in K} SP(g, l)$  then
15:    Swap the mapping, i.e.,  $(b_{s'}, b_{t'}) \mapsto (q_t, q_s)$ .
16:  else
17:    Choose any gate  $\hat{g}$  in  $K$  and add swap gates that strictly decrease  $c(l, \{\hat{g}\})$  until  $\hat{g}$  is resolved.
18:  end if
19: end loop

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9 to 13 are for considering Bridge gates. Like the exact one, the heuristic algorithm also maintains a layout l and blocking gates K ; however, unlike the exact one, we assume that an initial layout is given. The heuristic algorithm updates K at the beginning of each loop. If K is empty, it terminates. Otherwise, it selects a qubit pair to be swapped on the basis of its swap *score*, i.e., the difference between the sum of the length of the shortest paths before and after swapping the qubit pair. Note that the selected qubit pair should be an edge of the coupling graph C . Let U be a subset of unresolved CNOT gates including the current K and $SP(g, l)$ be the length of the shortest path from the two qubits of g with regards to the layout l . The (swap) score of a qubit pair $(q_i, q_j) \in E_C$

with l and U is defined as follows:

$$\begin{aligned} \text{score}((q_i, q_j), l, U) &= c(l, U) - c(\tilde{l}(q_i, q_j), U), \\ c(l, U) &= \sum_{g \in U} \gamma(g) SP(g, l), \end{aligned}$$

where $\tilde{l}(q_i, q_j)$ denotes the layout after swapping (q_i, q_j) from l and $\gamma(g)$ denotes the weight of the shortest path of the gate g . To prioritize swapping a qubit pair reducing shortest paths of blocking gates and other unresolved gates close to them, we let $\gamma(g) = 1$ for $g \in K$ and $\gamma(g) = \alpha^{d(K, g)}$ ($0 < \alpha < 1$) for $g \notin K$, where $d(K, g)$ denotes the longest path length among the paths from $g' \in K$ to g . At each loop of Algorithm 2, SWAP gates are added at either line 15 or at line 17. The former always decreases the length of the shortest paths of blocking gates, while the latter always decreases the size of K . This guarantees that the algorithm terminates after a finite number of loops.

The algorithm can be extended to handle Bridge gates by defining the score for replacing a non-adjacent CNOT with a Bridge gate. Since a Bridge gate does not change the layout, we can define $\text{score}((q_i, q_j), l, U) = 1$ for any (q_i, q_j) such that $(q_i, q_j) = (l(b_{i'}), l(b_{j'}))$ for a CNOT gate acting on $(b_{i'}, b_{j'})$ and the distance between (q_i, q_j) is two. Such extension are depicted at the lines from 9 to 13 in Algorithm 2.

5 Experimental Results

We conducted two sets of experiments: comparing the effectiveness of our formulation against that of formulations with fewer commutation rules and one without Bridge gates, and evaluating the performance of our heuristic algorithm against those of state-of-the-art algorithms. Both were conducted on a laptop PC with an Intel Core i7-6820HQ 2.7 GHz and 16 GB memory.

5.1 Comparison to formulations with fewer commutation rules and one without Bridge gates

In the first set of experiments, we compared the optimal numbers of additional gates with our formulation to those with the other formulations; two formulations with fewer commutation rules, i.e. the fixed-layer and standard-DAG, and one without Bridge gates. We obtained the optimal numbers of additional gates by applying our exact algorithm discussed in Section 4–4.1. To obtain the optimal numbers for the formulations with fewer commutation rules, we added extra edges to the dependency graphs so that they represent the fixed layers and standard-DAG, and then we applied our exact algorithm to them. We used two sets of 10 random circuits with five or six qubits. Each circuit contained 100 gates in which each gate was either a R_z , H , or CNOT gate with probability of 25%, 25%, or 50%, respectively. Here H is a single-qubit gate called the Hadamard gate.

Table 1 compares additional gates for our formulation and the other formulations. Recall that each of SWAP and Bridge gate introduces three extra CNOT gates as in Fig. 2a and 2b, so the total number of additional CNOT gates is exactly three times the number of additional SWAP and Bridge gates. By comparing our formulation (Proposed) with the standard-DAG formulation (Std-DAG), we observed that Proposed had fewer numbers of additional gates. We certainly succeeded in reducing the numbers of additional SWAP and Bridge gates from standard-DAG formulation, which is slightly better than fixed-layer formulation (Fixed-layer) as expected, for each of the coupling architectures. By comparing Proposed with the original formulation without Bridge gates (No-Bridge), we can see that Bridge gates indeed improve optimality of the formulation. It is not surprising that the consideration of Bridge gates works best in LNN coupling architecture, which have leaves in the coupling graph. Unfortunately, the runtime of the exact algorithm grows exponentially with the number of qubits and gates; while all runs for 5-qubit instances are within 1 minute, but those for 6-qubit instances are around 12 minutes.

Table 1: Comparison of averages of optimal numbers of additional SWAP and Bridge gates of our formulation (in the Proposed column) and those of fixed-layer and standard-DAG formulation for two sets of 10 random circuits with five or six qubits. The average numbers of Bridge gates are stated in (\cdot) . The No-Bridge column lists the optimal numbers of SWAP gates from the original formulation [3]. ($|B|$: Number of qubits in circuit)

$ B $	Coupling	Fixed-layer	Std-DAG	Proposed	No-Bridge
5	ibmqx4	9.4 (3.4)	8.9 (2.6)	7.2 (1.1)	7.4
5	LNN	22.1 (6.3)	21.8 (7.0)	19.5 (4.4)	21.2
6	2×3	11.8 (1.7)	11.7 (2.0)	10.1 (1.4)	10.7
6	LNN	28.2 (6.3)	27.5 (8.0)	23.7 (5.3)	26.4

5.2 Comparison with other heuristic algorithms for larger circuits

In the second set of experiments, we evaluated the heuristic algorithm against two state-of-the-art heuristic algorithms. One is a randomized heuristic algorithm (called QRAND) implemented in Qiskit, which is a Python software development kit for quantum programming [23]. The other is an A*-based heuristic search algorithm (called ZPW) proposed by Zulehner et al. [15]. Their C++ implementation is available to the public, including their test circuit data, which originated from the RevLib benchmarks [25]. From their data, we chose 44 circuits with $\#\text{qubits} (|B|) \geq 10$ and $\#\text{gates} \leq 50,000$ for the experiment. For all the circuits, we computed the mappings to the IBM Q 16 Rueschlikon V1.0.0 (ibmqx3) coupling architecture [26]. We implemented our algorithm on top of Qiskit v0.6. We set the parameter $\alpha = 0.5$ and restricted the g of $d(K, g)$ to the gates within 10 steps from K .

The proposed heuristic algorithm outperformed QRAND and ZPW for all instances. See Table 2 for all results. The numbers of additional SWAP and Bridge gates in the mappings with the heuristic algorithm (Proposed) decreased by 10.0–72.3% (Avg. 53.2%) and 10.9–48.8% (Avg. 34.7%) from those of QRAND and ZPW, respectively. Even without Bridge gates (No-Bridge), in the mappings with commutation rules the numbers of additional SWAP gates decreased by 10.0–72.3% (Avg. 45.5%) and 7.1–42.1% (Avg. 23.8%) from those of QRAND and ZPW, respectively. From the columns of Proposed and No-Bridge, we can confirm that Bridge gates can find better mappings in almost all cases except for a few small circuits. The

numbers of additional gates decreased by 14.2% on average. This implies, in spite of larger search space due to the consideration of Bridge gates, the proposed heuristic algorithm can efficiently explore it to find better solutions. All runs of heuristic algorithms were less than 15 minutes.

Since we needed to give the initial layout l_0 for our algorithm and QRAND, we used the trivial layout $l_0 : (b_1, \dots, b_{|Q|}) \mapsto (q_1, \dots, q_{|Q|})$. The number of additional gates may possibly be further reduced by finding a good initial layout for the heuristics. For our algorithm, we added a post-processing to remove leading useless SWAP gates by changing the given initial layout. The reverse traversal technique by Li et al. [19] can be applied instead of the post-processing, and to find a better initial layout.

6 Conclusion

We addressed the problem of mapping quantum circuits to NISQ computers, whose operations are limited by their coupling architecture, with as few additional gates as possible. Our proposed solution to the mappings is to use gate commutation rules and gate transformation rules in the form of SWAP and Bridge gates. Many previous studies did not consider such gate commutation rules or Bridge gates to reduce additional gates in the mappings. We developed exact and heuristic algorithms that take advantage of such rules. Comparing them with the state-of-the-art circuit mapping algorithms, we demonstrated that our proposed algorithms can find better mappings with fewer additional gates for the circuits of a commonly used benchmark dataset.

Table 2: Comparison of numbers of additional SWAP and Bridge gates in mappings with our proposed heuristic algorithm (Proposed), its original one without Bridge gates (No-Bridge), as well as QRAND and ZPW for circuits with 10 to 16 qubits from RevLib benchmark. The compositions of the numbers of SWAP and Bridge gates of Proposed are listed in the (#SWAP+#Bridge) column. The runtime of Proposed are listed in the Time column. ($|B|$: Number of qubits used in circuit)

Circuit name	$ B $	#gates	QRAND	ZPW	No-Bridge	Proposed	(#SWAP+#Bridge)	Time [s]
mini_alu_305	10	173	80	46	40	41	(28+13)	0.5
qft_10	10	200	82	40	33	33	(33+0)	1.9
sys6-v0_111	10	215	116	67	46	34	(22+12)	0.6
rd73_140	10	230	100	58	49	34	(23+11)	0.6
ising_model_10	10	480	18	14	12	12	(12+0)	0.7
rd73_252	10	5,321	2,054	1,541	1,212	999	(644+355)	20.1
sqn_258	10	10,223	4,060	2,867	2,254	1,875	(1,108+767)	57.5
sym9_148	10	21,504	8,001	5,907	4,456	3,770	(1,856+1,914)	237.5
max46_240	10	27,126	10,833	8,012	5,905	4,932	(2,573+2,359)	469.8
wim_266	11	986	385	269	225	155	(65+90)	4.8
dc1_220	11	1,914	721	548	446	329	(154+175)	6.4
z4_268	11	3,073	1,200	907	718	600	(364+236)	11.2
life_238	11	22,445	9,181	7,209	5,264	4,539	(2,638+1,901)	268.8
9symml_195	11	34,881	14,470	10,682	8,124	6,630	(3,909+2,721)	684.1
sym9_146	12	328	173	85	66	51	(33+18)	0.9
cm152a_212	12	1,221	423	341	269	175	(76+99)	4.3
sqrt8_260	12	3,009	1,263	956	728	587	(377+210)	11.8
cycle10_2_110	12	6,050	2,701	1,856	1,518	1,192	(725+467)	27.9
rd84_253	12	13,658	5,817	4,271	3,271	2,784	(1,777+1,007)	108.9
rd53_311	13	275	162	98	77	68	(53+15)	1.9
ising_model_13	13	633	28	28	18	18	(18+0)	1.1
suar5_261	13	1,993	797	605	422	446	(285+161)	6.0
radd_250	13	3,213	1,347	951	721	623	(382+241)	11.3
adr4_197	13	3,439	1,529	1,044	806	675	(422+253)	12.6
root_255	13	17,159	7,172	5,417	4,070	3,516	(2,160+1,356)	152.4
dist_223	13	38,046	16,548	11,930	9,326	7,879	(4,952+2,927)	809.2
0410184_169	14	211	88	76	44	45	(35+10)	0.6
sym6_316	14	270	123	70	65	58	(41+17)	0.8
cm42a_207	14	1,776	677	494	402	321	(207+114)	8.9
cm85a_209	14	11,414	4,906	3,598	2,694	2,370	(1,395+975)	75.8
clip_206	14	33,827	14,845	11,011	8,187	6,855	(4,185+2,670)	624.1
sao2_257	14	38,577	16,974	12,511	9,188	7,479	(4,691+2,788)	780.2
rd84_142	15	343	192	103	67	56	(39+17)	1.0
misex1_241	15	4,813	1,844	1,520	1,216	1,067	(602+465)	21.8
square_root_7	15	7,630	3,243	2,369	1,504	1,546	(1,393+153)	46.7
ham15_107	15	8,763	3,635	2,552	1,979	1,685	(980+705)	50.0
dc2_222	15	9,462	4,112	2,933	2,326	1,798	(1,099+699)	58.5
co14_215	15	17,936	8,423	6,566	4,318	3,294	(1,780+1,514)	183.9
cnt3-5_179	16	175	69	54	38	35	(23+12)	0.5
cnt3-5_180	16	485	183	124	98	88	(49+39)	3.0
qft_16	16	512	296	117	82	82	(82+0)	4.8
ising_model_16	16	786	20	24	18	18	(18+0)	1.3
inc_237	16	10,619	4,351	3,138	2,542	2,098	(1,198+900)	68.3
mlp4_245	16	18,852	8,104	6,212	4,547	3,988	(2,495+1,493)	179.7

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removing the edge (s, t) if there exists a path from s to t in the graph with reduced edge set excluding (s, t) .

A Construction of dependency graph

We give the algorithm for constructing dependency graph in Algorithm 3. Because it is specifically tailored to the commutation rules shown in Fig. 4, the commutation rules are not stated as input to the algorithm.

Algorithm 3 Constructing dependency graph

IN: List of gates L in a given logical circuit

OUT: Dependency graph D

- 1: $V_D \leftarrow \{g \mid g \in L\}$ // node set of D
 - 2: $E_D \leftarrow \emptyset$ // edge set of D
 - 3: **for all** gate pair (g_i, g_j) such that $i < j$ in L **do**
 - 4: **for all** common acting qubit b of g_i and g_j **do**
 - 5: $S \leftarrow \{s \mid \text{symbol } s \text{ between } g_i \text{ and } g_j \text{ on } b\}$
 - 6: **if** $S \not\subseteq \{R_z, \bullet\}$ and $S \not\subseteq \{R_x, \oplus\}$ **then**
 - 7: $E_D \leftarrow E_D \cup \{(g_i, g_j)\}$
 - 8: **end if**
 - 9: **end for**
 - 10: **end for**
 - 11: **return** (V_D, E_D)
-

Note that the dependency graph obtained by the algorithm is redundant. If necessary, the minimal set of edges can be obtained by checking each of the edges in E_D and