Analytical and Simulation Studies of Failure Modes in SRAM's Using High Electron Mobility Transistors

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Abstract—**Gallium Arsenide memories, which are now beginning to be used commercially, are subject to certain unusual parametric faults, not normally seen in silicon or other memory devices. This paper studies the behavior of Gallium Arsenide High Electron Mobility Transistor (HEMT) memories in the presence of material defects, processing errors and design errors to formulate efficient testing schemes. All defects and errors are mapped into equivalent circuit modifications and the resulting circuits are analyzed and simulated to observe the fault effects. Certain complex pattern-sensitive faults described in the testing literature are not observed at all, while certain other faults which have not been previously studied, are observed. It is shown that by slightly modifying and reordering existing test procedures, all faults in these RAM's can be adequately tested.**

Keywords: **Parametric testing, fault modeling, Gallium Arsenide, static RAM.**

I. Introduction

THE NEED FOR high-speed memories, with subnanosecond access times, has led to the development of Gallium Arsenide (GaAs) random-access memories. GaAs devices provide the fastest switching elements available today, not counting superconducting devices which operate at cryogenic temperatures. However, GaAs circuits are preferred to superconductor circuits because of their compatibility with ECL and other silicon logic families and their ability to operate at room temperature instead of at cryogenic temperatures. While several different high-speed GaAs circuits have been developed ([2] is a good state-of-the-art survey), our primary concern here is with GaAs memories. Notomi *et al.* [27] have described a 1-Kbit SRAM using GaAs High Electron Mobility Transistors (HEMT's) with 500 ps access time, clearly outperforming ECL and CMOS memories in terms of speed. They have also pointed out a major problem with GaAs memories—the variation of address access time over the whole address space is 150 ps, or 30% of the nominal access time. This anomaly has been attributed to process variations and design problems which are not normally encountered in silicon RAM's. Parasitic resistances are a much more serious problem in GaAs because of the higher currents and lower operating voltages. Leakage currents are much larger relative to the operating currents and the voltage margins are low. Hence GaAs devices have a number of distinct failure modes, which lead to faults unlike those commonly seen in silicon. This paper explores several of these failure modes and the consequent fault models and identifies parametric test procedures for these faults.

General test procedures for RAM's were developed in the past [1], but they were found inadequate for testing newer silicon RAM's in two ways; they did not cover all classes of parametric faults and they wasted time on improbable faults [11], [25]. These problems led researchers to study the physical causes of silicon RAM failures to devise efficient new ways of testing these RAM's. Dekker *et al.* [11] studied faults in silicon SRAMs, based on the inductive fault analysis methods of [15], [32] and the realistic fault models of [22]. Mazumder [25] studied failure mechanisms in silicon DRAM's and proposed efficient test algorithms based on the observed mechanisms.

Since the basic structure and the processing sequence of GaAs devices are different from those of silicon MOSFETs, the failure mechanisms are also different. Systematic variations in process parameters, such as threshold voltage across a wafer and across a chip, are observed more prominently in GaAs than in MOS. Moreover, new failure modes such as inter-electrode resistive path formation [12], [13] have been observed in GaAs. The objective of this paper is to study the causes of faults in GaAs SRAM's and to identify efficient algorithms for testing for the presence of these faults based on a clear understanding of the fault mechanism. Process and design related faults are studied and efficient parametric test procedures are proposed.

This paper describes how the failure modes of GaAs circuits lead to different types of faulty behavior in SRAMs. Several kinds of pattern-sensitive faults [16], [36] are observed. Some of these faults cannot be detected by the efficient algorithms of [36] and general algorithms for pattern-sensitive faults [16] have exponential time complexity; simpler test procedures are identified for these

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specific pattern sensitive faults. Variations in process parameters are shown to result in delay faults. Data retention faults are shown to have an entirely new mechanism, apart from the stuck-open mechanism observed in silicon [11], [20]. Parametric test procedures [25] for these faults are proposed.

II. High Electron Mobility Transistors

HEMT's, also known as MODFET's (Modulation doped FET's) or TEGFET's (Two dimensional Electron Gas FET's) are ultra-high-speed switching devices whose development came about as a result of advances in molecular beam epitaxy (MBE) that allowed heterostructures of GaAs and AlGaAs to be grown epitaxially [4], [5], [17]. HEMT's are field effect devices similar to MESFET's or JFET's and have the added advantage of being much faster. The increased speed results from the increased mobility of the electrons in the HEMT. In a regular MESFET or JFET channel, the mobility of the electrons is limited by impurity scattering and the number of impurity atoms in the conducting layer is high because it is doped heavily for good conductivity. In HEMT's, the electrons in the conducting layer of GaAs (see Fig. 1) come from the adjacent *n*-doped AlGaAs layer due to the properties of the AlGaAs/GaAs heterojunction. Since the GaAs layer is not doped, impurity scattering is minimized and the electron mobility can potentially go up to 10^5 $cm^2/V \cdot s$ at 77 K and of the order of 10^4 $cm^2/V \cdot s$ at room temperature. This is to be contrasted with the electron mobility of 500 $cm^2/V \cdot s$ in silicon FET's.

The operating voltages and especially the output voltages of circuits feeding other HEMT circuits are limited by the fact that when the gate-source voltage increases above the Schottky barrier voltage of the gate, the gate begins to conduct and clamps the gate voltage at 0.8–0.9 V above the source voltage. Hence the typical HEMT direct coupled logic circuit has a supply voltage range of 1 V with a logic high of 0.8 V and a logic low of 0.1 V. The drain–source current flowing through a HEMT when the gate-source voltage is at logic 0, the leakage current, is about 1/200 of the current through the HEMT when the gate–source voltage is at logic 1; in a typical silicon NMOS logic circuit this ratio is about 1/10 000. Hence leakage/subthreshold currents are much more likely to cause errors in HEMT RAM's.

2.1. Defects in GaAs

Fault modeling for GaAs RAM's starts with the study of material and processing defects. This study is then used to generate plausible circuit errors in the basic memory circuits; the observed erroneous behavior of the memory is a result of the errors in the component circuits. Reliability and aging studies [24] of HEMT's reveal the parametric and catastrophic failure modes of these transistors as a result of stress and aging. Fault effects of these failure modes may be studied to develop efficient tests for periodically testing these memories over their lifetime of operation. Study of the failure mechanisms also suggests ways to test for the presence of the resultant errors at the behavioral level.

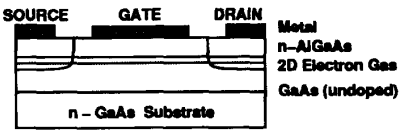

Fig. 1. Structure of HEMT.

The defects in GaAs wafers can be classified as primary and secondary defects [37]. Primary defects are related to the material itself. Compositional purity, control of stoichiometry and crystalline perfection are some of the factors affected by these primary defects. These defects manifest themselves at the device level in the form of threshold voltage variation, mobility degradation and trapped charges. Deep donor levels associated with DX centers in the AlGaAs layer of the HEMT play a major role in electron capture and release [8], leading to various problems such as kinks in the V–I characteristics of the HEMT. Trap related problems result in threshold voltage and transconductance shifts with temperature changes [18]. Surface defects known as oval defects are a by-product of the material growth process [3]. These defects range in size from submicron levels to a few microns. The effect of an oval defect in the gate region of a HEMT is to prevent the transistor from turning off.

Variation of the threshold voltage over the wafer has always been a major problem in GaAs. With improved processing technology, this problem can be alleviated to some extent but never eliminated completely. Whereas the threshold voltage variation across the wafer was in the range of a hundred millivolts some time ago [10], [21], the current state-of-the-art processes offer much better control over the threshold voltage. However run-to-run reproducibility is an intrinsic problem in the MBE process and variation of threshold voltage across wafers is larger [39]. Typical state-of-the-art parameters for threshold voltage over a wafer are [4]:

$$V_{TE} = 0.278 \text{ V}; \quad \sigma(V_{TE}) = 11.3 \text{ mV}$$

$$V_{TD} = -0.602 \text{ V}; \quad \sigma(V_{TD}) = 14.2 \text{ mV}.$$

Secondary defects are introduced during wafer processing in the form of surface and sub-surface damage. These defects are responsible for most of the observed faults in the circuits, such as stuck-at-faults, bridging faults, etc.

Ohmic contact degradation and interdiffusion of gate metal with GaAs have been reported [13]. Interdiffusion of gate metal with GaAs has been observed [13] to cause the ON resistance of the transistor to increase, the saturation current to decrease and the magnitude of the pinch-off voltage to decrease. Such a fault can also short the gate to the channel of the transistor. Gate metal diffusion and electromigration are the major failure mechanisms in GaAs [14], [30]. It has been reported that a major failure mode for depletion-mode transistors is the development of interelectrode metallic paths due to electromigration

and processing defects [12]. Another defect that has been reported [28] is via fracturing.

All the above errors are permanent or 'hard' errors; some recent work [38] shows that GaAs *IC*'s are more susceptible than silicon *IC*'s to single-event upset when alpha particles strike the device [29]. This shows that the reliable operation of a GaAs SRAM requires on-line error detection and correction circuits.

III. RAM Cell Design and Fault Analysis

One of the principal issues in memory design is design centering. This is the process of choosing nominal design parameters so that they lie in the 'center' of their respective tolerance intervals so as to maximize yield. Statistical circuit design techniques [34], [35], [40] have been used in the past to solve the design centering problem. Parameters such as the threshold voltage and transistor length vary across the wafer, and across the chip. If the distribution of the parameters is known in terms of the type of distribution, its mean and its variation, then statistical design attempts to assign nominal values m_{nom} to these parameters such that the design works satisfactorily for all actual values of the parameter m between m_{min} and m_{max}, where the values of m_{min} and m_{max} are chosen to maximize the probability of the actual value m being within the range. Hence statistical design and yield optimization involve the computation of circuit parameters for various values of process parameters and the computation of the sensitivities of the design parameters with respect to various process parameters in order to compute better nominal values starting from some given value.

Our approach to fault modeling is complementary to this design centering approach; starting from a nominal design value, the fault effect of parameter variations is studied. Various other defects such as resistive bridging, missing devices and so on, are mapped on to equivalent parameter variations where possible, to present a simple, unified view of the problem in terms of parametric faults. Parametric-yield and catastrophic-yield are the two basic yield figures which measure the loss due to parameter variation and catastrophic defects (missing device, shorts, open circuits, etc.) respectively [23]. These figures are usually obtained separately in yield estimation studies. The fault modeling approach presented here shows how the fault effect of catastrophic defects can be mapped onto equivalent parameter variations and vice versa. Analysis of a single good circuit is sufficient to provide an understanding of the fault effects of both parameter variations and catastrophic defects as demonstrated here.

3.1. HEMT Models

The basic memory cell consists of two cross-coupled inverters connected to complementary *bit* and $\overline{bit}$ lines via pass gates (see Fig. 2). This circuit is analyzed with the help of a simple equivalent circuit model, to identify the fault effects of variations in element parameters. This simplified analysis is then verified with the help of SPICE simulations using a more complex numerical model [42]. The HEMT model is shown in Fig. 3 and is a simplified version of the model presented in [42] and used in the simulator [41]. Typically the gate–source capacitance C_{GS} is the dominant capacitance term; C_{GS} is about five times C_{GD} and ten times C_{DS} [33]. The dependent current source equations are as follows in the simplified model:

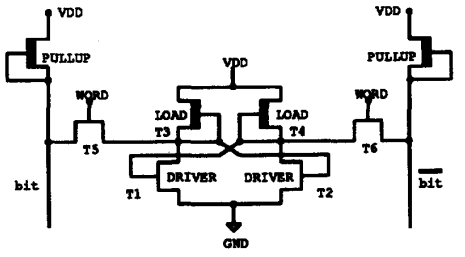

Fig. 2. Basic RAM cell.

$$\textit{Cutoff}\,(V_{GS} < V_T): \quad I_{DS} = 0 \tag{3.1}$$

$$\textit{Saturation}\,(V_{GS} \geq V_T;\ V_{GS} - V_T < V_{DS}):$$

$$I_{DS} = I_{DSAT} = \beta(V_{GS} - V_T)^2 \tag{3.2}$$

$$\textit{Linear}\,(V_{GS} \geq V_T;\ V_{GS} - V_T > V_{DS}):$$

$$I_{DS} = I_{DSAT} \tanh(\alpha V_{DS}) \tag{3.3}$$

where $\beta = K(W/L)$, and W and L are the width and length respectively of the HEMT. Here K and α are constants and the capacitances are assumed to be constant over the range of operation, even though the capacitances are actually voltage dependent to a large extent. The validity of this assumption is verified by simulating the circuits with the detailed HEMT model of [42] (see Fig. 4). The constant α has the dimensions of V^{-1}, while β and K have dimensions of A/V^2.

3.2. read and write Operations

The memory cell stores a value 0 (1) with a voltage V_H on the node adjacent to the $\overline{bit}$ line and a low voltage V_L on the node adjacent to the *bit* line. Prior to a *read* operation the *bit* and $\overline{bit}$ lines are precharged to V_H. Then the *word* line goes high, turning on the pass transistor connecting the cell node which is at V_L to the adjacent *bit* ($\overline{bit}$) line. The memory cell is designed so that the cell does not change state during the *read* operation, the *read/write* operations are fast and the cell area is minimized. The cell storage node voltages V_H and V_L are determined in the static case (when the access transistors are off) by the current ratios of the cell load and driver transistors and in the dynamic case by the sizes of the *bit* line pull-up transistors, the *bit* line capacitances and the access (pass) transistor currents.

Analysis of the noise margins and stability figures of silicon RAM cells consisting of four MOSFET's and two resistive loads has been performed in the past [6], [9], [31]. However, these analyses assume that the cell load

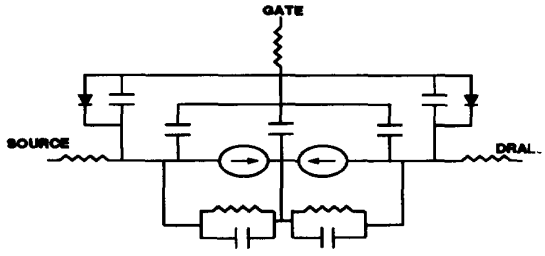

Fig. 3. HEMT equivalent circuit model.

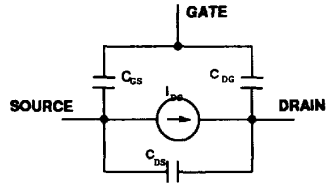

Fig. 4. Simplified equivalent circuit for HEMT.

resistor value is so high that the current through the resistor is not enough to charge the cell nodes in a single access cycle [9] or that the cell voltage V_L is greater than the threshold voltage of the FET so that the driver FET's of both inverters are conducting [31]. While these studies correctly model the behavior of silicon RAM cells with a resistive load, they do not accurately represent the behavior of HEMT RAM cells with depletion mode loads and samll operating voltages. Our analysis is based on observations of the operating points of HEMT's in cells corresponding to published HEMT RAM designs [19]. In the static case, the driver HEMT whose drain is at V_H is turned off and the depletion loads provide enough current to recharge the cell nodes every cycle.

read operation: Analysis of the *read* operation starts with the assumption that the cell storage node connected to the *bit* line (see Fig. 2) is at logic 0 and the node connected to the $\overline{bit}$ line is at logic 1. The *bit* and $\overline{bit}$ lines are precharged to V_H and the *word* line is at V_H. The corresponding operating points of the various transistors are as follows: the two depletion mode pull-up transistors on the *bit* and $\overline{bit}$ lines are in the linear region since $V_{GS} = 0\ V$, $V_T = -0.6V$ (typical) and $V_{DS} = 0.1\ V$. The access transistor T5 is in the linear region, the load transistor T3 is in saturation, the driver transistor T1 is in the linear region, the driver transistor T2 is in cutoff, the load transistor T4 is in the linear region and the access transistor T6 is in the linear region. During a correct *read* operation, the *bit* line is discharged by about 0.2 V and the sense-amp (not shown) converts difference between the *bit* and $\overline{bit}$ lines into a proper output voltage level. Since the $\overline{bit}$ line voltage V_H does not change significantly during the *read* operation on the cell storing a 0, it is sufficient to consider the devices connected to the *bit* line, T1, T3, T5 and the *bit* line pull-up. The transistor T2 is replaced by an equivalent load capacitor and the resultant circuit is shown in Fig. 5.

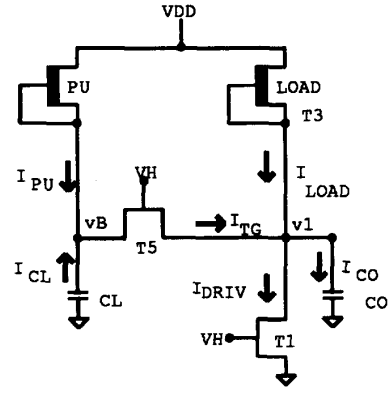

Fig. 5. Devices involved in the read operation.

Static analysis of the memory cell provides some information on the regions of correct operation. The aim of this analysis is to determine the range of V_{TE} and V_{TD}, the enhancement and depletion mode threshold voltages, for which the cell storage node voltage at the end of the *read* operation does not increase above the threshold voltage of the transistor T2. The capacitors are ignored and the currents through the various transistors shown in Fig. 5 are equated using Kirchoff's current law at the two nodes corresponding to the *bit* line and the cell storage node. The resulting equation for the cell storage node voltage is[1]

$$V_1 = \frac{(\beta'_{PU} + \beta_{LO})V_{TD}^2}{\alpha\beta_{DR}(V_H - V_{TE})^2} \tag{3.4}$$

where $\beta'_{pu} = \beta_{Pu} * \tanh(\alpha * v)$ and v, the drain-source voltage of the pullup, is about 0.1 V for the entire region of interest. A plot of the variation of V_1 with V_{TD} and V_{TE} is shown in Fig. 6, along with a plot $V_v = V_{TE}$. It can be seen that over a 3σ variation about the mean design values of the threshold voltages, the value of V_1 is less than $V_v (= V_{TE})$ for this particular design with a 3-μm/0.5-μm driver, a 0.5-μm/3-μm load, a 1.5-μm/0.5-μm access transistor, a 1.5-μm/0.5-μm pull-up and a 200 fF *bit* line capacitance.

If the time to discharge the *bit* line is too high, or the time to pre-charge the *bit* line is too high, the RAM cannot operate at its stated speed. Static analysis cannot catch these errors and hence a more detailed analysis taking into account *bit* line and storage node capacitances is required. The KCL equations may be written as follows, simplifying the HEMT model to just a single current source except for the transistor T2 which is replaced by its equivalent gate-source capacitance. This assumption is justified as long as the capacitor currents in the ON transistors are much less than the drain-source currents, as confirmed by subsequent simulations.

$$I_{T5} = I_{PU} + I_B \tag{3.5}$$

$$I_{T5} + I_{LO} = I_{DR} + C_O \frac{dV_1}{dt} \tag{3.6}$$

[1] α has the dimensions of V^{-1}.

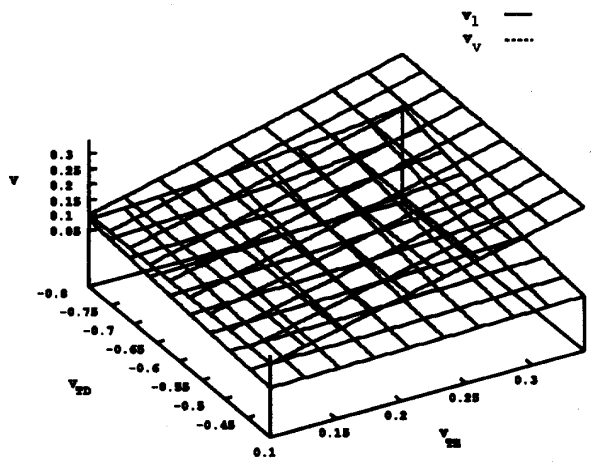

Fig. 6. Variation of V_1 with threshold voltage.

where $I_B = C_L\,(dV_B/dt)$ and the other currents are defined as before. The following differential equation for V_1 can then be derived.

$$C_O \frac{dV_1}{dt} + \beta_{DR}(V_H - V_{TE})^2 \alpha V_1 - \beta_{T5}(V_H - V_{TE} - V_1)^2 - \beta_{LO} V_{TD}^2 = 0 \quad (3.7)$$

This equation can be solved to give the time t as a function of the cell storage node voltage V_1.

$$t = C_O(C' - f(V_1)) \quad (3.8)$$

$$f(V_1) = A_1 \log (V_1 - u_1) + A_2 \log (V_1 - u_2) \quad (3.9)$$

$$C' = f(V_0) \quad (3.10)$$

$$u_1 = \frac{-B - \sqrt{B^2 - 4AC}}{2A} \quad (3.11)$$

$$u_2 = \frac{-B + \sqrt{B^2 - 4AC}}{2A} \quad (3.12)$$

$$A_1 = \frac{-1}{\sqrt{B^2 - 4AC}} \quad (3.13)$$

$$A_2 = \frac{1}{\sqrt{B^2 - 4AC}} \quad (3.14)$$

$$A = -\beta_{T5} \quad (3.15)$$

$$B = (V_H - V_{TE})(\beta_{DR}\alpha(V_H - V_{TE}) + 2\beta_{TG}) \quad (3.16)$$

$$C = -\beta_{LO} V_{TD}^2 \quad (3.17)$$

If V_1 reaches the value V_{TE} before the *read* phase is complete, then there is a cell stability problem. However, in the worst case *read* situation, the cell is selected and the chip is enabled for an indefinite time and the static stability situation holds. More importantly, this analysis is used to predict the discharge time of the *bit* line. The *bit* line is pre-charged to about 0.9 V and is discharged to between approximately 0.75 and 0.7 V during the *read* operation. At the same time, when the cell is stable, the cell storage node is almost constant at about 0.1 V, though it does change slightly, as shown by the previous analysis. Hence the KCL equation for the *bit* line is written assuming the storage node voltage V_1 to be constant.

$$\beta_{PU} V_{TD}^2 \alpha (V_H - V_B) - C_L \frac{dV_B}{dt} = \beta_{TG}(V_H - V_{TE} - V_1)^2 \quad (3.18)$$

This can be solved with the initial condition $V_B = V_H$ to give

$$V_B = K_4 e^{K_0 t} - \frac{K_1}{K_0} \quad (3.19)$$

$$= \log \left(\frac{V_B + \frac{K_1}{K_0}}{V_H + \frac{K_1}{K_0}} \right) \Bigg/ K_0 \quad (3.20)$$

$$K_0 = -\beta_{PU} V_{TD}^2 \alpha / C_L \quad (3.21)$$

$$K_1 = -\beta_{TG}(V_H - V_{TE} - V_1)^2 / C_L + \beta_{PU} V_{TD}^2 \alpha V_H / C_L \quad (3.22)$$

$$K_4 = V_H + K_1/K_0. \quad (3.23)$$

Fig. 7 shows the stable and unstable regions of operation and the *read*-error regions due to speed problems, as a function of β_{PU} and β_{TG} as the beta values vary from 50% to 200% of their nominal values.

write operation: Assume without loss of generality that the cell node connected to the *bit* line stores a 1 and the node connected to the $\overline{bit}$ stores a 0. Then the *write* operation attempts to flip the cell state by driving the *bit* line low so that T2 (see Fig. 2) is turned off while the $\overline{bit}$ line is driven high so that T1 is turned on. Since the load (pull-up) transistor of the cell is relatively weak compared to the cell driver, it is easier for a *bit* line driver transistor to pull the cell node at logic 1 to a low voltage than for the *bit* line pull-up to pull the cell node at logic 0 to a high level V_H. Hence the analysis focuses on the circuits that cause the originally high cell node to be pulled low; the transistors connected to the $\overline{bit}$ line are replaced by a single capacitor loading the left half of the memory cell—the equivalent circuit is shown in Fig. 8. The cell load transistor T3 is initially in the linear region and finally goes to saturation. The cell driver T2 goes from cut-off to linear while the access transistor T5 goes from saturation to linear. The *write* operation starts after the *bit* line is discharged and the *word* line goes high, turning on T5. The *bit* line driver T_{PD} is linear. The currents through the transistors and the KCL equations are as follows:

$$I_{LO} = I_{TG} \quad (3.24)$$

$$I_{PD} = I_{PU} + I_{PU2} + I_{LO} \quad (3.25)$$

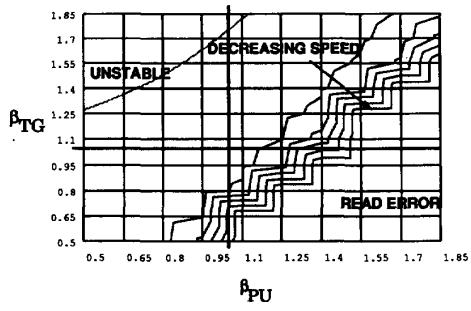

Fig. 7. Read error as a function of pull-up (PU) and access transistor (TG) betas.

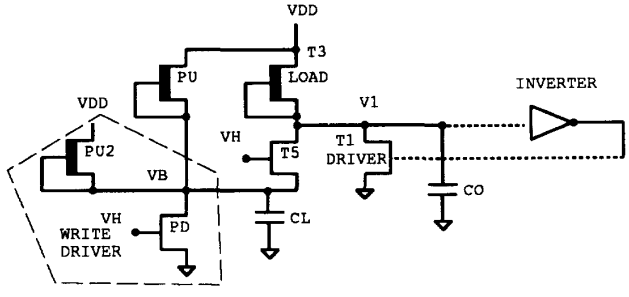

Fig. 8. Simplified circuit for analyzing the write operation.

$$I_{PD} = \beta_{PD}(V_H - V_{TE})^2 \tanh(\alpha V_B) \quad (3.26)$$

$$I_{TG} = \beta_{TG}(V_H - V_{TE} - V_B)^2 \cdot \tanh(\alpha(V_1 - V_B)) \quad (3.27)$$

$$I_{PU} = \beta_{PU} V_{TD}^2 \quad (3.28)$$

$$I_{PU} = \beta_{PU2} V_{TD}^2. \quad (3.29)$$

By approximating $\tanh(x)$ to x, the above equations can be solved to give

$$V_B = \frac{(\beta_{PU} + \beta_{PU2} + \beta_{LO})V_{TD}^2}{\beta_{PD}\alpha(V_H - V_{TE})^2} \quad (3.30)$$

$$V_1 = \frac{\beta_{LO} V_{TO}^2}{\beta_{TG}(V_H - V_{TE} - V_B)^2\alpha} + V_B. \quad (3.31)$$

V_1 should be less than V_{TE} for the cell to flip to the right state. Fig. 9 shows the predicted regions of *write* error as a function of the threshold voltages. Dynamic analysis of the *write* operation can be done in a similar fashion, by considering the capacitor currents as in the *read* analysis and augmenting the circuit to include the write-driver pullup on the other side ($\overline{bit}$) and the write access transistors as well. The analysis is further complicated by the fact that the operating region of the access transistor and the cell load transistor change during this process and these transitions must be properly sequenced. Hence the detailed calculations are not shown here and instead the final results based on circuit simulations are presented in the next section.

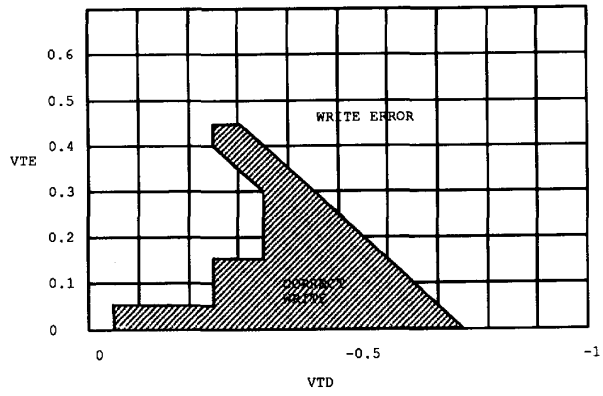

Fig. 9. Write error as a function of threshold voltages.

3.3 *Simulation Results: Design- and Process-Related Errors*

The memory cell was simulated with different values of process and design parameters such as transistor widths and threshold voltages. It was observed that these variations affected device performance in two ways—either the circuit became dysfunctional or it operated at a much lower speed. With proper design centering, the variation in device performance with process variations could be minimized, but the main focus of the research was on the identification of the fault effects.

The following parameters of a HEMT SRAM were varied directly or indirectly—V_T(enh), V_T(dep), β (for various transistors), and the results plotted (see Fig. 10). The nominal parameters of the cell were: $W_{TG} = 2$ μm; $W_{PU} = 1$ μm; $W_{DR} = 4$ μm; $W_{LO} = 2$ μm; $L = 1$ μm (for all transistors).

Table I shows the circuit behavior when the threshold voltages of the depletion- and enhancement-mode transistors are varied. The nominal values are $V_{TE} = 0.2$ V and $V_{TD} = -0.6$ V. As the absolute values of V_{TE} and V_{TD} are increased the delay increases as predicted, finally resulting in erroneous operation. When the enhancement mode threshold V_{TE} is reduced to nearly 0 V erroneous operation is observed as the enhancement mode transistors cannot be turned off. The results from simulation are tabulated below (Table I) and are seen to be in good agreement with the predictions from the analysis based on simplified models.

3.4. *Simulation Results: Design-Related Errors*

Fig. 10 shows the effect of varying the widths of the load transistor, the transmission gate, the driver transistor and the *bit* line pull-up transistor. β is directly proportional to the ratio of the width W of the transistor to its length L. In this design, all transistors have the same length based on minimum allowed feature size to make the transistors as fast as possible. Hence the beta ratio becomes just the ratio of the transistor widths (approximately, ignoring higher order effects). The first experi-

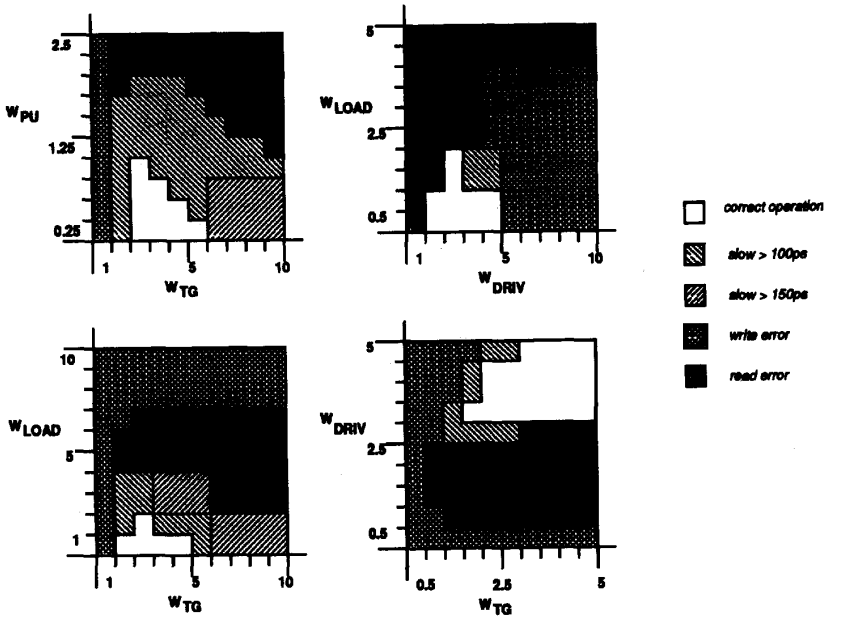

Fig. 10. Effect of parameter variations: simulation results.

TABLE I
THRESHOLD VOLTAGE VARIATION

V_{TD}	V_{TE} = 0.1 V	V_{TE} = 0.3 V	V_{TE} = 0.5 V	V_{TE} = 0.6 V
−0.1 V	Error	OK	OK	Error
−0.3 V	OK	OK	OK	Delay > 100 ps
−0.5 V	OK	Delay > 100 ps	Delay > 100 ps	Error
−0.7 V	Delay > 100 ps	Delay > 150 ps	Error	Error
−0.9 V	Delay > 150 ps	Error	Error	Error

ment varies the widths of the transmission gate and the load. From the figure, it can be seen that correct operation occurs only for a small range of values of W for the transmission gate and the load. If the width of the load transistor exceeds a certain value, the circuit becomes faulty. This is due to the fact that at this point the load transistor becomes much wider than the driver transistor and hence the inverter operation is itself faulty (the output high and low levels of the inverter are not within allowed limits). When the load transistor becomes wide (but not wide enough to cause malfunction), its gate capacitance increases, causing the circuit to slow down. When the transmission gate becomes too wide, the speed decreases as predicted by the analysis.

The next experiment varies W_{PU} and W_{TG}. It can be seen that the circuit operates as desired only for a small range of values. When the transmission gate is very small, the time taken to charge the cell node during a *write* operation and to discharge the *bit* line during a *read* operation become too large for correct operation, as expected. When the pull-up transistor becomes too large it prevents the *bit* line from discharging during a *read* operation, resulting in *read* error. When the pull-up transistor is much smaller than the transmission gate and the width of the transmission gate is increased, the *read* time increases as predicted.

For small values of W_{TG} where W_{TG} is not much bigger than W_{PU}, increasing W_{TG} while keeping W_{PU} constant improves the speed of operation, according to the analysis. The map showing the effect of varying W_{DRIV} versus W_{TG} clearly shows this improvement in speed with increasing W_{TG} for small W_{TG}. This map and the map plotting W_{DRIV} versus W_{LOAD} show that as the width of the driver transistor is increased the speed of the *read* operation increases but beyond a certain point the extra gate capacitance causes the *write* operation to fail. The analyses and simulation results show that the main effect of process variations, of minor errors causing width variations, and of design errors, is to reduce the operating speed and beyond a certain value, cause *read* and *write* errors.

Device Mismatches and Temperature Effects: When matched devices are used as in the differential input stage of the sense amplifier or in the memory cell itself, variation of device parameters can cause erroneous operation due to mismatching. However the intra-chip or intra-die variation of parameters is very small [2] and does not affect proper circuit operation adversely. Simulations show that a V_{TE} mismatch of 0.3 V is required for wrong

latching of the memory cell; the typical variation actually seen is of the order of a few millivolts. Similarly the extent of the mismatch in transistor widths required to cause an error is equal to the nominal width of the transistor. These extreme conditions are more properly categorized as catastrophic failures rather than parameter variations. The effect of catastrophic failures is studied in the next section.

As the operating temperature of the device increases, the electron mobility decreases and parameters such as threshold voltage experience shift [7]. While the temperature dependence of MESFET's is well defined in MESFET circuit simulators, there are no widely accepted temperature dependent HEMT models and the HEMT simulator [42] assumes the operating temperature is 300 K. Hence temperature effects must be approximated by variations of other parameters such as threshold voltage, β and so on.

IV. Catastrophic Failure Modes

The process and material defects discussed in the previous sections may lead to the following circuit modifications.

- Resistive paths between transistor electrodes/ increased leakage current.
- Bridging of metal lines—shorts between two adjacent signals.
- Transistors stuck-open.

Each transistor in the circuit could thus be stuck-open, or have a resistive path between any two of its electrodes. Any two lines in the circuit that lie within some arbitrary distance from each other in the layout, could be bridged. All these aberrations considered either individually or in groups, lead to a large number of modified, 'faulty' circuits. The coupling capacitance between lines, being small when air-bridge technology is used, is neglected, and the primary coupling mechanism is due to resistive bridging.

These faulty circuits have been analyzed and simulated to obtain the equivalent functional faults. For resistive shorts the basic memory cell together with the *bit* and *word* line circuits were simulated with a whole range of resistance values for the 'short' to obtain a complete picture.

4.1. Analysis of Resistive/Leakage current Failure Modes

Inter-electrode resistive paths and excessive leakage currents form the most commonly observed defect in processing as well as in aging and reliability studies, as observed earlier. Since the memory cell is symmetrical with respect to the *bit* and $\overline{bit}$ lines, it is sufficient to consider resistive/leakage paths between electrodes of transistors of one half of the memory cell. Inter-electrode paths could occur between the source and the gate, or between the drain and the gate or between the source and the drain of a transistor. The following is a list of all possible paths that could occur in a single half-cell (see Fig. 11). Not shown in the figure are the gate-substrate paths that connect the gate to the substrate and may be modeled as increased gate-leakage currents:

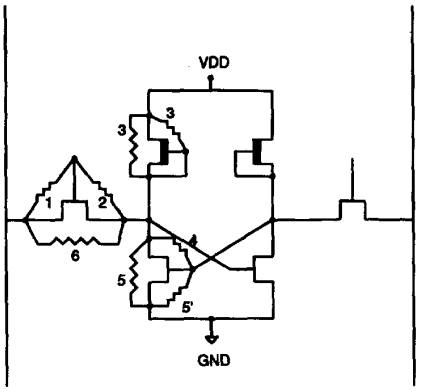

Fig. 11. Canonical set of resistive paths.

1) *bit* line to *word* line
2) *word* line to cell storage node
3) Cell storage node to power supply
4) Cell storage node to complementary cell storage node
5) Cell storage node to ground
6) *bit* line to cell storage node.

The operation of the memory cell in the presence of a resistive path between two nodes may be analyzed using a simplified equivalent circuit similar to the circuit used to analyze normal circuit operation in the previous section. However the addition of a resistor complicates the solution of the differential equations governing the operation of the cell and simple closed-form solutions cannot be obtained. However, when the resistive path occurs in parallel with an existing current path in a transistor that is ON, the conductance of a transistor in the linear region can be augmented with the conductance of the parallel resistive path to simplify the analysis. For example, a resistive path (with resistance R), between the power supply node and the cell storage node, across the drain-source nodes of the cell load transistor (resistor 3 in Fig. 11) can be modeled as an increased beta if the transistor is in the linear region. The transistor current is $I_{DS} = \beta_{LO} V_{TD}^2 \alpha V_{DS}$, approximating the tanh function by its argument, and the resistor current is $(1/R)V_{DS}$. The total current between the drain and source nodes can thus be represented as $\beta' V_{TD}^2 \alpha V_{DS}$, where $\beta' = \beta_{LO} + (1/(RV_{TD}^2\alpha))$. However this kind of simplification is not always possible and we use simulation to obtain our results.

Table II shows the result of a resistive path between the gate and source (*bit* line) nodes of the transmission gate connected to the *bit* line. The main effect of this error is to cause the *write*(0) operation to fail. The *read*(0) operation also fails. This is because the *bit* line which is sup-

TABLE II
GATE-SOURCE SHORT ON TRANSMISSION GATE—*bit* LINE TO *word* LINE

Resistance (ohms)	*Write*	*Read*	Comments
100	*Write*(0) fails *Write*(1) Delay < 100 ps	Weak 1	*Write*(0) fails *Write*/*Read*(1) slow
500	*Write*(1) Delay > 100 ps *Write*(0) fails	Weak 1	—
1000	Delay > 100 ps	Read(0) fails	—
2000	Delay > 150 ps	Same as above	—

TABLE III
COUPLING BETWEEN CELLS ON THE SAME *bit* LINE DUE TO A *bit* LINE TO *word* LINE SHORT IN ONE OF THE CELLS

Resistance (ohms)	*Write*	*Read*	Comments
100	*Write*(1) fails	*Read* error	—
500	*Write*(1) fails	*Read* error	—
1000	OK	*Read*(1) error	Cell flips to 0 when read
2000	OK	*Read*(1) error	—
5000	OK	OK	OK

TABLE IV
GATE-SOURCE SHORT ON TRANSMISSION GATE: *word* LINE TO CELL

Resistance (ohms)	*Write*	*Read*	Comments
100	Cell follows *word* line	—	Cell follows *word* line
500	Weak 1—decays after 22 ps	*Read*(1) error	—
1000	Weak 1 decays after 60 ps	*Read*(1) error	—
2000	Weak 1—decays very slowly	*Read* ok	Data retention problem
5000	OK	OK	OK

posed to be at 0 is connected to the *word* line which goes high when enabled, causing the *bit* line voltage to increase. Table III shows the effect of the above fault on a different cell connected to the same *bit* line. Table IV shows the effect of a short between the gate and source nodes of a transmission gate. This time the gate node (*word* line) is shorted to the cell directly. As a consequence, the cell follows the *word* line when the resistance is small. When the resistance is large there is a data retention problem. It may be noted that this problem occurs even though there is no missing pull-up—the chief cause of data retention problems in silicon SRAM's [11], [20].

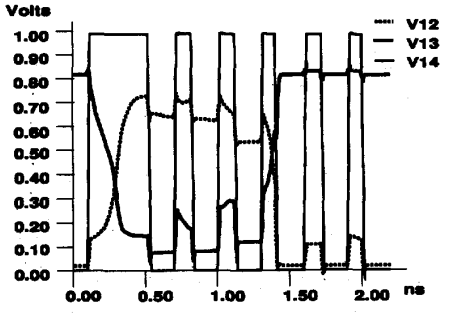

Fig. 12. Simulation of cell with missing load: V_{12} and V_{13} are the cell storage nodes. The figure shows a write followed by three *read* operations, the last one causing the cell to change state.

4.2. *Stuck-open Faults*

A stuck-open fault on a transistor is characterized by the transistor being stuck in the cut-off region with an open circuit between the drain and the source nodes. Stuck-open faults are caused by catastrophic failures and usually result in some major circuit malfunction. The stuck-open fault is equivalent to a missing transistor fault; it is also the limiting case of a device mismatch problem. Simulations of the memory cell with various stuck-open faults show that the behavior is equivalent to either a stuck-at fault or to a data retention problem. Consider a cell with the load transistor stuck-open; whereas a cell that is not accessed for *read* retains its data indefinitely, a cell that is repeatedly read, loses some of the stored charge at the faulty node with each *read* and eventually the cell changes state on a *read* operation. Three *read* operations were found to be sufficient to cause the cell to change state in simulation studies (see Fig. 12). Stuck-open faults on other transistors yield fairly obvious and predictable results and will not be discussed further.

V. Coupling and Multiple Faults

It has been shown that the formation of inter-electrode metallic paths [12] in GaAs devices is accelerated by aging and stress. It is possible that more than one device is affected by such defects. Another problem is that of increased leakage currents in normally off devices; this problem is accentuated in HEMT memories by the fact that the ratio of the ON to the OFF currents in HEMT's is much lower than in silicon. This leads to row/column pattern sensitive faults as described below.

5.1. Increased Drain–Source Leakage Currents in Access Transistors

Increase in drain–source leakage current is caused by a systematic variation in device parameters, by defects such as oval defects and by resistive paths between the drain and source of a transistor. Consider the situation where all the access transistors (among others) of the memory cells have increased leakage due to one or more of the above causes. Then consider the cells connected to one *bit* line pair as shown in Fig. 13. When all the cells store a 1 adjacent to the *bit* line and a 0 adjacent to the $\overline{bit}$ line and an attempt to write a 0 on one of the cells is made, two simultaneous effects combine to create a *write* error. The leakage current from the 1 nodes to the *bit* line prevents the *bit* line from being pulled low enough and the leakage from the $\overline{bit}$ lines to the 0 nodes prevents the $\overline{bit}$ lines from being pulled high enough. This problem affects the *read* operation even more than the write operation. When the cell to be read stores a 0 and all the other cells store a 1, the cell 0 state causes the *bit* line voltage to be pulled down and the $\overline{bit}$ voltage to be constant at V_H but the leakage currents cause the *bit* and $\overline{bit}$ line voltages to move in the opposite directions, causing a *read* error.

5.2. bit Line to word Line Short

The effects of a single *bit* line to *word* line short and a single *word* line to cell storage node short have been documented in Tables II and IV. It was seen that the final result was a function of the relative strengths of the *bit* line and *word* line drivers and of the resistance of the path between the *bit* line and the *word* line. The following behavior was seen (see Tables II and IV for details)

- if the *bit* line driver is stronger than the *word* line driver, cell C (where the defect occurred) could get written even when it is not selected,
- if the *word* line driver is stronger than the *bit* line driver, all cells on the *bit* line are stuck-at-0,
- if the strengths of the two drivers are comparable, the *read* operation is slowed down,
- if this defect (*bit* line to *word* line short) occurs in more than one cell connected to the same *bit* line, then depending on the resistance of each path from the *bit* line to the *word* lines, either all cells on the *bit* line are stuck-at-0, or the *read* operation is very slow,

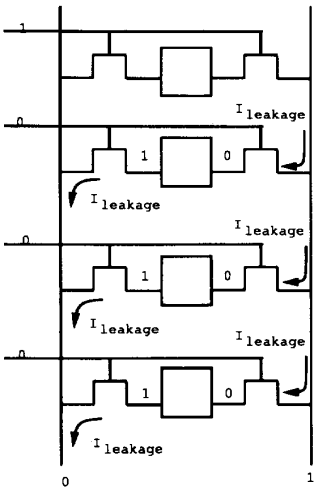

Fig. 13. Parametric pattern sensitive fault due to leakage currents.

- if this defect occurs in more than one cell connected to the same *word* line, all bits on the *word* line are stuck-at-1.

It was observed that the dominant fault effect of this failure mode, considered in isolation, was the creation of multiple cell-stuck-at faults along the same *bit* line, and the creation of delay faults for all cells on a single *bit* line.

5.3. word Line to Cell-Storage-Node Short

It can be seen from Table 4 that a single such defect could lead to data retention problems in a cell, and could also cause the cell to stuck-at-1 (0). However, it is the presence of multiple defects of this type that leads to interesting new pattern-sensitive faults.

The first case to be considered, has multiple defects of type 2 in cells connected to the same *word* line. It is assumed that the resistance of the path from a cell storage node to the *word* line is high enough to avoid data retention and stuck-at problems for the cell (see Table IV). Now, if all the cells with defect 2 store a 1, there are multiple resistive paths from the *word* line to the nodes storing a 1. The effective resistance of the path from the *word* line to a node at logic level 1, is thus decreased. These so-called storage nodes are actually *driven* by an inverter—so the effect of multiple defects of type 2 is to connect many drivers in parallel to the *word* line. If the strength of these drivers is more than the strength of the *word* line driver, the *word* line is stuck-at-1. Another aspect of this problem is the fact that some cells might have a defect 2 which connects the *bit* line to the cell storage node, while some others might have the defect in the other half of the cell, connecting the complementary storage node with the *word* line. In that case, the *word* line fault is sensitized by a pattern of ones and zeros such that each cell with a path between the storage node and the *word* line stores a 1, while each cell with a path between the complementary storage node and the *word* line stores a 0, so that the *word* line gets a maximum strength 1 drive.

TABLE V
OBSERVED FAULTS, THEIR CAUSES AND THEIR TESTS

Fault Type	Causes	Tests
Stuck at	Parameter Variations	
Simple coupling	Resistive Bridging	
	Leakage currents (parametric)	$8N$ March test
Stuck open		
Delay faults	Resistive bridging/Leakage currents	At speed test ($8N$)
Data retention	Missing/stuck open transistors	Temperature and voltage stress with stuck-at tests or
Row/Column pattern sensitive	Resistive bridging	exhaustive row/column patterns
	Leakage Currents (parametric)	Sliding diagonal

VI. TEST PROCEDURES

Well-known test procedures exist for virtually every kind of functional fault in memories. The objective of this section is to identify test procedures that test exactly the faults that were described in earlier sections. Complex general test procedures for pattern sensitive faults and coupling faults may thus be eliminated.

6.1. Leakage Current in Access Transistors

A sliding diagonal test is ideal to detect this type of fault. The fault is sensitized by a pattern of all ones (0's) on the cells in the *bit* line and tested by writing and reading 0 to one cell (see Fig. 13).

6.2. Multiple word Line to Storage-Node Shorts

If the defects in the cells were truly randomly distributed between the two storage nodes, 2^n patterns would be required to guarantee that the fault is sensitized, where n is the number of cells on a single *word* line. An analysis of the causes of the gate-drain short reveals that this short is caused by a metallic path between the electrodes that develops as a result of stress, aging and the voltage difference between the two electrodes. Hence this defect can be made to manifest itself by continuously storing a pattern of all ones and all zeros. This would lead to the development of paths between the storage node and *word* line of every potentially defective cell. These failure modes can then be detected by simple stuck-at tests for each cell since they do not exhibit any fault-masking behavior.

6.3 Other Multiple Shorts and Their Tests

There are three other types of shorts that can occur in a single memory cell. These are (3) cell storage node to power supply, (4) cell storage node to complementary cell storage node, and (5) cell storage node to ground.

A resistive path between the cell storage node and power supply, makes the cell stuck-at-1. A resistive path between the cell storage node and ground makes the cell stuck-at-0. A resistive path between the two complementary storage nodes of a cell, tends to equalize the voltages at the two nodes that are supposed to be at opposite polarities. Hence a *write* operation on the cell fails. The two node values cannot be changed by a *write* operation. Subsequent *read* operations, therefore, always give the same result, regardless of what is written on to the cell (assuming the sense amplifier has some hysteresis to take care of fluctuations due to noise).

Multiple faults of the same kind (3 alone or 5 alone) do not mask one another or create new kinds of pattern-sensitive faults. Hence such faults can be detected by a march test or a classical RAM test pattern such as the $30N$ pattern of Nair [26].

Faults coupling different memory cells occur due to shorts between lines of adjacent cells. The effect of these faults is to cause coupling between a cell and one of its two neighbors on the same *word* line since the layout ensures that other cells are separated by power or ground lines. Hence a simple $8N$ test which reads and writes 1 and 0 on each cell in the presence of all combinations of 1 and 0 in the two adjacent cells is sufficient to cover all expected pattern-sensitive faults of this type. Table V lists the observed faults and the corresponding tests.

VII. CONCLUSIONS

Realistic fault models for GaAs memory devices have been identified on the basis of an extensive study of the defect mechanisms in GaAs. The memory faults have been classified as design-related, process-related and layout-related faults. Design related faults occur due to marginal design and lead to simple *read/write* errors. These faults can be detected by classical test procedures such as the march test of [26] or the more recent $13N$ algorithm of [11]. Process and layout related faults cause data-retention faults, delay faults and some specific types of pattern-sensitive faults. A new mechanism for data retention problems, unique to GaAs processes, has been identified. This data retention problem is caused by gate leakage currents that are considerably larger than the leakage currents seen in silicon processes. Row- and column- pattern-sensitive faults have been observed, which cannot be detected by the conventional tests for five- or nine-cell neighborhood pattern-sensitive faults. A simple test procedure that relies on sensitization of the fault by application of suitable voltages and temperatures has been proposed to detect this type of fault. Other pattern-sensitive faults have been shown to have a locality property and hence a fast $O(N)$ test pattern.

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S. Mohan for a photograph and a biography, please see page 1326 of the September 1993 issue of this TRANSACTIONS.

Pinaki Mazumder (S'84–M'87) for a photograph and a biography, please see page 136 in the January 1993 issue of the TRANSACTIONS.