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Invited Talk #2

Analog Computation-in-Memory (CiM) for AI Applications

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***Abstract*—** This talk overviews analog CiM, Computation-in-Memory with non-volatile memories for edge AI applications. To extremely enhance the energy efficiency of edge AI, the heterogeneous integration of sensors like event-based sensors and CiM is promising. By tolerating some degree of device errors of CiM, the trade-off of performance, energy and cost is resolved. CiM can be effectively used for various AI algorithms such as Convolutional Neural Network, Recurrent Neural Network, event driven Spiking Neural Network, Reservoir Computing, Transformers and Lottery Ticket Hypothesis Neural Network Algorithm.

Biography

Dr. Ken Takeuchi received the B.S. and M.S. degrees in applied physics and the Ph.D. degree in electric engineering from The University of Tokyo, Tokyo, Japan, in 1991, 1993, and 2006, respectively, and the M.B.A. degree from Stanford University, Stanford, CA, USA, in 2003. Since he joined Toshiba, Yokohama, Japan, in 1993, he had been leading Toshiba's NAND flash memory circuit design for 14 years. He was an Associate Professor with the Department of Electrical Engineering and Information Systems, Graduate School of Engineering, The University of Tokyo, from 2007 to 2012. He was a Professor with the Department of Electrical, Electronic and Communication Engineering, Faculty of Science and Engineering, Chuo University, Tokyo, from 2012 to 2020. In 2020, he rejoined The University of Tokyo, where he is currently a Professor with the Department of Electrical Engineering and Information Systems, Graduate School of Engineering. He designed six world's highest density NAND flash memory products, such as 0.7-µm 16-Mbit, 0.4-µm 64-Mbit, 0.25-µm 256-Mbit, 0.16-µm 1-Gbit, 0.13-µm 2-Gbit, and 56-nm 8-Gbit NAND flash memories. He is working on data centric computing, such as computation in memory, approximate computing, data scale computing, AI chip design, brain-inspired memory, and quantum computing. He holds 228 patents worldwide, including 124 U.S. patents. Especially, with his invention, "multipage cell architecture," presented at the Symposium on VLSI Circuits in 1997, he successfully commercialized world's first multi-level cell NAND flash memory in 2001. He has authored numerous technical articles.