Modified H-Bridge Inverter with Reduced Number of Switching Devices

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***Abstract*—In this paper, a modified topology for developing H-bridge inverter is proposed which the number of components is lower than other inverters as well as the proposed inverter generates a high number of level with low total harmonics distortions. In the first, the new developed h-bridge inverter is proposed and then a cascaded connection of this inverter to increase the number of levels is presented. Three different methods are proposed to determine the DC power sources magnitudes and among them, the best algorithm is chosen for comparison the proposed cascaded inverter with other cascaded inverters. Finally, the proposed cascaded inverter consist of two proposed basic inverters to generate thirty-three voltage levels is simulated to evaluate the performance of the proposal.**

***Index Terms*—developed H-bridge inverter; cascaded inverter; reduced components.**

I. Introduction

Increasing the use of multilevel inverters (MLIs) in the industry, including renewable energy sources, drive motors, FACTS devices, distributed generation and etc, the researchers interested in developing of this field [1], [2]. Multilevel inverters have more advantages than two-level inverters such as higher power quality, lower blocking voltage on the switching device, lower THDs, less electromagnetic interference, medium and high voltages capability, lower power losses, etc [3], [4]. In 1970, cascaded h-bridge (CHB) multilevel inverter introduced into the industry and then natural point diode clamped (NPC) and flying capacitor (FC) multilevel inverters have been developed in 1981 and 1999. NPC and FC inverters have problems such as an imbalance of voltage capacitors, complex control, and require a large number of capacitors and semiconductor switch. In addition, in the conventional multilevel inverters by increase the number of levels the number of components are raised rapidly [5]. For above reasons, many researchers are working on cascaded h-bridge multilevel inverters [6].

To reduce the number of components in cascaded multilevel inverters, basically, they are separated into two structures: symmetrical and asymmetrical structures. In symmetric structure, all DC power sources have the same value in each unit while in the asymmetric structure are different. Anyway, the high number of required DC power sources and power switches are disadvantageous for symmetric and asymmetric multilevel inverter when the number of output levels increase [7], [8]. The most multilevel inverter topologies which presented recently only can generate positive voltage levels. To overcome this problem, an additional H-bridge is used to produce negative levels so the sum of all DC power sources blocks on the H-bridge inverter that creates high switching losses, as well as the rating of the power switches are increased due to suffering the maximum blocking voltage on these switches [9].

According to the presented document in the literature, the researcher is developing multilevel inverters topologies based on reducing the number of switching devices [10]–[13]. One of these topologies is the developed H-bridge inverter that has been extended in the different design. The presented topologies in [14], [16] has been designed based on developed H-bridge inverter. But the number of used switches in each of these topologies is different. As a result, the number of output voltages levels and the maximum output voltage are different. According to the comparison of the first presented topology [14] with the redesigned topologies from this topology, the newly presented topologies generated a large number of voltage levels with a lower number of switching devices and the maximum blocking voltage [15], [16].

In this work, a modified developed H-bridge topology presents which can create all positive and negative voltage levels with less number of switching devices and DC power sources than other multilevel inverter topologies. After that, a cascaded connection is introduced based on three proposed algorithm for DC power sources values to compare the proposed inverter with other cascaded multilevel inverters. In the end, a 33 level cascaded multilevel inverters based on two proposed basic inverters is simulated and the output waveforms are analyzed.

II. Methodology

The proposed topology is investigated in two structures: proposed basic topology and cascaded multilevel inverter. Also, The calculation of total standing voltage by the power

switches, number of components, and three methods to determine DC power sources are presented.

A. Proposed Basic Inverter

The power circuit of the proposed modified developed H-bridge inverter is shown in Fig. 1. The proposed inverter consists of ten power switches with four independent DC power sources. The type two switches are bidirectional switches because they have to conduct currents and block voltages in both polarities. The right side of the proposed inverter creates the voltage levels of $\pm V_1, \pm 2V_1$ and left side creates the voltage levels of $\pm V_2, \pm 2V_2$.

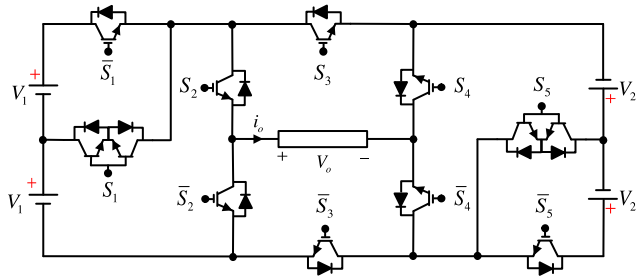

Fig. 1: The proposed 17-level basic inveretr.

TABLE I: The Switching States of 17-level Basic Inverter

V_o	S_1	$\bar{S}_1$	S_2	$\bar{S}_2$	S_3	$\bar{S}_3$	S_4	$\bar{S}_4$	S_5	$\bar{S}_5$
$+8V_{dc}$	0	1	1	0	0	1	1	0	0	1
$+7V_{dc}$	1	0	1	0	0	1	1	0	0	1
$+6V_{dc}$	0	0	0	1	0	1	1	0	0	1
$+5V_{dc}$	0	1	1	0	0	1	1	0	1	0
$+4V_{dc}$	1	0	1	0	0	1	1	0	1	0
$+3V_{dc}$	0	0	0	1	0	1	1	0	1	0
$+2V_{dc}$	0	1	1	0	0	1	0	1	0	0
$+1V_{dc}$	1	0	1	0	0	1	0	1	0	0
0	0	0	0	1	0	1	0	1	0	0
	0	0	1	0	1	0	1	0	0	0
$-1V_{dc}$	1	0	0	1	1	0	1	0	0	0
$-2V_{dc}$	0	1	0	1	1	0	1	0	0	0
$-3V_{dc}$	0	0	1	0	1	0	0	1	1	0
$-4V_{dc}$	1	0	0	1	1	0	0	1	1	0
$-5V_{dc}$	0	1	0	1	1	0	0	1	1	0
$-6V_{dc}$	0	0	1	0	1	0	0	1	0	1
$-7V_{dc}$	1	0	0	1	1	0	0	1	0	1
$-8V_{dc}$	0	1	0	1	1	0	0	1	0	1

The total output voltage levels in the proposed topology are obtained from the sum of right side voltage levels and left side. Table 1 shows the operation modes of the proposed basic inverter to generate all voltage levels. It is evident that in the proposed inverter the switches current is equal with the load current so the limitation of the switch current is specified by the values of the load current of the inverter. In the basic inverter, the switches $(S_1, \bar{S}_1)$, $(S_2, \bar{S}_2)$, $(S_3, \bar{S}_3)$, $(S_4, \bar{S}_4)$ and $(S_5, \bar{S}_5)$ are complementary of each other. Namely, when the switch S_1 is on, the switch $\bar{S}_1$ should be off to prevent the short-circuiting. The magnitudes of DC power sources can consider symmetric and asymmetric. If the values of DC power sources are considered equal ($V_1 = V_2 = V_{dc}$), the inverter is in symmetric mode. So the proposed basic inverter generates nine levels. In the asymmetric mode, the values of DC power sources are considered differently ($V_1 = V_{dc}$, $V_2 = 3V_{dc}$). So the inverter can generate seventeen voltage levels at the output.

B. Total Standing Voltage Calculation

The maximum total standing voltage (TSV) on the power switches is an important creation to reducing the cost of multilevel inverters and reducing of the voltage of the switches rating in high-power medium-voltage applications. In the proposed modified developed H-bridge inverter the value of TSV is obtained as follows:

$$TSV_{basic} = \sum_{j=1}^{5} V_{Si} + V_{\bar{S}i} \tag{1}$$

The standing voltage on each switching device is:

$$V_{S1} = V_{\bar{S}1} = 2V_1 \tag{2}$$

$$V_{S2} = V_{\bar{S}2} = 2V_1 \tag{3}$$

$$V_{S3} = V_{\bar{S}3} = 2(V_1 + V_2) \tag{4}$$

$$V_{S4} = V_{\bar{S}4} = 2V_2 \tag{5}$$

$$V_{S5} = V_{\bar{S}5} = V_1 + V_2 \tag{6}$$

Considering the relations (1) to (6), the valued of TSV in asymmetric mode with values of $V_1 = V_{dc}, V_2 = 3V_{dc}$ (to generation 17-level) is defined as:

$$TSV_{basic} = 2(7V_1 + 5V_2) = 44V_{dc} \tag{7}$$

C. Proposed Cascaded Multilevel Inverter

To obtain the maximum voltage levels in Fig. 2 a cascaded connection is proposed. The proposed cascaded inverter consists of n number of the proposed basic inverter. Therefore the output voltage levels are obtained as follow:

$$V_o = V_{o1} + V_{o2} + ... + V_{on} \tag{8}$$

In order to achieve the maximum output voltage levels in cascaded connection, the number of DC power sources are considered constant in each proposed inverter.

$$n_1 = n_2 = ... = n_j = n \tag{9}$$

The number of components: switch, driver, insulated gate bipolar transistor (IGBT), diode, DC power source in the proposed cascaded inverter are as follows:

$$N_{switch} = N_{driver} = 10n \tag{10}$$

$$N_{IGBT} = N_{diode} = 12n \tag{11}$$

$$N_{DC} = 4n \tag{12}$$

The value of TSV for proposed cascaded inverter, considering equation (7) is calculated as follows:

$$TSV_{cascaded} = 12 \sum_{j=1}^{n} (V_{1j} + V_{2j}) \tag{13}$$

D. DC Power Sources Values

Three different methods are proposed to determine the DC power sources values in the proposed cascaded inverter.

First Method: The first method is a symmetric mode, in this mode, the magnitudes of all DC power sources are equal as follows:

$$V_{1j} = V_{2j} = V_{dc} \tag{14}$$

So in this method, the maximum output voltage and the number of levels, are calculated as follows:

$$V_{o,max} = 4nV_{dc} \tag{15}$$

$$N_{Level} = 8n + 1 \tag{16}$$

Second Method: the second method is an asymmetric mode, in this mode, the values of DC power sources are based on trinary mode. So the magnitudes of DC power sources are considered as follow:

$$V_{1j} = V_{dc}, V_{2j} = 3V_{dc} \tag{17}$$

Therefore, the maximum output voltage and the number of levels, are obtained as follows:

$$V_{o,max} = 16nV_{dc} \tag{18}$$

$$N_{Level} = 16n + 1 \tag{19}$$

In this method, the first basic unit generates 17 voltage levels and other cascaded units generate a same 17 voltage levels. For example, if the number of cascaded unit are assumed two basic unit, the number of levels is equal 33 levels correspond equation (19).

Third Method: the third method is an asymmetric method with the capability to generate a high number of voltage levels. In this method, the magnitudes of all DC power sources are considered differently for all cascaded units. Therefore, the magnitudes of DC power sources in each unit are assumed as follows:

$$V_{1j} = 17^{j-1}V_{dc}, V_{2j} = 3(17^{j-1})V_{dc} \tag{20}$$

Therefore, the maximum output voltage and the number of levels are obtained as follows:

$$V_{o,max} = [(17^n - 1)/2]V_{dc} \tag{21}$$

$$N_{Level} = 17^n \tag{22}$$

In this case, the first inverter generates 17 levels and other units generate 17 levels differently from their previous unit.

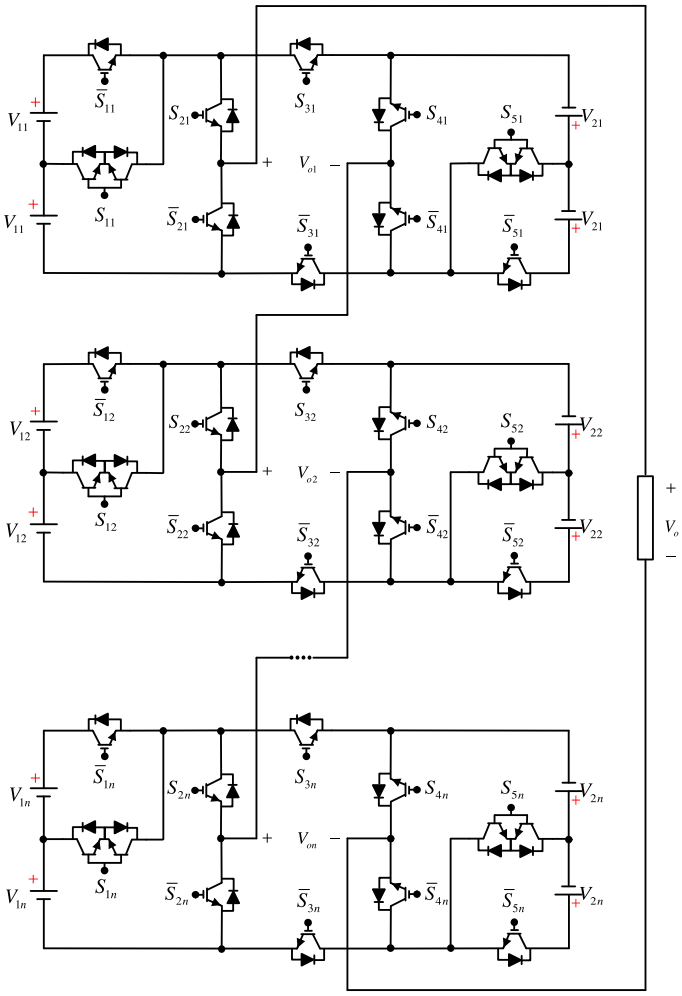

Fig. 2: Cascaded multilevel inverter based on n number of proposed basic inverter.

III. Comparison the Proposed Cascaded MLI with Presented Cascaded MLIs in [11]–[16]

To illustrate the advantages and disadvantages of the proposed multilevel inverter, the comparison is performed among the proposed cascaded topology with similar cascaded multilevel inverter topologies in terms of the number of power switch, IGBTs, DC power sources and the values of TSV to validate the new capabilities of the proposed topology in competition with other topologies. In this comparison, the all cascaded topologies are correspond the presented topologies in [11]–[16]. All cascaded multilevel inverters have been presented using developed H-bridge inverter and the number of left and right DC power sources are equal in all topologies. In each topology, the number of components is unique and they have expanded based on their designing methods to generate the maximum voltage at the output. In addition, in all topologies, two bidirectional power switches are separated topologies into two sides: right and left side and the maximum voltage drop is stood by both of these switches. The used power switches are bidirectional and unidirectional switches in the presented topologies.

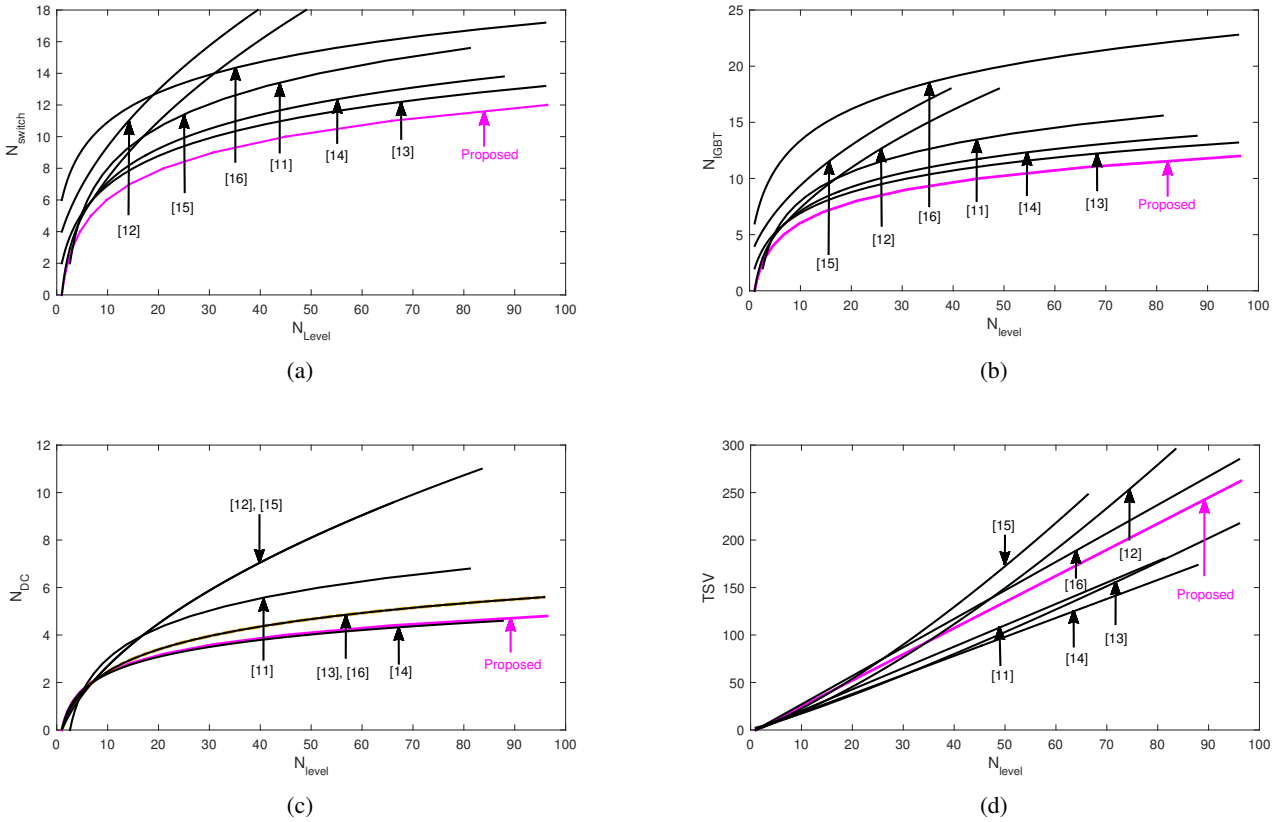

Fig. 3: (a) the variation number of required switches versus N_{Level} ; (b) the variation number of required IGBTs versus N_{Level}; (c) the variation number of required DC power sources versus N_{Level}; (d) the variation magnitude of TSV versus N_{Level}.

A bidirectional switch includes an IGBT with a reverse parallel diode that requires a driver circuit, but a unidirectional switch consists of two IGBTs with two reverse-parallel diodes that are connected in a common emitter. In order to maximize the effect of each topology, the methods that create the highest number of output levels are chosen to compete with other topologies.

Fig. 3(a) shows the number of switches in each topology to generate different number levels. According to the figure, the proposed topology uses less number of the switch to create the maximum number of levels, after the proposed topologies are the presented topologies in [13], [14].

Fig. 3(b) presents the number of IGBT in each topology to generate a different number of levels. As one can see, the proposed topology requires lower IGBT than other topologies to generate the same levels, after the proposed topology, are the presented topologies in [13], [14].

Another important criterion in designing multilevel inverter topologies is the number of DC power sources. Fig. 4(c) shows the required number of independent DC power sources to generate different levels at the output of inverters. With respect to this figure, the presented topology in [14] and new proposed topology are competing to each other, and then the presented topologies in [13], [16] have less number of independent DC power sources.

Fig. 3(d) presents the variation of the maximum total standing voltage against the different levels in all cascaded topologies. According to this figure, the presented MLI in [11], [13], [14] have less TSV value, topologies [12], [15] have high TSV value and the proposed topology along with presented topology [16] has an average TSV value for generating a same voltage levels .

However, based on the presented comparison the proposed cascaded inverter requires less number of components to generate a high number of levels as well as the proposed topology used less number of independent DC power sources than other presented topologies.

IV. Simulation Results

In this section to show the capability of the proposed inverter, the simulation results of a thirty-three level cascaded inverter are presented that consist of two basic units. In order to generate the switching pulses, the fundamental frequency technique is used for the proposed 33-levels cascaded inverter. The main objective of the fundamental frequency modulation is its low switching frequency that leads to low switching losses [17].

The power scheme of the proposed 33 level cascaded multi-level inverter is shown in Fig. 4. The load type is an R-L load with 20Ω and $15mH$ with $50Hz$ frequency. Each unit consists of ten power switch and four DC power sources. In order to achieve 33 levels, the proposed second method is used for the

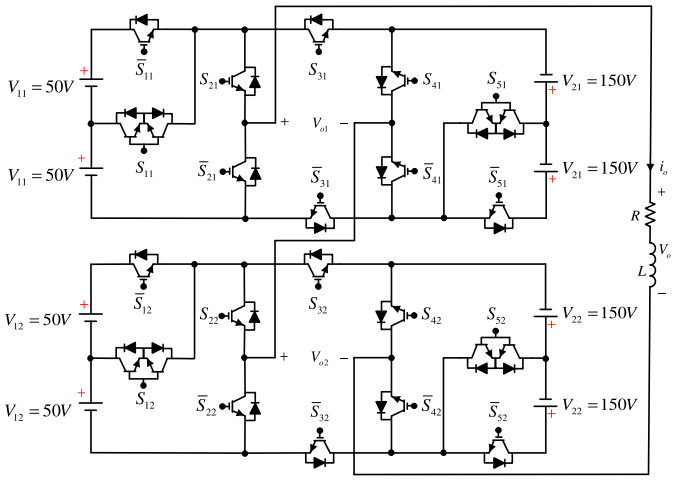

Fig. 4: Proposed 33-level cascaded multilevel inverter power circuit under simulation.

values of DC power sources. Therefore, the DC power sources values for first and second units are $V_{1,1} = V_{1,2} = 50V$, $V_{2,1} = V_{2,2} = 150V$. So, each inverter generated a same seventeen voltage levels at their output.

Figs. 5(a) and (b) illustrate the output voltage of each basic unit. The total voltage of the cascade inverter is the sum of the output voltage of each basic unit. Fig. 5(c) shows the total output voltage of proposed cascaded topology which is 33-levels with the peak value of $800V$ as well as the multilevel sine signal is made up of $50V$ voltage steps from the maximum negative value up to the positive maximum. The output current of a 33-level cascaded inverter is shown in Fig. 5(d). The output current has a phase shift with output voltage due to load type which consists of an inductive load.

The FFT of the load voltage and current are indicated in Figs. 6(a) and 6(b). As can see from these figures, THD values are 1.23% and 0.44% for the voltage and current of the 33-level cascaded inverter, respectively.

Figs. 7(a) and 7(b) show the maximum blocking voltage on the power switches S_3, $\bar{S}_3$. As obvious from this figure, the maximum voltage is blocked by these both switches. These switches suffer the maximum voltage of $400V$ from $800V$ that is the peak of the output voltage.

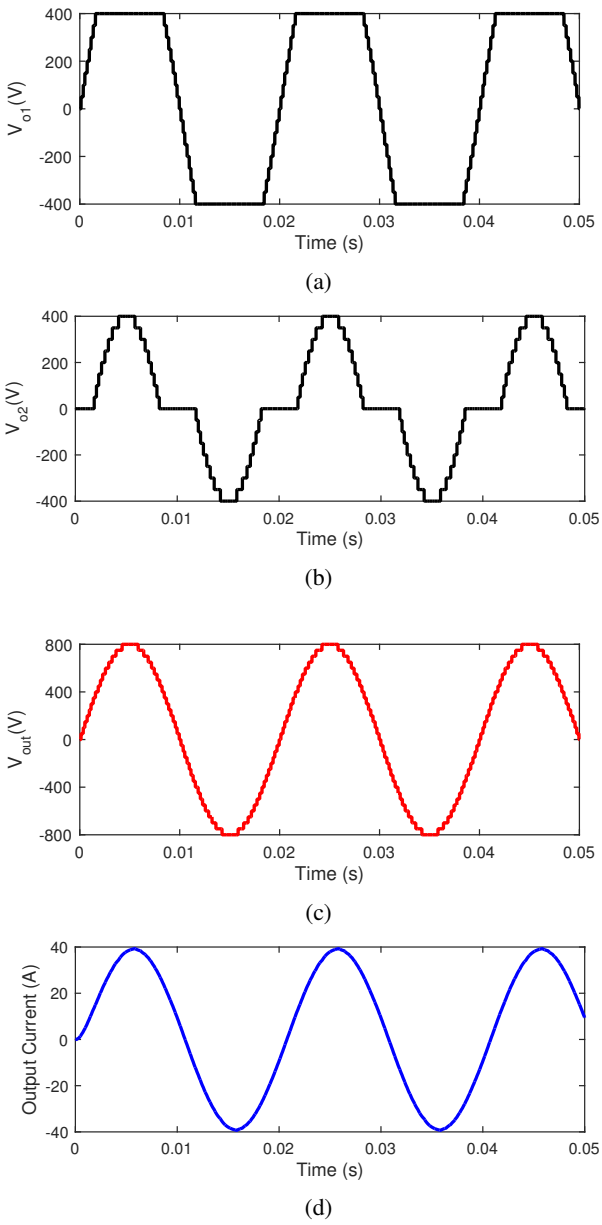

Fig. 5: Simulation studies; (a) 17-level output voltage curve of first unit; (b) 17-level output voltage curve of second unit; (c); 33-level total output voltage curve of the proposed cascaded multilevel inverter; (d) output current curve.

V. Conclusion

In this paper, a modified developed H-bridge inverter was introduced for symmetric and asymmetric cascaded multilevel inverters. A cascaded topology was presented along with three different methods to achieve a high number of voltage levels. The proposed cascaded modified H-bridge inverter decreased the number of switches, driver circuits, IGBTs and DC power sources than other similar presented cascaded topologies based on the presented comparison that was performed. In the end, to confirm the capability of the proposed modified H-bridge inverter a cascaded connection was simulated in Matlab/Simulink platform to obtain 33 voltage levels.

Acknowledgment

The authors wish to acknowledge the financial support of FONDECYT Regular 1160690 Research Project.

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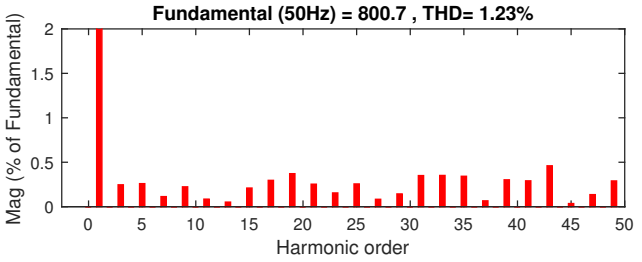
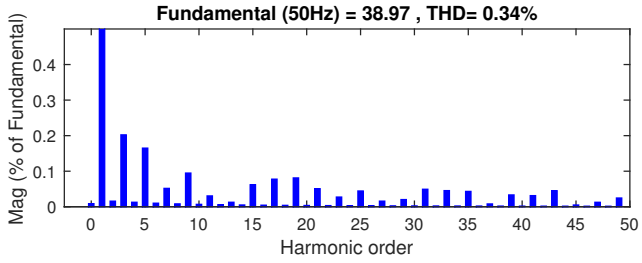
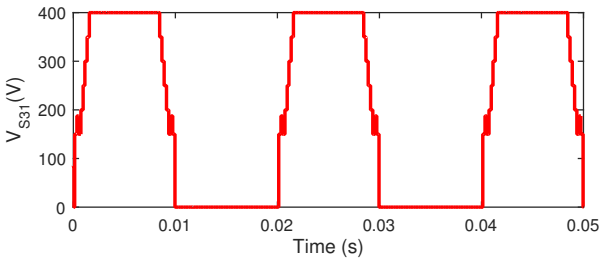


(a)

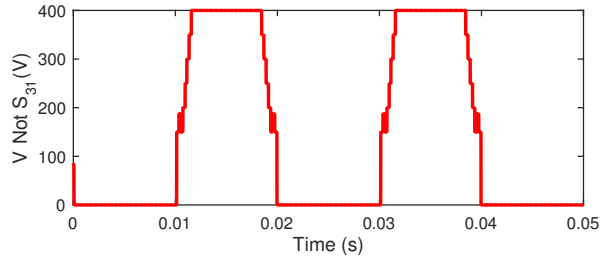


(b)

Fig. 6: (a) FFT of the voltage (THDv = 1.23%); (b) FFT of the current (THDi = 0.34%).



(a)



(b)

Fig. 7: (a) the maximum blocked voltage by switch S_{31}; (b) the maximum blocked voltage by switch $\bar{S}_{31}$.

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