TESTING HIGH RESOLUTION ADCS USING DETERMINISTIC DYNAMIC ELEMENT MATCHING

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ABSTRACT

Dynamic element matching (DEM) is an effective approach to achieving good average performance in the presence of major mismatch in matching-critical circuits. This paper presents a deterministic DEM (DDEM) strategy for ADC testing that offers substantial reductions in testing cost. The approach is mathematically formulated and validated with simulation results that show the number of test vectors needed is comparable to what are currently used with standard code density linearity testing. It is demonstrated that the DDEM method can be used to accurately test ADCs with linearity that far exceeds that of the DAC used as a signal generator. This technique offers potential for use in both production test and BIST environments where high linearity devices are difficult to test and characterize.

1. INTRODUCTION

Analog-to-Digital Converters (ADCs) are recognized as the world's largest volume mixed-signal circuit [1]. With the increasing complexity of mixed-signal circuits and the emergence of low-cost mixed-signal IC market, testing of analog and mixed-signal circuits in general and ADCs in particular has become a challenging and costly process [2].

Built-in-self-test (BIST) structures offer potential solutions not only in terms of reduction of costs, but also in terms of its ability to test deeply embedded systems on a chip (SOCs) [3]. There have been many attempts in providing BIST solutions for ADCs, but most existing approaches in the literature have been aimed at duplicating a standard tester on chip [4] [5] which has better performance than the device under test (DUT). This becomes a significant challenge since such high performance signal generators require more design effort and more silicon area than the ADC to be tested.

The DEM method has been used by many researchers to improve the performance of DACs [6-10]. Most researchers use these DACs on Delta-Sigma converters when high linearity is required.

Although there have been concerns about using DEM to create "effectively linear" devices since the actual nonlinearity in the signal path is not removed, we believe the "averaged linearity" provided by DEM can be exploited to generate "effectively linear" stimulus signals for ADC testing. This approach allows the signal generator to be realized with a not-so-accurate DAC, hence eliminating the need of large silicon area and reducing the cost of the test signal generator. In a preliminary study, a test strategy was introduced to use random DEM in a highly-nonlinear DAC to test low-resolution ADCs [11]. A new DDEM testing technique was also introduced and compared with the random DEM testing approach when a low accuracy DAC is used to characterize/test an ADC with higher linearity in [12]. In this work the DDEM algorithm is explained in detail with mathematical proof of its behavior. Also simulations for high resolution ADC characterization using DDEM are shown in this work.

This paper is organized as follows. Details are presented in Section 2 about both the DDEM implementation, along with mathematical derivation and algorithm description. In Section 3 simulation results for high resolution ADCs are shown and discussed. Section 4 summarizes this work.

2. DDEM METHOD FOR THERMOMETER CODED DACS

A current steering DAC can be thermometer coded, binary coded or their combination. To get started, the DDEM method was applied to a thermometer coded DAC. Suppose the DAC has n-bit resolution, then it has 2^n-1 current source elements. The DAC structure is shown in Figure 1.

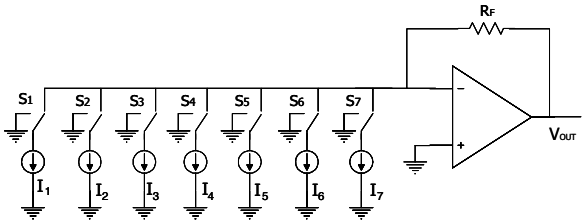

Figure 1: A 3-bit current mode thermometer-coded DAC

The deterministic method deterministically picks the current sources to be switched on. The pattern used attempts to distribute the sources to be switched on in a way that all sources are used almost uniformly. As explained in [11] and [12], p represents the number of samples to be generated for each DAC input word.

The following deterministic DEM switching scheme (Cyclic Switching Sequence) was applied to the DAC current sources:

1. All current sources are arranged conceptually along a circle so we can visualize the wrapping effect (physical layout of the current sources can be a rectangular array). p starting

places are selected among the current sources spaced by $q = N / p$.

2. For each input code k, the DAC generates p samples of output. Each sample is obtained by switching k current sources consecutively starting from one of the p starting places. The d^{th} $(1 \le d \le p)$ sample is obtained by switching k current sources starting from $i_{(d-1)q+1}$ in the clock-wise direction.
3. The output analog signal is obtained by forcing the summation of the selected k current sources to drive a resistor R_F. Since the resistor value can be viewed as a normalization factor, we only need to examine the current through it to evaluate the DAC performance.

Now, we will formally show that the "averaged DAC" with our DDEM approach can generate a signal that is very close to being an ideal ramp. This is done by showing that the INL of the averaged DDEM DAC is very small.

The mismatch in the current sources of the DAC will be modeled by the relationship:

$$I_j = I_0(1+\varepsilon_j) \quad (j = 1,...,N) \tag{1}$$

where $\varepsilon_j \ (j = 1,...,N)$ are independent and identically distributed Gaussian random variables that model the mismatch in the current sources. Beyond the current source mismatch, it will be assumed that the DACs are ideal. The standard notation for the distribution of ε_j is thus $\varepsilon_j \ i.i.d. \sim N(0,\sigma^2)$ where the standard deviation σ is determined by the area allocated in the design and by process variations.

Since one extra current source has been added to the current source array for notational convenience, we will define the fit line to be the line connecting the DAC output voltages corresponding to the first and last DAC thermometer input codes. Since the DAC output voltage is assumed to be proportional to the output current of the current source array, we will characterize the linearity of the output current instead of the voltage in all computations. The output current for the input code **0** is 0 and the output current for input code **k** for $1 \le k \le N$ is given by:

$$I(k) = \sum_{j=1}^{k} I_j = kI_0 + I_0 \sum_{j=1}^{k} \varepsilon_j \tag{2}$$

From (2) it follows that the output for code N is given by

$$I(N) = \sum_{j=1}^{N} I_j = NI_0 + I_0 \sum_{j=1}^{N} \varepsilon_j \tag{3}$$

therefore the LSB of the DAC is given by:

$$I_{LSB} = \frac{I(N)}{N} = I_0 + \frac{I_0}{N} \sum_{j=1}^{N} \varepsilon_j \tag{4}$$

It can be observed that the random variable I_{LSB} is Gaussian with a $N(I_0, \frac{I_0^2}{N}\sigma^2)$ distribution. Since N is very large for even modest resolution, the deviation of I_{LSB} from I_0 is very small. The fit-line of the DAC for each input code k is then given by:

$$I_{FIT}(k) = k \cdot I_{LSB} = kI_0 + I_0 \frac{k}{N} \sum_{j=1}^{N} \varepsilon_j \tag{5}$$

It follows that the INL_k for the DAC without using dynamic element matching is given by the expression

$$\mathrm{INL_k} = \begin{cases} 0 & k = 0, N \\ I_0\left(\sum_{\mathrm{j}=1}^{\mathrm{k}} \varepsilon_{\mathrm{j}} - \frac{k}{N} \sum_{\mathrm{j}=1}^{\mathrm{N}} \varepsilon_{\mathrm{j}} \right) & 0 \le k \le N-1 \end{cases} \tag{6}$$

It follows from (6) that the distribution for the INL_k is

[13] $N(0, \frac{(N-k)kI_0^2}{N}\sigma^2)$

and the largest standard deviation in INL_k, in LSB, is approximately

$$\sigma_{INL_k} = \frac{\sqrt{N}}{2}\sigma. \tag{7}$$

The average deviation from the average fit line for the DDEM DAC will now be determined. Since each code is input p times and since it will be assumed that the first and last input codes, codes **0** and **N,** are also input p times, these codes determine the end-point fit line. Then the average fit line is identical to the fit line defined in equation (5). The average deviation from the average fit line at code k is defined to be the INL_k for the DDEM DAC at code k and is denoted as $\overline{INL_k}$.

Each of the p inputs for code k in the Cyclic Switching Sequence is given by

$$I_d(k) = \sum_{j=1}^{k} I_{(d-1)q+j} \qquad d = 1,..., p \tag{8}$$

The average of the p samples for code k, denoted by $\bar{I}(k)$, is given by

$$\bar{I}(k) = \frac{1}{p} \sum_{d=1}^{p} \sum_{j=1}^{k} I_{(d-1)q+j} \tag{9}$$

It follows from (1), (5), and (9) that

$$\overline{\mathrm{INL_k}} = \bar{\mathrm{I}}(\mathrm{k}) - \mathrm{I_{FIT}}(\mathrm{k}) = \frac{I_0}{p} \sum_{d=1}^{p} \sum_{j=1}^{k} \varepsilon_{(d-1)q+j} - k\frac{I_0}{N} \sum_{j=1}^{N} \varepsilon_j \tag{10}$$

From this simple expression, it can be observed that whenever k is a multiple of q, that is k=hq, then (10) can be rewritten as

$$\overline{\mathrm{INL_k}} = \bar{\mathrm{I}}(\mathrm{k}) - \mathrm{I_{FIT}}(\mathrm{k}) = \frac{hI_0}{p} \sum_{j=1}^{N} \varepsilon_j - hq\frac{I_0}{N} \sum_{j=1}^{N} \varepsilon_j = \tag{11}$$

$$= hI_0\left(\frac{1}{p} - \frac{q}{N} \right) \sum_{j=1}^{N} \varepsilon_j$$

The term in parenthesis in (11) is zero whenever k is a multiple of q, since qp=N. This implies the average value of the input for the Cyclic Switching Sequence is exactly on the fit line whenever k is a multiple of q.

We will now derive an expression for the standard deviation of the $\overline{INL_k}$ when k is not necessarily a multiple of q. The two terms on the right hand side of (10) contain correlated random variables so the standard deviation is difficult to obtain directly from this equation. If we express k = tq+s, then the index k will span the linear space from 0 to N when t and s span the linear space from 0 to p-1 and 1 to q respectively where we are again assuming that pq=N.

It follows from (1) and (9) that

$$\bar{I}(k) = k \cdot I_0 + I_0 \cdot \frac{1}{p} \cdot \left(t \cdot \sum_{d=1}^{p} \sum_{j=s+1}^{q} \varepsilon_{(d-1)q+j} + (t+1) \cdot \sum_{d=1}^{p} \sum_{j=1}^{s} \varepsilon_{(d-1)q+j} \right) \quad (12)$$

This can be simplified to the expression

$$\bar{I}(k) = k \cdot I_0 + I_0 \cdot \frac{1}{p} \cdot \left(t \cdot \sum_{j=1}^{N} \varepsilon_j + \cdot \sum_{d=1}^{p} \sum_{j=1}^{s} \varepsilon_{(d-1)q+j} \right) \quad (13)$$

It thus follows from (5) and (13) that

$$\overline{INL_k} = i_0 \frac{1}{P} \cdot \left(t \cdot \sum_{j=1}^{N} \varepsilon_j + \cdot \sum_{d=1}^{p} \sum_{j=1}^{s} \varepsilon_{(d-1)q+j} \right) - i_0 \frac{k}{N} \sum_{j=1}^{N} \varepsilon_j \quad (14)$$

This can be rewritten as

$$\overline{\mathrm{INL_k}} = \mathrm{I_0} \left[\left(\frac{1}{\mathrm{p}} - \frac{\mathrm{s}}{\mathrm{N}} \right) \sum_{\mathrm{d=1}}^{\mathrm{p}} \sum_{\mathrm{j=1}}^{\mathrm{s}} \varepsilon_{\mathrm{(d-1)q+j}} - \frac{\mathrm{s}}{\mathrm{N}} \sum_{\mathrm{d=1}}^{\mathrm{p}} \sum_{\mathrm{j=s+1}}^{\mathrm{q}} \varepsilon_{\mathrm{(d-1)q+j}} \right] \quad (15)$$

The random variables under the two summands in (15) are now uncorrelated and then the $\overline{INL_k}$ normalized to a LSB is a Gaussian random variable characterized by:

$$\frac{\overline{\mathrm{INL}_k}}{\mathrm{I_0}} \sim \mathrm{N}\left(0, \mathrm{A}\sigma^2\right) \quad (16)$$

where

$$\mathrm{A} = \left(\frac{1}{\mathrm{p}} - \frac{\mathrm{s}}{\mathrm{N}} \right)^2 \mathrm{ps} + \left(\frac{\mathrm{s}}{\mathrm{N}} \right)^2 \mathrm{p(q-s)} = \frac{\mathrm{s(q-s)}}{\mathrm{pq}} \quad (17)$$

It can be shown from (17) that the variance of $\overline{INL_k}$ reaches a maximum value at s = q/2. Using this value for s it follows that the standard deviation of $\overline{INL_k}$ in LSB is given by

$$\sigma_{\overline{INL_k},max} = \sqrt{\frac{q}{4p}}\sigma = \sqrt{\frac{N}{4p^2}}\sigma \quad (18)$$

A comparison of the maximum standard deviation of INL_k for the basic DAC as given in (7) with the $\overline{INL_k}$ of the DDEM DAC as given in (18) will illustrate the level of reduction achievable with the Cyclic Switching Sequence for the DDEM structure. Consider n=18, $p=2^7=128$ and $q=2^{11}$. It thus follows that the maximum standard deviation of the Cyclic DDEM DAC is $\sqrt{\frac{q}{4p}}\sigma = 2\sigma$ LSB and that of the basic DAC is $\frac{\sqrt{N}}{2}\sigma = 2^8\sigma$ LSB. Thus although the Cyclic DDEM DAC is not perfectly linear, it has many points that lie exactly on the fit line and the standard deviation of the largest variant from the fit line is reduced by a factor of 2^7 as compared to that of the basic DAC.

Since $\frac{\sqrt{N}}{2}\sigma$ is generally much larger than $\sqrt{\frac{q}{4p}}\sigma$, it can be concluded that the average INL of the DDEM DAC, $\overline{INL}$, will be much smaller than the INL of the basic DAC. Furthermore, since $\overline{INL_k}$ for the Cyclic DDEM DAC is so small even with σ modestly large, the current sources in the DDEM DAC can be built without using large area.

Although we assumed in the above analysis that the current source variations are random, the DDEM method can reduce the effect of current source variations due to other errors such as gradient as well. This is because the summation of all N current source variations is 0 relative to the fit line, regardless the causes of the current source errors. The DDEM method simply uses this fact to realize error reduction. The Cyclic Switching Sequence can be implemented using only a shift register in which each element will control a current source element. The starting point in the register can be set by a simple digital logic.

3. SIMULATION RESULTS

For the following simulation results, ADCs have 16 bit resolution with INL around 0.5 LSB which means that our ADCs are almost 16 bit linear. The original 18 bit DACs without DDEM in simulation have only 13 bit linearity in the best case. The DAC output range is 2% bigger than the ADC input voltage range and noise bounded to ± 3 LSB was added to the DAC output. For this results P is set equal to 128.

We generated one particular 18 bit DAC with INL equal to 136 LSB and used it as the ramp signal generator to test the same 1000 ADCs. Figure 2 shows the histogram of the INL_k estimation errors. INL_k estimation error is defined as the maximum absolute error between the real INL_k and the estimated INL_k. Figure 3 plot the real INL versus estimated INL, where INL is defined as the maximum INL_k. In this case the DAC is used as a tester on a production environment.

For this particular DAC we can see that the INL_k error is around ¼ LSB which means that we can characterize 1000 16 bit linear ADCs using a 10 bit linear DAC with DDEM. Figure 3 shows a mapping between the real ADC INL (x axis) and the estimated INL (y axis). It arises from this figure that we can estimate the INL with less than ½ LSB errors while the estimated INL is always bigger than the real INL assuring that no deficient part will be sent to the customer.

In figures 4 and 5 simulation results for a BIST approach are shown. In this case each ADC has a correspondent DAC to test it. Figure 4 shows the INL_k estimation maximum absolute error distribution for 1000 ADC-DAC pairs, while in Figure 5 we plot real INL versus estimated INL.

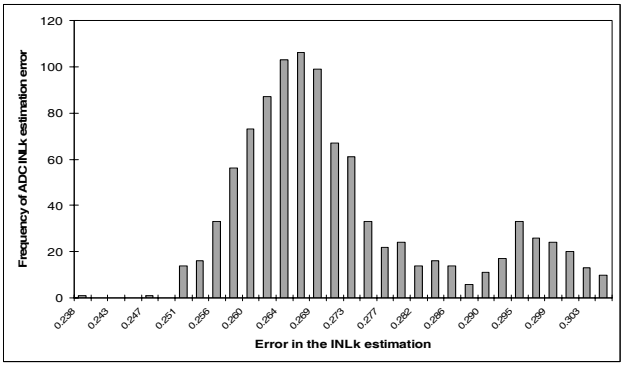

Figure 2: INL_k maximum absolute error distribution for 1000 16 bit ADCs.

These figures show that the error when characterizing the ADC is mostly bellow ½ LSB, which means that the INL_k estimation is close for all k transitions. On other hand we can see from Figure 5 that the estimation of the INL has also errors bellow ½ LSB and that in most cases the INL is overestimated, which assures that no bad parts is going to be shipped as a good one.

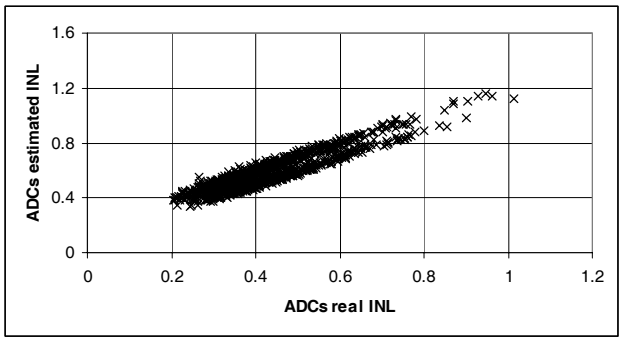

Figure 3: ADC real INL versus ADC estimated INL for 1000 16 bit ADCs.

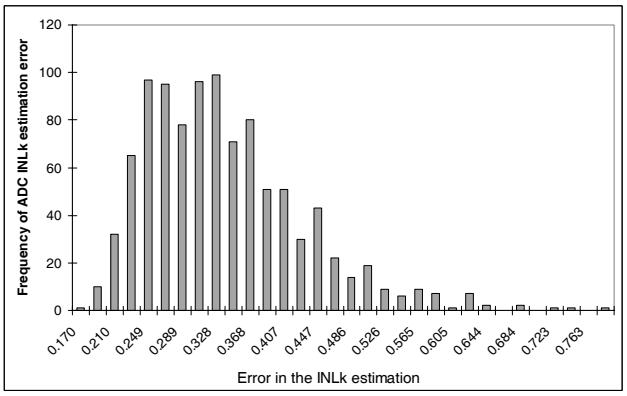

Figure 4: INL_k maximum absolute error distribution for 1000 ADC-DAC pairs.

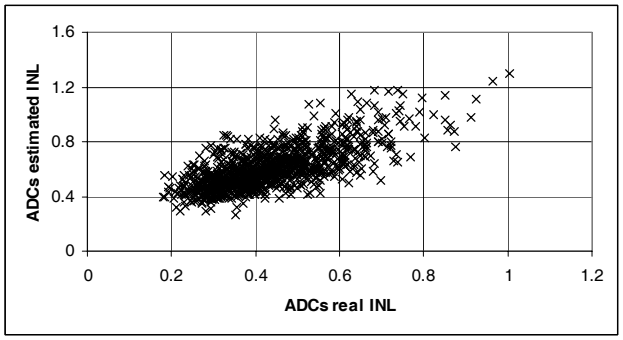

Figure 5: ADC real INL versus ADC estimated INL for 1000 ADC-DAC pairs.

4. SUMMARY

In this paper a Cyclic DDEM method for testing ADCs is characterized mathematically and also corroborated through simulations. It was shown by calculations that the Cyclic DDEM approach can significantly improve a DAC signal source's performance in the sense of much improved average linearity. It is also demonstrated that in the Cyclic DDEM testing approach, DACs that are substantially less accurate than the ADCs under test can be used to generate the test signal for the ADCs. Simulations showed that 16 bit linear ADCs can be tested with 13 or less bit linear DACs if Cyclic DDEM is applied to the DAC. Cyclic DDEM is not used in the real-time signal path, avoiding some of the limitations related to using DEM for real-time signal processing. Since this technique improves the signal generation it is not ADC architecture dependant. The DDEM technique offers potential for use both in BIST and production test environments. The linearity of the testing signal generator is relaxed since the DDEM will improve the signal quality, then the area required to implement it in silicon is small. This reduces cost in the production tester and allows the BIST implementation since we can achieve a highly linear signal on chip.

5. REFERENCES

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