A harmonic cancellation-based high-frequency on-chip sinusoidal signal generator with calibration using a coarse-fine delay cell

Ankush Mamgain, Salvador Mir, Jai Narayan Tripathi, Manuel Barragan

A harmonic cancellation-based high-frequency on-chip sinusoidal signal generator with calibration using a coarse-fine delay cell

Ankush Mamgain[1], Salvador Mir[1], Jai Narayan Tripathi[2], and Manuel J. Barragan[1]
[1]Univ. Grenoble Alpes, CNRS, Grenoble INP*, TIMA, F-38000 Grenoble, France
[2]Department of Electrical Engineering, Indian Institute of Technology Jodhpur, Jodhpur, Rajasthan, 342037, India

***Abstract*—An on-chip high-frequency sinusoidal signal generator with a calibration circuit based on a coarse-fine delay cell is presented in this work. The proposed signal generator is based on harmonic cancellation by adding scaled and time-shifted versions of a periodic signal. However, as we increase the target frequency of the generated signal, harmonic cancellation can be severely degraded by timing issues, degrading in turn the spectral purity of the generated signal. This paper proposes an architecture of a harmonic cancellation-based sinusoidal signal generator including a calibration circuit. The calibration circuit is based on a coarse-fine delay cell that can correct timing inaccuracies. Postlayout simulations of the proposed generator in FD-SOI 28 nm technology show a THD better than -60 dB in the frequency range from 173 MHz to 2 GHz.**

I. Introduction

The use of Built-In Self-Test (BIST) for Analog, Mixed-Signal and RF (AMS-RF) circuits is one of the solutions to improve yield in advanced nanometric processes. BIST circuits allow the characterization of internal blocks in highly integrated SoCs and SiPs and avoid the use of expensive AMS-RF testers. Moreover, advanced features like calibration and in-field testing in safety-critical applications can be enabled via AMS-RF BIST. In a wide variety of AMS-RF tests, a key element is the test stimulus generator. In particular, many analog test strategies are based on applying a sinusoidal signal with a high spectral quality as test stimulus. Therefore, on-chip sinusoidal signal generation can be identified as a key point for enabling AMS-RF BIST. In this regard, signal generators based on the harmonic cancellation principle have been extensively explored because they offer a highly linear output signal with reduced on-chip resources, in some cases mostly relying on digital circuits [1]–[12]. The harmonic cancellation process linearizes a periodic signal by combining time-shifted and scaled versions of the original periodic signal [13]–[15].

The work presented in [1] shows a Total Harmonic Distortion (THD) below -90 dB at 3 kHz and signals are generated using oscillators. However, the implementation is based on discrete components. The work in [2] presents an integrated solution based on the biquad filter with programmable inputs. The result shows a THD of -90 dB at 1 MHz. [3]–[7], [9] present a solution based on digital implementations in which time-shifted signals are generated using digital circuits, and scaling is done using a Digital-to-Analog Converter (DAC). [3], [4] use a digital counter that generates the time-shifted signals while scaling and addition are done using a current steering DAC. However, the mismatch from DAC can degrade the linearity of the output signal. To mitigate this, a partial dynamic element matching technique is employed. The results show a THD below -40 dB at 20 MHz [4].

A solution based on a skew circulant matrix-based coefficient generator for scalar weights is presented in [11]. The Spurious Free Dynamic Range (SFDR) reported is 66.8 dBc for 0.8 MHz and as frequency increases to 100 MHz, the SFDR degrades to 38.4 dBc. The focus of the work in [5], [7], [9] is on high-frequency signal generation in the order of MHz. The work in [7], [9] employ the circular shift register for time-shifted signals and a current steering DAC to scale and add these signals. A calibration scheme is also proposed to correct the scalar weights which achieves a THD of -46 dB at 330 MHz. In [5], the time-shifted signals are generated using a ring oscillator and these signals are scaled and added using a weighted resistor network connected with a capacitor. The authors have proposed a calibration circuit for correcting the timing issues. The results show a THD of -57 dB at 650 MHz and -62 dB at 750 MHz which are achieved after calibration.

In practical implementations, the accuracy of the scalar weights and the phase shifts limit the quality of the generated signal. Generally, advanced processes are prone to large process and mismatch variations and this leads to inaccurate scalar weights, time-shifts, and duty cycle of the signals. Also, as frequency increases the timing inaccuracies are significantly larger than the mismatch in scalar weights [10]. This paper presents a harmonic cancellation-based sinusoidal signal generator in which these timing errors at higher frequencies can be corrected with the help of a coarse-fine delay cell.

The rest of the paper is organized as follows. In Section II, the background of the harmonic cancellation principle is discussed. In Section III, the timing inaccuracies at a higher frequency are discussed along with the mitigation of these inaccuracies using a delay cell. In Section IV, the architecture along with simulation results are discussed. To conclude the paper, Section V summarizes our main contributions.

*Institute of Engineering Univ. Grenoble Alpes

II. Theoretical basis

As discussed in the previous section, in a harmonic cancellation-based sinusoidal signal generator a sinusoidal signal is generated by adding scaled versions of time-shifted periodic signals of the same frequency. Since the generation of digital square-wave signals is simple compared to other types of periodic signals, square-wave signals are considered in the following discussion. A periodic square-wave signal $q(t)$ with a unit amplitude and a 50% duty cycle can be represented as

$$q(t) = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2}{n\pi} (-1)^{\frac{n-1}{2}} \cos(n\omega_0 t), \tag{1}$$

where T and ω_0 are the time period and the angular frequency of the signal, respectively. Eq. (1) shows that only odd harmonics are present in the spectrum. Let us define a signal $y(t)$ which is a linear combination of p pairs of time-shifted versions of signal $q(t)$ in opposite directions t_i and $-t_i$ and scaled by a factor α_i as follows

$$y(t) = q(t) + \sum_{i=1}^{p} \alpha_i \left[q(t + t_i) + q(t - t_i) \right]. \tag{2}$$

By solving Eq. (1) and Eq. (2) we obtain

$$y(t) = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2}{n\pi} (-1)^{\frac{n-1}{2}} \left[1 + 2 \sum_{i=1}^{p} \alpha_i \cos(2n\pi \frac{t_i}{T}) \right] \times \cos(n\omega_0 t). \tag{3}$$

Eq. (3) represents the spectrum of the output square wave signal that is similar to the spectrum of the input square wave signal $q(t)$ in Eq. (1). However, the amplitude of the harmonic components in the output signal $y(t)$ depend on the applied time-shifts and scalar weights compared to the original input signal $q(t)$. Thus, by carefully selecting these time-shifts and the scalar weights, the coefficient of the harmonics can be made equal to zero. Multiple solutions of Eq. (3) can be achieved, in fact in a practical implementation, the lower order harmonics close to the fundamental frequency can be canceled with the help of the harmonic cancellation, while higher-order harmonics can be attenuated using a low-pass analog filter so that a good trade-off between the linearity of the output signal and the complexity of the design can be achieved [8]. A practical solution that represents a good trade-off consist of p=2 pairs of time-shifted signals (that is, 5 square-waves). The first pair is phase-shifted by $\phi_1 = \pm\frac{\pi}{6}$ and the second by $\phi_2 = \pm\frac{\pi}{3}$, while the first pair is scaled by $\alpha_1 = \frac{\sqrt{3}}{2}$ and the second by $\alpha_2 = \frac{1}{2}$. By choosing this solution, the lower order odd harmonics below the 10-th harmonic component of output signal $y(t)$ are cancelled. The timing diagram for these square-waves is shown in Fig. 1. Signal C is the reference signal where as signals A and B are advanced by $\frac{-\pi}{3}$ and $\frac{-\pi}{6}$, respectively, and signals D and E are delayed.

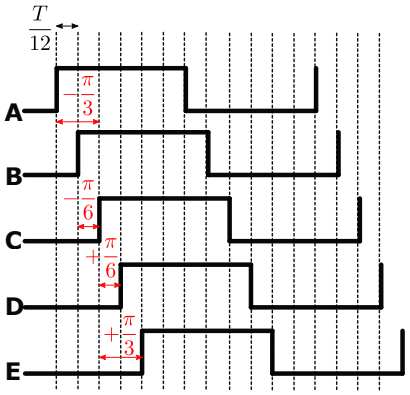

Fig. 1. Ideal timing diagram for harmonic cancellation.

III. Timing inaccuracies in high frequency and their mitigation

A. Timing inaccuracies in high frequency

Mismatch and process variations are unavoidable outcomes of the fabrication process. These variations can vary the timing parameters (the relative time-shift and duty cycle of the signal), and the scalar weights which affects the efficiency of the harmonic cancellation and can severely degrade the quality of the generated output signal. Theoretical analysis shows that in low frequency applications, the quality of the output is mainly limited by the inaccuracies in the scalar weights, while in high-frequency applications timing errors are responsible for the quality of the output signal [10].

Thus, the focus of the work in [1]–[4] is on the effect of mismatch on scalar weights for frequencies below 100 MHz, while the calibration of timing errors for signal generators operating at higher frequencies is discussed in [5], [10]. In [5], a binary weighted capacitor bank is used in each signal path and an external calibration loop is considered. These capacitor banks are phase-shifters that are used to compensate the phase and the duty cycle of time-shifted signals. The authors in [10] have used a pulse-width modification circuit to correct the duty cycle and a capacitor bank for phase correction. Although the capacitor bank is a practical solution for phase correction, the resolution of the unit capacitor in these works is a limitation. To address this limitation, in this work we make use of a coarse-fine tunable delay cell that takes advantage of the back bias capabilities of FD-SOI technology [16]. This delay cell is used to correct the discussed timing errors with a higher degree of resolution.

B. Delay cell with timing calibration

The schematic view of the delay cell is shown in Fig. 2 [17]. This delay cell presents a coarse-fine variable delay in which the coarse delay can be fixed with the help of a control gate voltage while the fine delay is controlled with the help of a body bias voltage. The first stage of the delay cell is a current starved inverter and the second stage is a gated inverter. The output of the second stage (Vf) acts as a feedback signal to the input of an inverter in parallel with the current starved

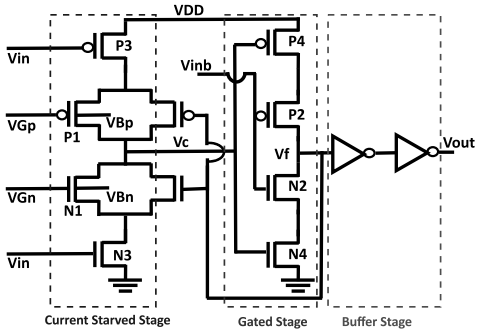

Fig. 2. Coarse-fine delay cell in FD-SOI technology.

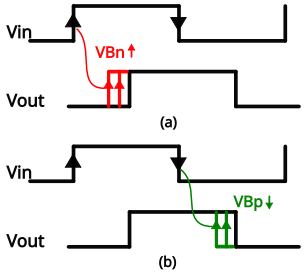

Fig. 3. (a) Phase change due to change in VBn. (b) Duty cycle change due to change in VBp.

inverter. Finally, inverters are cascaded after the second stage to drive the next stage.

The operation of delay cell can be explained as follows. As the input of delay cell rises from '0' to '1', the voltage of node Vc discharges slowly due to the current starving nature of the inverter till it reaches the threshold of the gated inverter in next stage. Once the input of the second stage crosses the threshold, the output of the second stage which is the feedback signal to the first stage cancels the current starving nature of the inverter by activating the inverter in parallel with it. The Vc node then discharges at a faster rate. The operation for the input voltage falling from '1' to '0' is similar.

In the nominal state, the delay cell is biased by setting the gate input voltage of transistors N1 and P1 in the current starved stage in such a way that the rise and fall times are the same. Then, the delay can be fine-tuned to the required value by changing the body bias of the NMOS (N1). When the body bias voltage VBn is increased, the threshold voltage of the N1 transistor decreases which reduces the fall time of the signal Vc (which is the rising edge of the input signal), thus the input signal advances as shown in Fig. 3(a). Similarly, when VBp is decreased, the falling edge of the input signal is advanced which changes the duty cycle of the input signal as shown in the Fig. 3(b). From these observations, it can be concluded that the timing errors can be corrected using this delay cell. It is worth noticing that the reduction of the threshold voltage is a feature of the FD-SOI technology, in which we have used LVT transistors, based on the flip-well scheme. The NMOS is built on an n-well while the PMOS is built on a p-well and a deep n-well is present to isolate the p-well of the PMOS from the global p-well. The p-well of the transistor P1 is isolated using deep n-well and the n-well of the transistor N3. Except transistors P1 and N1, the wells of other transistors are connected to ground.

IV. Practical Implementation and Results

The architecture of the sinusoidal signal generator with timing calibration is shown in Fig. 4. The square-wave signals with the required phase-shifts discussed in section II are generated from a 6-stage fully-differential ring oscillator. These signals are passed through a buffer stage and the output of the buffer stage is then fed to the coarse-fine delay cells for correction of timing errors. The output of each delay cell is connected to a single-to-differential signal converter, built as a double-ended digital buffer, to generate differential signals. The outputs of the single-to-differential stage are scaled and added using a weighted RC network. Additional output filtering is provided by a simple low pass filter (LPF) for attenuating higher-order harmonics. For more details, the readers can refer to [10]. The complete system has been implemented using STMicroelectronics 28 nm FD-SOI technology. The layout of the architecture is shown in Fig. 5. The area of design is $0.0113\,\mathrm{mm}^2$ excluding pads. Next, we validate the functionality of the implemented coarse-fine delay cell and the complete generator by transistor level and post-layout simulation results.

A. Delay cell characterization

In order to illustrate the functionality of the coarse-fine delay cell and its ability to correct the phase shift and duty cycle we performed electrical simulations of a standalone delay cell. Fig. 6 shows the delay as a function of VBn, for a fixed value of VGp$=0.2\,\mathrm{V}$ and sweeping VGn from $0.6\,\mathrm{V}$ to $1\,\mathrm{V}$. As it can be observed, when VBn increases from $0\,\mathrm{V}$ to $1.8\,\mathrm{V}$, the delay of the cell decreases. As VGn decreases, the sensitivity to delay change increases. The sensitivity is $2.77\,\mathrm{ps/V}$ when VGn is equal to $1\,\mathrm{V}$ while it increases to $28\,\mathrm{ps/V}$ when VGn is equal to $0.6\,\mathrm{V}$. This shows a wide range of resolution, ranging from fs to ps, for phase calibration. Of course the change in VGn also affects the duty cycle but this can be compensated by changing VGp. In this regard, Fig. 7 shows the duty cycle of the signal Vout versus VBp for different values of VGp while keeping VGn equal to $0.8\,\mathrm{V}$. When VBp decreases the duty cycle of the signal decreases. As VGp increases, the sensitivity of change in duty cycle increases. This sensitivity is $0.348\,\%/\mathrm{V}$ when VGp is equal to $0\,\mathrm{V}$ while it increases to $4.38\,\%/\mathrm{V}$ when VGp is increased to $0.4\,\mathrm{V}$ which is also a wide range of resolution for duty cycle correction. Thanks to the FD-SOI technology, a wide range of body-bias can be achieved compared to the bulk technology.

B. Simulation results of signal generator

The complete sinusoidal signal architecture in Fig. 4 has been simulated at transistor level. The values of the control voltages in the coarse-fine delay cell are optimized to minimize the THD of the generated output signal. Due to space constraints, the optimization algorithm is not detailed in this paper. Fig. 8 shows the THD as a function of the frequency of

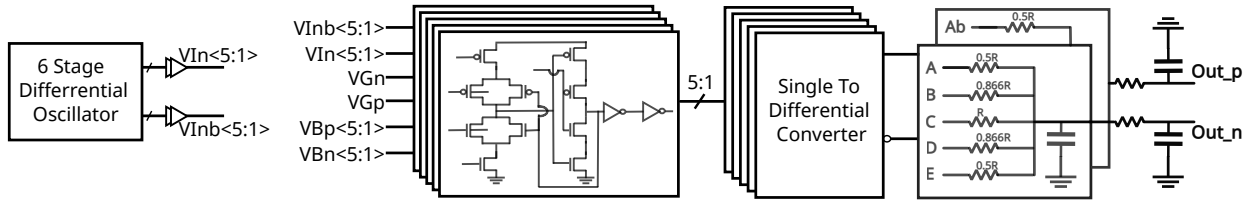

Fig. 4. Conceptual block diagram of the proposed sinusoidal signal generator with calibration.

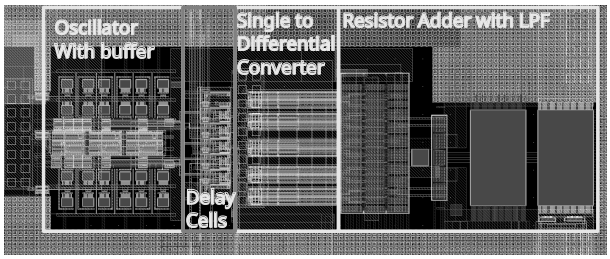

Fig. 5. Layout of the sinusoidal signal generator.

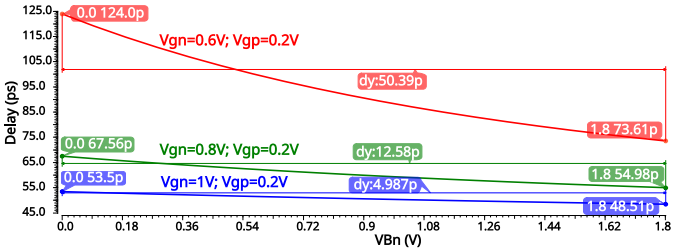

Fig. 6. Input-output delay as a function of body bias *VBn* and gate voltage *VGn* of transistor N1 of the delay cell.

the output signal before (red) and after (green) optimization of the control voltages, for frequencies ranging from 173 MHz to 2.73 GHz. It can be observed that the THD is improved to −56 dB at 173 MHz and improved to −66 dB at 2.73 GHz. This shows a significant improvement in all frequencies due to the calibration of timing issues. For frequencies greater than 500 MHz, the THD of the generated signal is consistently better than −60 dB. The frequency spectrum of the output signal generated in post-layout simulation is shown in Fig. 9. The THD after optimization improved by more than 20 dB with respect to the non-optimized one, with a value of −62 dB at 1.99 GHz.

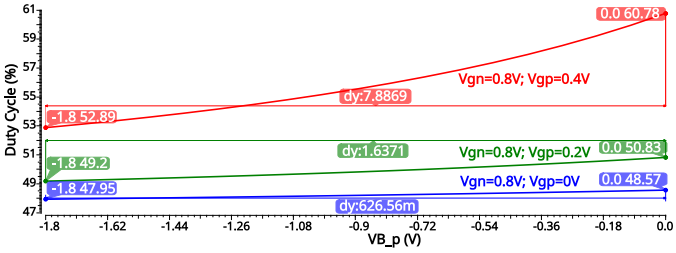

Fig. 7. Output duty cycle as a function of body bias *VBp* and gate voltage *VGp* of transistor P1 of the delay cell.

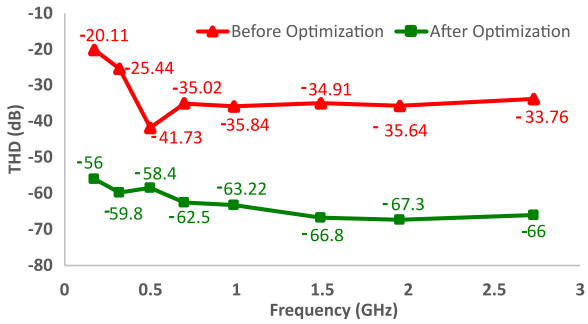

Fig. 8. THD of the generated signal before and after optimization as a function of the output frequency.

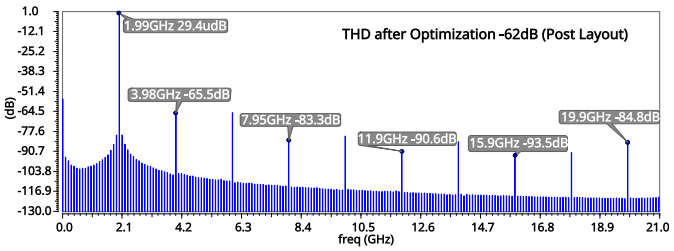

Fig. 9. Output signal spectrum after calibration of timing issues.

V. Conclusions

A harmonic cancellation-based sinusoidal signal generator with calibration of timing errors using a coarse-fine delay cell is proposed in this work. The timing errors (phase mismatch and duty cycle error) severely degrade the quality of the sinusoidal signal in a conventional harmonic cancellation-based signal generator. A coarse-fine delay cell with a wide range has been proposed to compensate these timing errors, which improves on previous solutions based on discrete phase-shifters. The proposed generator has been implemented using STMicroelectronics 28 nm FD-SOI technology. Simulation results show that compensation of timing errors results in a significant improvement of the linearity of the generated signal. A THD better than −60 dB can be achieved for a wide range of output frequencies from MHz to GHz.

Acknowledgements

This work has been carried out in collaboration with STMicroelectronics within the Nano2022 research program. We are grateful to Jean-Baptiste Moulard and Fabien Granoux for their help in chip fabrication.

REFERENCES

[1] B. Karthik Vasan, S. K. Sudani, D. J. Chen, and R. L. Geiger, "Low-distortion sine wave generation using a novel harmonic cancellation technique," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1122–1134, 2013.

[2] M. J. Barragan, G. Leger, D. Vazquez, and A. Rueda, "On-chip sinusoidal signal generation with harmonic cancellation for analog and mixed-signal BIST applications," *Analog Integrated Circuits and Signal Processing*, vol. 82, no. 1, pp. 67–79, 2015.

[3] P. Aluthwala, N. Weste, A. Adams, T. Lehmann, and S. Parameswaran, "Design of a digital harmonic-cancelling sine-wave synthesizer with 100 mhz output frequency, 43.5 db sfdr, and 2.26 mw power," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2015, pp. 3052–3055.

[4] P. D. Aluthwala, N. Weste, A. Adams, T. Lehmann, and S. Parameswaran, "Partial dynamic element matching technique for digital-to-analog converters used for digital harmonic-cancelling sine-wave synthesis," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 2, pp. 296–309, 2017.

[5] C. Shi and E. Sánchez-Sinencio, "150–850 mhz high-linearity sine-wave synthesizer architecture based on fir filter approach and sfdr optimization," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 9, pp. 2227–2237, 2015.

[6] ——, "On-chip two-tone synthesizer based on a mixing-fir architecture," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 8, pp. 2105–2116, 2017.

[7] H. Malloug, M. J. Barragan, S. Mir, L. Bastères, and H. Le Gall, "Design of a sinusoidal signal generator with calibrated harmonic cancellation for mixed-signal bist in a 28 nm fdsoi technology," in *2017 22nd IEEE European Test Symposium (ETS)*, 2017, pp. 1–6.

[8] H. Malloug, M. J. Barragan, and S. Mir, "Practical Harmonic Cancellation Techniques for the On-Chip Implementation of Sinusoidal Signal Generators for Mixed-Signal BIST Applications," *Journal of Electronic Testing: Theory and Applications*, vol. 34, no. 3, pp. 263–279, 2018.

[9] ——, "A 52 db-sfdr 166 mhz sinusoidal signal generator for mixed-signal bist applications in 28 nm fdsoi technology," in *2019 IEEE European Test Symposium (ETS)*, 2019, pp. 1–6.

[10] A. Mamgain, M. J. Barragan, and S. Mir, "Analysis and mitigation of timing inaccuracies in high-frequency on-chip sinusoidal signal generators based on harmonic cancellation," in *2021 IEEE European Test Symposium (ETS)*, 2021, pp. 1–6.

[11] G. G. Garayar-Leyva, H. Osman, J. J. Estrada-López, and E. Sánchez-Sinencio, "A harmonic-canceling synthesizer using skew-circulant-matrix-based coefficient generator," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2020, pp. 1–5.

[12] G. G. Garayar-Leyva, H. Osman, J. J. Estrada-López, and O. Moreira-Tamayo, "Skew-circulant-matrix-based harmonic-canceling synthesizer for bist applications," *Sensors*, vol. 22, no. 8, 2022. [Online]. Available: https://www.mdpi.com/1424-8220/22/8/2884

[13] E. Mensink, E. A. M. Klumperink, and B. Nauta, "Distortion cancellation by polyphase multipath circuits," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 52, no. 9, pp. 1785–1794, Sept. 2005.

[14] E. Seok, C. Cao, D. Shim, D. J. Arenas, D. B. Tanner, C.-M. Hung, and K. K. O, "A 410ghz cmos push-push oscillator with an on-chip patch antenna," *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, pp. 472–629, 3-7 Feb. 2008.

[15] Y.-L. Tang and H. Wang, "Triple-push oscillator approach: theory and experiments," *Solid-State Circuits, IEEE Journal of*, vol. 36, no. 10, pp. 1472–1479, Oct 2001.

[16] S. Clerc, T. Di Gilio, and A. Cathelin, *The Fourth Terminal: Benefits of Body-Biasing Techniques for FDSOI Circuits and Systems*. Springer, 2020.

[17] A. C. L. C. I. Sourikopoulos, A. Frappe and A. Kaiser, "A digital delay line with coarse/fine tuning through gate/body biasing in 28nm fdsoi," *42nd European Solid-State Circuits Conference (ESSCIRC)*, pp. 145–148, Sept. 2016.