

Session 14 Overview: *Digital PLLs and Building Blocks*

High-Performance Digital Subcommittee



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The nine papers presented in this session highlight developments in clock generation and distribution, on-die sensors, cross-die communication, and timing margin recovery. These designs implement functions traditionally constructed with analog techniques, but now leveraging digital architectures to improve PVT tolerance, area, power efficiency, and enable rapid process migration and technology adoption.

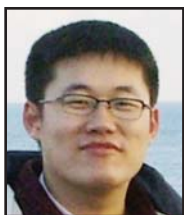


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14.1 A 0.022mm² 970μW Dual-Loop Injection-Locked PLL with -243dB FOM Using Synthesizable All-Digital PVT Calibration Circuits

W. Deng, Tokyo Institute of Technology, Tokyo, Japan

In Paper 14.1, the Tokyo Institute of Technology presents a 0.022mm² 970mW dual-loop injection-locked PLL implemented in 65nm CMOS and using all-digital PVT-calibration circuits. The small area is achieved using a TDC-less digital FLL with injection locking. The PLL uses both a main loop and a replica loop for PVT tracking resulting in 0.7ps_{RMS} jitter.



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14.2 A 0.032mm² 3.1mW Synthesized Pixel Clock Generator with 30ps_{rms} Integrated Jitter and 10-to-630MHz DCO Tuning Range

W. Kim, Seoul National University, Seoul, Korea

In Paper 14.2, Seoul National University and Samsung present a 0.032mm² 3.1mW synthesized pixel-clock generator in 28nm CMOS based on an all-digital dual-loop PLL. The 250MHz pixel clock is generated from a 100kHz input and exhibits 30ps_{rms} jitter. The synthesized DCO shows 0.37ps resolution and 1.8LSB differential non-linearity, with a PVT-compensated wide tuning range (10 to 630MHz) and locks within 120 input cycles.



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14.3 An All-Digital PLL Using Random Modulation for SSC Generation in 65nm CMOS

N. Da Dalt, Infineon Technologies, Villach, Austria

In Paper 14.3, Infineon Technologies presents a CMOS digital PLL, which uses random modulation to generate a spread-spectrum clock (SSC). It reduces accumulated jitter by 8× with respect to an equivalent triangular modulation without penalty in EMI reduction. The DPLL is implemented in 65nm CMOS, occupies 0.23mm², and draws 5mA at 500MHz output.



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14.4 A 0.026mm² 5.3mW 32-to-2000MHz Digital Fractional-N Phase Locked-Loop Using a Phase-Interpolating Phase-to-Digital Converter

T-K. Jang, Samsung Electronics, Yongin, Korea

In Paper 14.4, Samsung Electronics presents a 28nm CMOS digital PLL, which introduces a phase-interpolating phase-to-digital converter, calibration-free DSM noise canceller and supply-insensitive DCO. The DPLL occupies 0.026mm² and consumes 2.2 to 5.3mW at 1-to-2GHz output frequencies. Measured RMS integrated jitter in integer mode is 20ps and in fractional mode is 26ps.



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14.5 A 2.5GHz 2.2mW/25μW On/Off-State Power 2ps_{rms}-Long-Term-Jitter Digital Clock Multiplier with 3-Reference-Cycles Power-On Time

T. Anand, Oregon State University, Corvallis, OR

In Paper 14.5, Oregon State University presents a digital clock multiplier targeting mobile SoC platforms and servers. It achieves rapid turn-on by accurate frequency presetting and reference insertion. Fabricated in a 90nm CMOS process, the prototype achieves 2ps_{rms} jitter, while consuming 2.2mW/25μW on/off-state power from a 1.1V supply with 12pJ energy overhead due to power cycling at 2.5GHz output frequency.



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14.6 3D Clock Distribution Using Vertically/Horizontally-Coupled Resonators

Y. Take, Keio University, Yokohama, Japan

In Paper 14.6, Keio University presents a 0.18μm 3D wireless clock system which distributes a 1.1GHz clock across stacked chips using vertically-coupled LC oscillators and horizontally-coupled ring oscillators. Clock skew is <18ps for a 1.8V supply, and <25ps for a 0.9V supply, with RMS jitter <1.72 ps. The proposed frequency-locking and phase-pulling scheme widens the lock range to ±10% at a power dissipation of 196mW at 0.9V.

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14.7 All-Digital Hybrid Temperature Sensor Network for Dense Thermal Monitoring

S. Paek, KAIST, Daejeon, Korea

In Paper 14.7, KAIST presents a 0.13μm 1.2V CMOS distributed digital-thermal sensing network. This design combines a small number of accurate thermal sensors with a large number of tiny relative thermal sensors, achieving an average area of 2578μm² per sensing point. By combining these sensor outputs, a thermal-map up-sampler synthesizes a higher-spatial-resolution thermal map. Silicon results demonstrate an average error of 0.2°C over a sensing area of 3.24mm² resulting in a 57.7% area reduction versus prior art.



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14.8 A 95fJ/b Current-Mode Transceiver for 10mm On-Chip Interconnect

S-K. Lee, Pohang University of Science and Technology, Pohang, Korea and Samsung Electronics, Hwasung, Korea

In Paper 14.8, Pohang University, Samsung and the University of Michigan describe a current-mode transceiver for on-chip global interconnects, implemented by series stacking of a current-sensing load as the receiver and an open-drain driver as the transmitter. The transceiver is fabricated in 65nm CMOS and achieves 95fJ/b at 3Gb/s and 0.9V and 108fJ/b at 4Gb/s and 1.0V over a 10mm link with a BER of less than 1E-12.



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14.9 Razor-Lite: A Side-Channel Error-Detection Register for Timing-Margin Recovery in 45nm SOI CMOS

S. Kim, University of Michigan, Ann Arbor, MI

In Paper 14.9, The University of Michigan introduces "Razor-Lite" for timing-margin recovery. This approach reduces area and energy overhead of previous error-detection and correction schemes using a simple 8-transistor transition detector integrated in a flip-flop. This is done with an energy/area overhead of 2.7%/33%. The technique is validated in a 45nm SOI 7-stage pipeline Alpha processor, showing energy efficiency gains of 83% over a baseline design at 1.2GHz and 1.1V, with 4.42% core area overhead.