Curvature of BEOL Cantilevers in CMOS-MEMS Processes

Juan Valle, Daniel Fernández, Jordi Madrenas and Laura Barrachina

***Abstract*—This article presents the curvature characterization results of released back-end-of-line (BEOL) 5 µm-wide cantilevers for two different 0.18 µm 1P6M complementary metal–oxide semiconductor microelectromechanical systems (CMOS-MEMS) processes. Results from different runs and lots from each foundry are presented. The methodology and accuracy of the characterization approach, based on optical measurements of test cantilever curvature are also discussed. Special emphasis is given to the curvature average and variability as a function of the number of stacked layers. Analytical equations for modeling the bending behavior of stacked cantilevers as a function of the tungsten (W) vias that join the metal layers are presented. In addition, the effect of various post-processing conditions and design techniques on the curvature of both single and stacked cantilevers is analyzed. In particular, surpassing certain time-dependent temperature stress conditions after release lead to curvature shifts larger than one order of magnitude. Also, the W via design was found to strongly affect the curvature of the test cantilevers.**

***Index Terms*—CMOS-MEMS, Bending Stiffness, Curvature, Stacks, Temperature, Test Cantilevers**

I. Introduction

Monolithic integration of CMOS electronics and MEMS devices can potentially reduce fabrication costs and achieve smaller size and lower parasitics than other integration approaches. One way to achieve CMOS-MEMS monolithic integration is by using the back-end-of-line (BEOL) layers of the CMOS process as structural layers for the MEMS device (CMOS-MEMS micromachining) [1, 2].

One of the main concerns of CMOS-MEMS processes is the curvature of the released BEOL structural layers [3–5], which is caused by the residual stresses and thermal coefficient mismatches of the different layers that form each BEOL layer. These are not tightly monitored or controlled by the CMOS foundries [6] given that their effects mostly arise after a release step only necessary for MEMS fabrication and, therefore, do not pose a strong concern for the reliability of standard CMOS circuits. Unfortunately, this curvature is typically large and, most importantly, its repeatability is poor as we shall see in section V. These limitations impose device size limits and therefore reduce the range of valid MEMS designs compared to other MEMS processes [4, 7, 8]. The variability of process and design parameters is particularly important in the case of commercial devices, which need to achieve the required levels of performance in the full range of process variability. The curvature of the BEOL layers plays a very important role in this sense and, although there are plenty of works dealing with curvature and residual stresses [5, 9–14], no large studies regarding the curvature of the BEOL metal layers of CMOS-MEMS processes are available in the literature.

A well-known method to achieve flatter CMOS-MEMS structures is layer stacking or composite cantilevers [2, 5, 9, 15], but statistical data, curvature variability and mathematical description of the mechanical bending behaviour is not presented in these studies. In addition, although analytical modeling of multilayered structures was presented in [16], analytical formulas for modeling the bending behavior when the layers are joined with vias is not found in the literature. Thus, curvature characterization of single and composite cantilevers of CMOS-MEMS processes joined with tungsten (W) vias is one of the main objectives of this paper.

In this work we analyze the limitations of test cantilever curvature measurement and the effect on curvature of different processing conditions, like etch time or temperature history, and design variations, such as W via design or layer stacking. A large database is constructed from all the analyzed samples from two different CMOS-MEMS processes. We will begin by describing the CMOS-MEMS fabrication process in section II. Then, the general relationship between curvature and residual stress is briefly introduced in section III. The characterization methodology employed in this paper and its limitations are explained in section IV, where analytical equations that describe the mechanical bending behaviour and curvature of metal stacks joined with W vias are also presented. The results are discussed in section V, where the effects on curvature of thickness variations, several processing conditions and design variations are discussed. In particular, the effects on final curvature of past temperature stress and of different via design that join the BEOL metal layers are studied in detail.

II. CMOS-MEMS fabrication process

The CMOS process flow can be divided in two parts: the front-end-of-line (FEOL), where the active devices, mainly transistors, are built; and the BEOL, where the metal interconnecting layers are deposited. The CMOS-MEMS devices studied in this article are built with the BEOL materials. Initially, as fabricated by the CMOS foundry, the MEMS structures are surrounded by the BEOL inter-metal dielectric

J. Valle and J. Madrenas are with the Department of Electronic Engineering, Universitat Politècnica de Catalunya, Jordi Girona 1 i 3, Edifici C4, 08034 Barcelona, Spain (e-mail: juan.valle.fraga@gmail.com, jordi.madrenas@upc.edu)

D. Fernández is with Nanusens, Av. del Parc Tecnològic 3, CENT - Parc Tecnològic del Vallès, 08290 Cerdanyola del Vallès, Spain (e-mail: daniel.fernandez@nanusens.com)

L. Barrachina is with Owlstone, 127 Cambridge Science Park, Milton Road, Cambridge CB4 0GD, United Kingdom (e-mail: laura.barrachina@owlstone.co.uk).

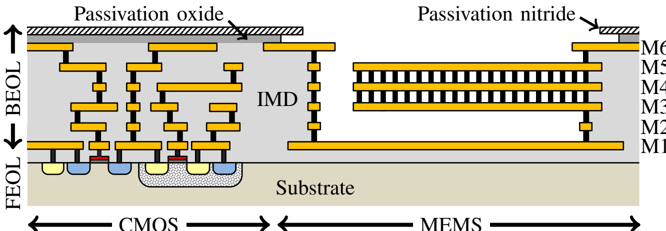


Figure 1: Cross section of a cantilever made of a stack of layers M3, M4, M5 and the W vias that join them (in black) after the vHF release process in a typical 0.18 µm 1P6M CMOS process. The vHF is masked by the passivation nitride layer (dashed) that only allows IMD oxide etching in the MEMS area. Note the cavity around the cantilever used to confine the etching.

Metal cross section		LF	GF
a (Ti/TiN)	M1-M5 t (nm)	400±40	570±57
	M1-M5 a (nm)	40±15	60±15
b (Al-based)	M1-M5 b (nm)	320±32	440±44
	M1-M5 c (nm)	40±15	70±15
c (Ti/TiN)	M6 t (nm)	900±90	900±90
	Gap bewteen metals (nm)	500±50	900±90

Table I: MEASURED BEOL THICKNESSES.

(IMD) oxide. The sacrificial IMD oxide is etched away with a vapor HF (vHF) process [17] that does not etch the BEOL metals, releasing the MEMS structures as in figure 1, and providing them with their functionality, i.e., freedom to move or others. After the vHF release some impurities are left from the etching reaction [17], which can be removed with a baking step, which typically consists on rising the temperature to 250 °C approximately during one minute. The BEOL materials may be combined in several ways when creating the MEMS structure. For example, a single layer of metal may be used, or several layers of metal may be stacked with the aid of vias as shown in figure 1. Other ways may be possible, depending on the specific options of the CMOS-MEMS process. Finally, the MEMS devices are sealed, diced and packaged [18].

While 0.18 µm CMOS technologies are currently the sweet spot (lowest overall cost) for mixed-signal applications, a large number of BEOL metal layers improves MEMS design flexibility. For these two reasons, and for widening the generality of this work, two 1P6M 0.18 µm CMOS processes were used: one from Global Foundries (GF) and another from LFoundry (LF). In terms of MEMS design, the main difference between both processes is the thickness of the BEOL metal layers and the gaps between them, being greater for the GF process. Typically, thicker layers lead to reduced curvatures, greater stiffness and larger minimum separation between features. Which process is the best suited will be determined by the requirements of the MEMS application.

The BEOL metal layers of the two CMOS processes used have the same base materials (Al-based alloy, Ti and TiN). The metal layers are generally labeled according to the deposition order (metal 1 is the bottom metal layer and metal 6 is the top layer). The thickness of the BEOL layers was measured with focused-ion-beam (FIB) cuts, which cannot distinguish between Ti and TiN layers, yielding the results of table I, where the error is never lower than 10 % to account for the typical BEOL thickness variations in CMOS processes.

III. WHY THIN FILMS CURVE

After release, the initially flat cantilevers of a CMOS-MEMS process curl up or down depending on their initial residual stresses. Residual stress may arise from intrinsic stress gradients originated during the formation of the cantilever, or from thermal coefficient mismatches (different materials, same material but slightly different deposition conditions, etc.).

The average residual stress creates an expansion or contraction force F that will lead to the corresponding cantilever expansion or contraction when it is not constrained. Likewise, nonuniform axial residual stress (usually referred to as residual stress gradient) creates a bending moment M, which will curl the cantilever when it is not constrained. Mechanical equilibrium relates the expansion force F and the bending moment M caused by the initial residual stress distribution σ as described by the following equations [19]:

$$F = -\int_A \sigma \, \mathrm{d}A = 0 \tag{1}$$

$$M = \int_A \sigma z \, \mathrm{d}A = 0 \tag{2}$$

where A is the cross-sectional area and z the distance to the neutral axis (the axis at which strain and stress are zero when the beam is subjected to bending when no initial residual stress is present.)

The expansion force F produces a length increment ΔL equal to [19]:

$$\Delta L = \frac{FL}{EA} \tag{3}$$

where L is the cantilever length and E the Young's Modulus.

Also, the bending moment M produces a curvature K, which are related by the so-called moment-curvature equation [19]:

$$K = \frac{M}{EI} \tag{4}$$

where E is the Young Modulus and I the second moment of area of the beam's cross section. The product EI is usually called flexural rigidity or bending stiffness, and it is proportional to the spring constant of beams under bending when the residual stress effect is negligible.

IV. CURVATURE CHARACTERIZATION METHOD

A. Measurement Setup

The curvature characterization was performed by measuring the curved profile of test cantilevers uniformly distributed over the wafers in order to extract with-in-wafer (WIW) uniformity. The topography of the test cantilevers after release (see figure 2a) was measured optically with a Reflection Digital Holographic Microscope (DHM) from Lyncée-Tec [20]. These type of microscopes record holograms like in figure 2b, which contain both the intensity and the phase of the incident

light, allowing digital focusing during post-processing and precise curvature measurements. Due to surface roughness, residues and image quality our vertical resolution was around 10 nm, while the horizontal resolution was around 1.5 µm, which proved enough for our purposes. All the holograms were taken automatically at wafer level with the aid of a Cascade probe station 12000b assembled with Lyncée-tec's DHM R1000 allowing us to perform automatic on wafer measurements. All measurements were performed in a clean room controlled environment at 22 °C and 45% of relative humidity. The profiles of the test cantilevers were extracted from their corresponding holograms automatically with Matlab using an image recognition algorithm. Then, the extracted profiles were fitted to a circumference, obtaining, this way, the curvature radius R and the curvature $K = 1/R$ of the cantilevers. The fit was generally very good, as expected for cantilevers with uniform curvature along their length. How circular the cantilever profile is was quantified with the circularity parameter, defined as the distance between the two closest concentric circles that enclose the cantilever profile, and defined as:

$$Circularity = \min_{\forall(x_c,y_c)} (R_a - R_b) \quad (5)$$

where (x_c, y_c) are the center coordinates of two concentric circles with radii R_a and R_b, which satisfy:

$$y_c+\sqrt{R_a^2 - (x - x_c)^2} \leq y(x) \leq y_c+\sqrt{R_b^2 - (x - x_c)^2} \quad (6)$$

for $0 \leq x \leq L$, and where $y(x)$ is the cantilever profile.

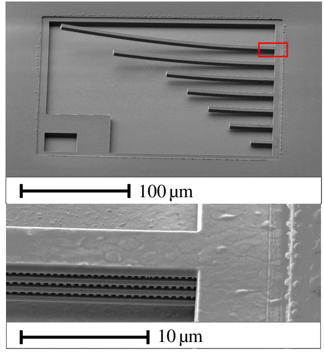
The smaller the circularity, the better the cantilever follows a circular shape. In practice, it is not zero due to several factors, like surface roughness, measurement noise and curvature non-uniformity along the length of the cantilever. In order to determine if curvature is the most important contributor to cantilever profile, the measured circularity values will be compared in section V-B with the theoretical tip displacement (z_{tip}) due to curvature of the measured cantilevers, which is:

$$z_{tip} = \frac{2}{K} \sin^2\left(\frac{KL}{2}\right) \approx \frac{KL^2}{2} \text{ for } KL \to 0 \quad (7)$$

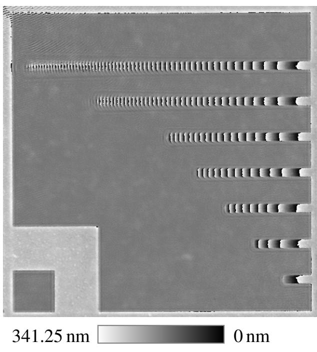
where K and L are the cantilever curvature and length, respectively. A zero initial slope at the anchor point is assumed.

B. Test Structure Design and Modeling

Clamped-free cantilevers were used for monitoring the BEOL metal layers curvature after vHF release. Each BEOL metal layer (M2, M3, M4, M5 and M6) had its corresponding test cantilevers, which were grouped in arrays of 7 cantilevers (see figure 2a), each of a different length. Several lengths are needed in order to deal with very different curvature values. The cantilever width needs to be large enough to be compatible with the horizontal resolution of the measuring optical system and to avoid low aspect ratio effects that can take place when the width is comparable to the thickness of the layer and which can influence the curvature of the cantilever [4, 21]. The width also needs to be thin enough to avoid undesirable anchor and



(a) SEM image (top) and zoomed region at the anchor (bottom).



(b) Hologram after release.

Figure 2: Test Cantilevers of metals M3456 after release. Taken from Half of Wafer 2, Lot 1, Run 1, LFoundry.

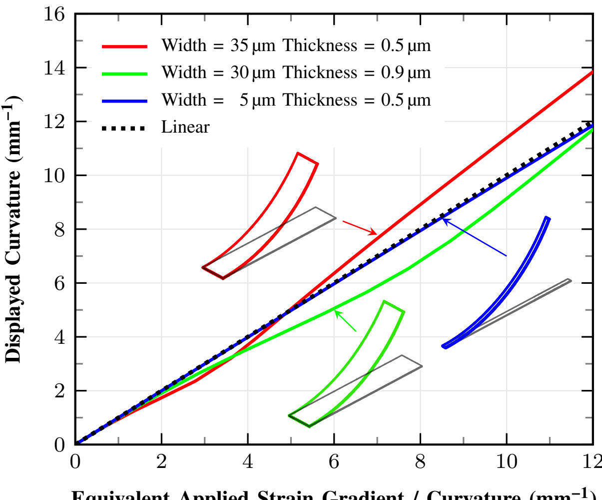


Figure 3: ANSYS simulation results showing the non-linear relationship between applied gradient strain and curvature for three clamped-free cantilevers of different widths and thicknesses (Length = 200 µm, Poisson's ratio = 0.3). Non-linearities are significantly more pronounced for the wider and thinner cantilevers, but are negligible below 1 mm^{-1}.

non-linear effects (see figure 3) which would prevent making a readily linear correspondence between curvature and gradient stress or strain. The width was chosen to be 5 µm, which complied with both requirements. Typically, no appreciable curvature dependence on cantilever width was observed for moderate curvature levels and cantilevers ranging from 5 µm to 30 µm, as in the case shown in figure 4. The used lengths were 20 µm, 40 µm, 60 µm, 80 µm, 100 µm, 150 µm and 200 µm.

In our experience, the curvature along x and y directions was the same when the structure was free to curve and the curvature was small enough to avoid geometrical non-linearities, so curvature characterization along more than one direction would be redundant.

Also, CMOS-MEMS cantilevers (and other structures) may be composed of several layers joined with W vias, here referred to as stacked cantilevers. For example, M234 is the short for a stack made of metal layers 2, 3 and 4. Metal stacks are very useful for reducing the curvature [2] at the expense of

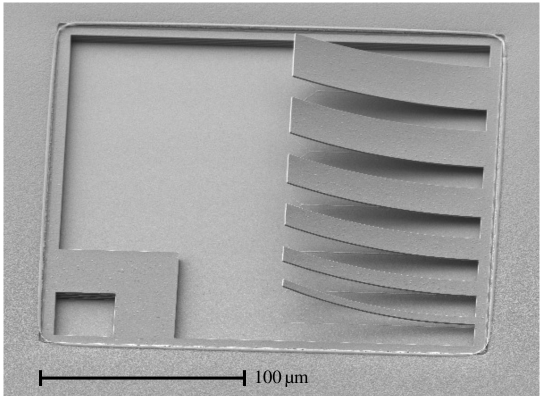


Figure 4: SEM image showing released 100 µm-long M6 cantilevers of different widths (5, 10, 15, 20, 25 and 30 µm). Note that their curvature (≈ 3 mm^{-1}) does not appreciably depend on the cantilever width. Taken from Half of Wafer 2, Lot1, Run 1, LFoundry.

higher bending stiffness as described by equation 4. Statistical curvature data of all the possible stacks is, therefore, very interesting, so the corresponding test cantilevers were included in all analyzed wafers. These are different from the stacks used in other CMOS-MEMS processes as in this study only metals are used, and there is no oxide surrounding the metal layers as in [3, 9, 22–24], which is not possible in our case due to our release process characteristics. The typical stacks used in this work are metal cantilevers joined by W vias distributed in a rectangular array as they are commonly used in CMOS designs. However, other non-standard via designs were tested and are described in section V-J.

Using equations 2 and 4, the bending stiffness of the stacks (EI_{stack}) as a function of the number of stacked layers was calculated analytically and is shown in table II. The coefficient α accounts for the type of W via design used for joining the metal layers, which has to be determined numerically or empirically. For a solid W layer between the metal layers $\alpha = 1$. Interestingly, for the rectangular W via array used in this work, numerical simulations show and experiments indicate (see section V-J) that the W vias do not contribute to EI_{stack}, in which case $\alpha \sim 0$. This, and other W via designs for which $1 > \alpha > 0$ are further discussed in section V-J. In addition, E_{LF}, I_{LF}, E_{GF} and I_{GF} stand for the effective Young's modulus and inertia moment of a single metal layer of LF and GF processes; t and w are the considered thickness and width, respectively. Coefficient γ is equal to the ratio E_W/E, where E_W and E are the Young's modulus of the via material and the effective Young Modulus of a single metal layer (E_{LF} or E_{GF}). Columns 3 and 4 show the EI values for LF and GF stacks, and are expressed in two different ways: the top line compares EI_{stack} to the EI of a single layer, and the second line is useful for modeling the stack as a solid beam with an equivalent Young's Modulus ($0.93E$ for a LF 2-metal stack, for example).

The deformation of a 2-metal stack from GF due to electrostatic actuation was used to calculate the effective Young modulus of the stack by comparison with FE simulations of a solid beam, which yielded $E_{2metals}$ =180±20 GPa. Applying the corresponding coefficient from table II (0.92), the effective Young's modulus of a single metal layer from GF was calculated, yielding E_{GF} =196±22 GPa.

Using equation 4, the curvature of a stack (K_{stack}) can be estimated from the curvature of the single metals (K_i), their average residual stress (σ_i) and the bending moment produced by the vias (M_{Wj}), as described by the following equation:

$$K_{stack} = \sum_i K_i \frac{EI_i}{EI_{stack}} + \sum_i \frac{\sigma_i\ t_i\ w\ z_i}{EI_{stack}} + \sum_j \frac{M_{Wj}}{EI_{stack}} \quad (8)$$

where, EI_i and EI_{stack} are the bending stiffness of the ith layer and the stack, respectively, defined in table II; w is the cantilever width, and t_i and z_i are the thickness and z position of the ith layer center with respect to the neutral axis, respectively.

C. Accuracy and Limitations

Although curvature displayed by the cantilevers is measured optically, not all cantilever lengths are suitable for curvature monitoring: short cantilevers may be too flat (high curvature measurement error) and long ones too curved (touching the substrate or exceeding maximum slope measurable by the DHM). These limitations are discussed in the following.

1) Condition 1: Avoid touching the substrate. In order to avoid touching the substrate, the length L of a test cantilever must be:

$$L < \frac{1}{|K|} \arcsin\left(|K| \sqrt{\left(\frac{2}{|K|} - g\right) g}\right) \quad (9)$$

for an initial gap g between the test cantilever and the substrate, and a negative curvature K.

Since typically the radius of curvature is much larger than the distance to the substrate ($1/K \gg g$), the previous condition may be simplified to:

$$L < \sqrt{\frac{2g}{|K|}} \quad (10)$$

For example, figure 5 shows that cantilevers larger than 60 µm touch the m1 substrate, so 60 µm-long cantilevers were used in that case.

2) Condition 2: Maximum slope. Holograms taken by the DHM are composed of fringes (see figure 2b) that correspond to different z-positions of the analyzed surface. Each fringe represents a vertical range of 341.25 nm. Larger slopes lead to narrower fringes that may be beyond the horizontal resolution of the measurement setup. Therefore, when a given slope is reached the cantilever profile cannot be measured as shown in figure 6. Experimental data showed that, in our setup, the maximum measurable slope (y'_m) was around 0.2. This imposes a relationship between the curvature and the maximum measurable length of the test cantilevers, which is:

$$L < \frac{1}{|K|} (\theta_m - \theta_i) \approx \frac{0.1}{|K|} \quad (11)$$

Number of layers	Stack Bending Stiffness (EI_{stack}) Analytic Formula	EI_{stack} ($\alpha = 0$) LF ($\frac{g}{t} \sim 1.25$)	GF ($\frac{g}{t} \sim 1.58$)
1	$EI = E\frac{1}{12}wt^3$	$1 \cdot E_{LF}I_{LF}$ $I_{LF} = I(t = 0.40\,\mu\text{m})$	$1 \cdot E_{GF}I_{GF}$ $I_{GF} = I(t = 0.57\,\mu\text{m})$
2	$EI\left[8 + 12\left(\frac{g}{t}\right) + 6\left(\frac{g}{t}\right)^2 + \alpha\gamma\left(\frac{g}{t}\right)^3\right]$	$32 \cdot E_{LF}I_{LF} =$ $0.93 \cdot E_{LF}I(t = 1.30\,\mu\text{m})$	$42 \cdot E_{GF}I_{GF} =$ $0.92 \cdot E_{LF}I(t = 2.04\,\mu\text{m})$
3	$EI\left\{27 + 48\left(\frac{g}{t}\right) + 24\left(\frac{g}{t}\right)^2 + \alpha\gamma\left[6\left(\frac{g}{t}\right) + 12\left(\frac{g}{t}\right)^2 + 8\left(\frac{g}{t}\right)^3\right]\right\}$	$125 \cdot E_{LF}I_{LF} =$ $0.75 \cdot E_{LF}I(t = 2.20\,\mu\text{m})$	$163 \cdot E_{GF}I_{GF} =$ $0.70 \cdot E_{LF}I(t = 3.51\,\mu\text{m})$
4	$EI\left\{64 + 120\left(\frac{g}{t}\right) + 60\left(\frac{g}{t}\right)^2 + \alpha\gamma\left[24\left(\frac{g}{t}\right) + 48\left(\frac{g}{t}\right)^2 + 27\left(\frac{g}{t}\right)^3\right]\right\}$	$308 \cdot E_{LF}I_{LF} =$ $0.66 \cdot E_{LF}I(t = 3.10\,\mu\text{m})$	$403 \cdot E_{GF}I_{GF} =$ $0.60 \cdot E_{LF}I(t = 4.98\,\mu\text{m})$

Table II: BENDING STIFFNESS (EI) AS A FUNCTION OF NUMBER OF LAYERS STACKED.

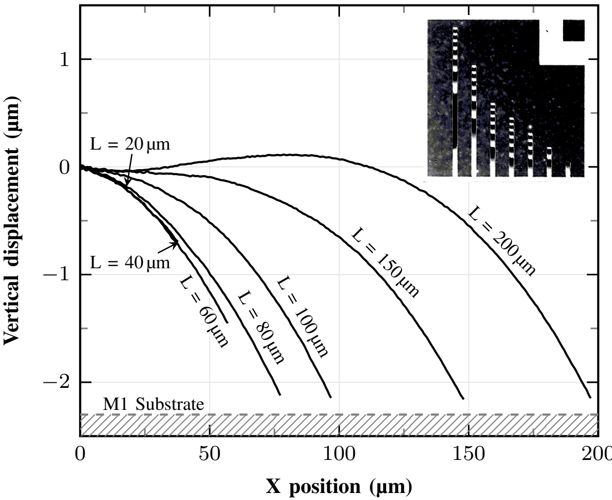


Figure 5: Profiles of the 7 cantilevers from a m45 test structure curved downwards (negative curvature). The longest ones are touching the M1 substrate, represented with a dashed region. Note that the profile near the tip is not measured to avoid border effects. Taken from Quarter of Wafer 2, Lot1, Run 2, LFoundry.

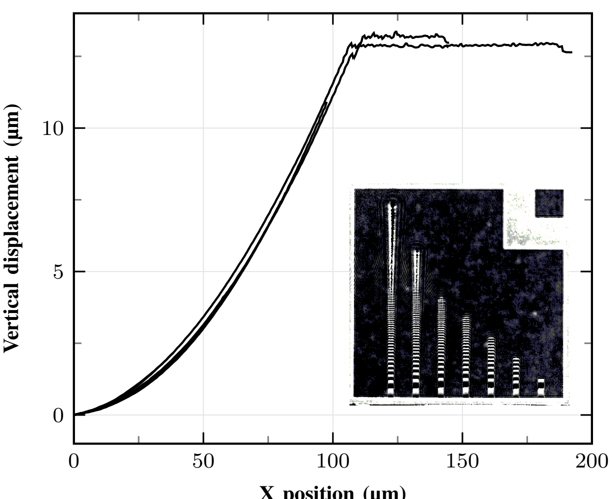


Figure 6: Profiles of the 7 cantilevers from a m4 test structure. The longest cantilevers surpass the maximum allowable slope at an approximate distance of 110 µm from the anchoring point. Hologram of the plotted profiles is at the bottom right corner.

where

$$\theta_m = \arcsin\left(\frac{y'_m}{\sqrt{1+(y'_m)^2}}\right)\Bigg|_{y'_m=0.2} \approx 0.2 \qquad (12)$$

$$\theta_i = \arcsin\left(\frac{y'_i}{\sqrt{1+(y'_i)^2}}\right)\Bigg|_{y'_i=0.1} \approx 0.1 \qquad (13)$$

and where y'_i is the slope of the cantilever at the anchoring point. In our case, initial slopes smaller than 0.1 conform the vast majority of the analyzed test cantilevers. Values derived from equation 11 for each of the cantilever lengths used in this article are shown in table III.

Cantilever length (µm)	Curvature limit (mm^{-1})	Curvature error (1/mm)
200	0.51	0.0021
150	0.69	0.0038
100	1.05	0.0089
80	1.33	0.0142
60	1.82	0.0264
40	2.86	0.0653
20	6.67	0.3556

Table III: MEASUREMENT LIMITATIONS IMPOSED BY THE LENGTH OF THE TEST CANTILEVERS.

3) Condition 3: Accuracy. Small curvatures cannot be measured accurately with short cantilevers as they remain very flat and vertical deformations due to the curvature are smaller or comparable to several error sources (surface roughness, imperfections and small residues, measurement noise, misfocusing, etc). In order to quantify the measurement error, several known curvature levels were measured with cantilevers of different lengths. For each cantilever, the measurement was repeated several times, yielding slightly different values in each observation: mean curvature (K_{mean}) and standard deviation (K_{dev}) values were obtained. Measured variability increased substantially for shorter test cantilevers. Also, K_{mean} did not match perfectly the curvature obtained with larger cantilevers. This was modeled in Matlab with 3 points

that represented the initial, central and final part of a given cantilever. A certain vertical noise (z_{noise}) was applied to the z coordinate of each point and curvature was calculated based on the new position of the 3 points. The difference between the real and measured curvature is the measurement error. By repeating this simulation many times for each cantilever, and for many different curvatures, we obtained the measurement error as a function of cantilever length and curvature. Each level of noise yields a different plot. However, the simulated errors followed a similar trend which allowed us to derive approximate semi-empirical equations 14 and 15 that relate the cantilever length with the error in curvature estimation. We found that a vertical noise of $\pm 10\,\mathrm{nm}$ matched well the observed errors, and, in fact, it matched roughly the variability measured in the cantilever profiles.

$$\text{Absolute curvature error } (\mathrm{mm}^{-1}) \approx \frac{\lambda}{L^2} \tag{14}$$

where λ is a coefficient determined experimentally that accounts for all the measurement error sources. In our case, $\lambda \approx 8 \times 10^{-11}$ matched well the worst-case observations.

$$\text{Relative curvature error } (\%) \approx 100 \times \frac{\lambda}{KL^2} \tag{15}$$

Remarkably, for a given λ the absolute error (equation 14) does not depend on the curvature value being measured, but only on the length of the test cantilever, yielding a very simple formula, applicable for all cantilever curvature measurement techniques in general. The intuitive explanation for this simple relationship is that the shape of the cantilever follows a circumference, and the z displacement depends quadratically with the distance to the anchor (see equation 7). Therefore, an error in the measurement of the z position of cantilever tip will be less important the further it is from the anchor. The predicted curvature error derived from equation 14 is shown in table III for each cantilever length used in this work, assuming initial slopes equal to 0.1 and being the measured length 5 µm smaller than the total length of the cantilever. Given that more accurate measurements can be achieved with longer cantilevers, these were the preferred option for the characterization tests presented in section V, whenever the other limitations would allow it.

Note that the measured curvature variability (σ_K) that appears on all tables and plots is composed of two components, namely, the real variability (σ_K^{real}) plus the measurement error (σ_K^{meas}), which is larger for shorter cantilevers (see table III). The two components are uncorrelated sources of dispersion so they satisfy, according to the Bienaymé formula:

$$\sigma_K^2 = \left(\sigma_K^{real}\right)^2 + \left(\sigma_K^{meas}\right)^2 \tag{16}$$

V. Results

A. Introduction

The curvature of the released test cantilevers from both CMOS processes was analyzed. The measured parameter was curvature rather than radius of curvature given that, contrary to curvature values, which tend to be normally distributed (see bottom of figure 7) and are linearly dependent on the stress value (see equations 2 and 4), radius of curvature distributions do not provide an intuitive description of the physical system. For example, cantilevers from figure 7 have either large positive or negative curvature radius, which apparently yields non-representative variability results. On the other hand, all the associated curvature values are grouped around the mean.

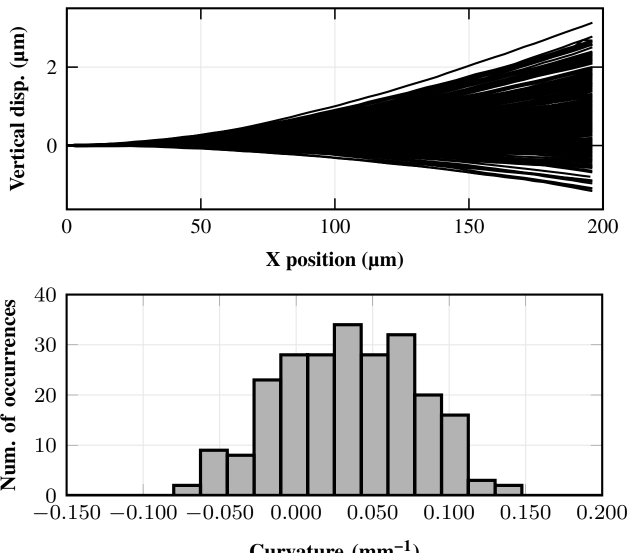


Figure 7: (Top) Profiles of all the 238 M345 200 µm cantilevers from Wafer 1, Lot 2, Run 3, LFoundry. (Bottom) Curvature distribution. Results from table V and the associated wafer map in figure 11b show that the measured curvature was $0.034 \pm 0.044\,\mathrm{mm}^{-1}$. A gaussian distribution describes well the data. In this case, the average curvature is positive but there are cantilevers curved upwards and downwards in the same wafer. The slope at the anchoring point was 0.001 ± 0.001, close to zero.

Results are presented in tables IV and V for GF and LF, respectively. For each CMOS process, 8” wafers from different lots from the same run and from different runs were analyzed. The wide range of measurements performed can give the CMOS-MEMS designer an idea of the expected with-in-wafer (WIW), wafer-to-wafer (W2W), lot-to-lot (L2L), run-to-run (R2R) and CMOS process-to-process (P2P) variations.

For each set of measurements several parameters are specified, namely, the stack or metal layer characterized, mean curvature and variability across the sample, number and length of cantilevers measured, and other relevant information such as size of the sample (full wafer, quarter or small piece), run and lot number and other processing conditions. All wafers etched with Primaxx were baked after release except when indicated otherwise. Also, no backgrinding was applied except when indicated otherwise.

Note that the variability is the measured variability, which includes the measurement uncertainty (see equation 16). This uncertainty is usually not important compared to real variability except for the 20 µm-long cantilevers. It is important to note that the measured variability of small pieces or quarters of wafers is generally smaller than for full wafers, so care must be taken to extract conclusions from different sized samples.

		M2	M23	M234	M2345	M23456	M3	M34	M345	M3456	M4	M45	M456	M5	M56	M6
WAFER 1 - no hot plate	Length (µm)		20	80	100	150		20	100	150		20	150		40	
LOT 2	#Cantilevers		52	52	44	34		52	49	52		52	52		51	
GF - RUN 1	**Average (1/mm)**	**K**	**2.997**	**0.613**	**0.333**	**0.181**	**K**	**1.339**	**0.267**	**0.013**	**K**	**1.919**	**0.212**	**K**	**0.880**	**K**
MEMSSTAR 28 min	**Dev (1/mm)**		**1.039**	**0.277**	**0.207**	**0.101**		**0.552**	**0.136**	**0.137**		**0.719**	**0.201**		**0.598**	
WAFER 1 - after hot plate 30 s	Length (µm)		20	80	100	150		20	100	150		20	150		40	
LOT 2	#Cantilevers		52	52	43	38		51	49	51		50	52		52	
GF - RUN 1	**Average (1/mm)**	**K**	**2.581**	**0.613**	**0.303**	**0.138**	**K**	**1.390**	**0.267**	**0.062**	**K**	**1.967**	**0.212**	**K**	**0.848**	**K**
MEMSSTAR 28 min	**Dev (1/mm)**		**1.017**	**0.277**	**0.173**	**0.109**		**0.501**	**0.136**	**0.183**		**0.623**	**0.201**		**0.600**	
WAFER 1	Length (µm)	20	150	200	200	200	20	200	200	200	20	150	200	20	100	20
LOT 1	#Cantilevers	40	50	48	49	50	49	50	50	50	49	50	51	50	50	51
GF - RUN 3	**Average (1/mm)**	**7.864**	**0.999**	**0.313**	**0.096**	**0.132**	**6.049**	**0.575**	**0.129**	**0.182**	**6.625**	**0.595**	**0.392**	**8.050**	**1.277**	**8.093**
PRIMAXX 36 min	**Dev (1/mm)**	**1.479**	**0.118**	**0.054**	**0.032**	**0.025**	**0.622**	**0.088**	**0.040**	**0.052**	**0.728**	**0.099**	**0.103**	**0.746**	**0.164**	**1.564**
WAFER 2	Length (µm)	20	150	200	200	200	20	150	200	200	20	150	200	20	150	20
LOT 1	#Cantilevers	52	52	49	50	50	52	52	47	50	52	52	47	52	50	52
GF - RUN 3	**Average (1/mm)**	**6.916**	**0.656**	**0.246**	**0.101**	**0.104**	**5.392**	**0.649**	**0.189**	**0.154**	**4.955**	**0.568**	**0.261**	**6.733**	**0.878**	**6.384**
PRIMAXX 40 min	**Dev (1/mm)**	**0.926**	**0.076**	**0.033**	**0.021**	**0.024**	**0.425**	**0.079**	**0.040**	**0.042**	**0.427**	**0.071**	**0.096**	**0.866**	**0.156**	**0.876**
QUARTER OF WAFER 4	Length (µm)	20	150	200	200	200	20	150	200	200	20	150	200	20	150	20
LOT 1	#Cantilevers	12	11	11	12	11	12	12	12	10	12	12	12	12	11	12
GF - RUN 3	**Average (1/mm)**	**8.291**	**1.005**	**0.289**	**0.145**	**0.138**	**7.272**	**0.656**	**0.227**	**0.209**	**7.621**	**0.731**	**0.330**	**8.779**	**1.107**	**7.329**
PRIMAXX 55 min	**Dev (1/mm)**	**0.337**	**0.092**	**0.046**	**0.028**	**0.025**	**0.591**	**0.082**	**0.051**	**0.075**	**0.766**	**0.049**	**0.129**	**0.966**	**0.170**	**1.415**
QUARTER OF WAFER 4	Length (µm)	20	150	200	200	200	20	150	200	200	20	150	200	20	150	20
LOT 1	#Cantilevers	5	4	4	5	5	5	4	4	5	4	4	4	4	4	5
GF - RUN 3	**Average (1/mm)**	**7.816**	**0.745**	**0.227**	**0.109**	**0.117**	**4.612**	**0.468**	**0.160**	**0.177**	**3.965**	**0.526**	**0.223**	**6.306**	**0.859**	**5.735**
PRIMAXX 36 min	**Dev (1/mm)**	**0.262**	**0.041**	**0.027**	**0.013**	**0.018**	**0.114**	**0.058**	**0.015**	**0.033**	**0.260**	**0.040**	**0.053**	**0.198**	**0.096**	**0.972**

K = The profile of cantilevers could not be measured due to excessive initial slope at the anchor. The first run from GF (RUN 1) was experimental and several factors may have affected the measured curvature, so those particular results must be taken with caution.

Table IV: CURVATURE MEASUREMENT RESULTS FROM WAFERS FROM A CMOS 0.18 µm PROCESS FROM GLOBAL FOUNDRIES.

B. Circularity

The circularity of each of the 200 µm-long cantilever profiles shown in figure 7 was measured. The mean of the 238 circularity values obtained was 71 nm with a standard deviation of ± 35 nm. Surface roughness and/or measurement noise accounted for $30 - 40\%$ of the measured circularity given that circularity values around 20-30 nm were typically measured over flat metal surfaces. The cantilever profile deviations from a circular shape (71 nm) are small ($\sim 10\%$) compared to the tip displacement caused by the measured curvature (0.034 mm^{-1}), which, according to equation 7, is 680 nm. This is a near worst case example. The same assessment was performed in all wafers, yielding circularity values between 1% and 10% (except in some cases where K was accidentally close to zero), showing that the cantilevers follow a very circular profile.

C. Curvature of Stacks and Single Metals

The Al-based BEOL metallization is typically sandwiched between two double thin layers of titanium (Ti) and titanium nitride (TiN). The larger coefficient of thermal expansion coefficient (CTE) of aluminum ($23.1 \times 10^{-6}\,°C^{-1}$), compared to those of Ti ($8.6 \times 10^{-6}\,°C^{-1}$) and TiN ($9.35 \times 10^{-6}\,°C^{-1}$), generally leads to tensile stresses for aluminum (Al) and compressive stresses for Ti and TiN as a result of cooling down from higher processing temperature [25]. The final residual stresses create a bending moment that curls the cantilever upwards or downwards.

However, there are additional physical phenomena that affect cantilever curvature after release. For example, LFoundry single metals and their corresponding sub-layers have the same nominal thickness for all metal levels and corresponding sub-layers, and no differences were measured in SEM images. However, the mean curvature of the metal levels is more negative the higher the metal level (see figure 8). This indicates that other factors apart from thickness are important in terms of curvature after release. These probably include residual stress variations dependent on temperature history of each metal level (see [26] and section V-K). As a matter of fact, lower metals like M2 go through more temperature cycles than higher ones like M5. This is a notable difference between LF and GF, as the curvature of GF single metals was independent of the metal level, large and positive.

Measured curvature of cantilevers from several LF and GF runs (one of them being a full CMOS-process that included the FEOL) is displayed in figure 8. The mean curvature of single metals (a few mm^{-1}) and their WIW variations (generally between 0.5 and 1.0 mm^{-1}) were generally very large compared to other MEMS processes [27]. In addition, their W2W, L2L and R2R variations were also in the same order of magnitude, around 1 mm^{-1}, roughly. Unfortunately, this imposes serious restrictions to design competitive MEMS with single metals. As a result of single metals curvature (positive for GF and generally negative for LF), the vast majority of stacks from all the runs from GF showed an average positive curvature, while negative curvatures were more predominant in the case of LF, as the first right hand side (RHS) term of equation 8 predicts. For stacks of metal layers results consistently showed that not only the mean curvature but also, and more importantly, their WIW, L2L, R2R and P2P variations were significantly reduced with respect to single metal layers. For example, for the full process wafer from LF, both average curvature and WIW variations of M2345 ($-0.091 \pm 0.040\,\mathrm{mm}^{-1}$) were reduced around 20 times with respect to M2 ($-1.903 \pm 0.766\,\mathrm{mm}^{-1}$), and mean curvature was reduced around 64 times when compared to M5 ($-5.865 \pm 0.829\,\mathrm{mm}^{-1}$). This improvement is greatly correlated with the number of stacked layers, which is explained by equation 8, as the denominators are the increased bending stiffness of the stacks, presented in table II. Curvature reduction varied from case to case, achieving more than 2 orders of reduction in some cases (see M2345 and M5 from wafer 2, lot 1, run 4, LF) and around 1 order of magnitude in others (see M2345 and M3 from wafer 1, lot 3, run 3, LF). With-in-wafer variability reductions for 4-

		M2	M23	M234	M2345	M23456	M3	M34	M345	M3456	M4	M45	M456	M5	M56	M6
HALF OF WAFER 2	Length (µm)	20	60	200	200		20	80	80	100	20	60		20	60	60
LOT 1	#Cantilevers	47	51	50	50		51	50	51	52	52	52		52	52	52
LF - RUN 1	**Average (1/mm)**	**0.700**	**0.111**	**0.105**	**0.023**	**NA**	**-0.516**	**-0.159**	**-0.257**	**1.223**	**-1.687**	**-0.877**	**NA**	**-3.828**	**2.420**	**3.054**
PRIMAXX	**Dev (1/mm)**	**1.827**	**0.245**	**0.103**	**0.065**		**2.148**	**0.258**	**0.107**	**0.164**	**1.964**	**0.235**		**1.926**	**0.372**	**0.457**
QUARTER OF WAFER 1	Length (µm)						20	100	80	200	20	80	200	20-40	200	100
LOT 1	#Cantilevers						62	60	58	62	62	61	61	59	60	61
LF - RUN 2	**Average (1/mm)**	**NR**	**NR**	**NR**	**NR**	**NR**	**-1.281**	**0.008**	**-0.183**	**0.376**	**-2.397**	**-0.629**	**0.512**	**-5.934**	**0.725**	**-0.175**
PRIMAXX 25 min	**Dev (1/mm)**						**1.094**	**0.050**	**0.090**	**0.094**	**0.660**	**0.148**	**0.104**	**1.551**	**0.110**	**0.082**
QUARTER OF WAFER 2	Length (µm)	20	40	100	60	150	20	80	40	150	20	60	150	20	200	100
LOT 1	#Cantilevers	52	52	51	45	51	52	44	49	40	51	45	49	52	51	52
LF - RUN 2	**Average (1/mm)**	**-1.864**	**-0.338**	**-0.030**	**-0.144**	**0.241**	**-3.463**	**-0.129**	**-0.293**	**0.311**	**-3.933**	**-0.886**	**0.430**	**-7.860**	**0.678**	**-0.335**
PRIMAXX 35 min	**Dev (1/mm)**	0.418	0.085	0.050	0.055	0.057	0.581	0.097	0.138	0.101	0.685	0.180	0.136	0.910	0.113	0.135
QUARTER OF WAFER 1	Length (µm)			200	200	150	20	200	200	150	20	100	100	20	100	60
LOT 1	#Cantilevers			87	85	89	87	81	88	88	84	81	87	87	89	88
LF - RUN 3	**Average (1/mm)**	**NR**	**NR**	**0.079**	**0.167**	**0.673**	**-1.581**	**0.105**	**0.184**	**0.849**	**-3.366**	**-0.186**	**1.040**	**-4.325**	**1.400**	**2.986**
PRIMAXX 25 min	**Dev (1/mm)**			**0.061**	**0.040**	**0.075**	**0.573**	**0.079**	**0.038**	**0.079**	**0.701**	**0.100**	**0.165**	**0.736**	**0.270**	**0.353**
QUARTER OF WAFER 2	Length (µm)	20	60	200	200	200	20	80	150	200	40	80	150	40	100	60
LOT 1	#Cantilevers	83	86	85	85	84	86	83	86	85	86	86	86	85	86	86
LF - RUN 3	**Average (1/mm)**	**-1.765**	**0.012**	**0.033**	**0.072**	**0.554**	**-2.758**	**-0.229**	**-0.046**	**0.689**	**-2.733**	**-0.410**	**0.898**	**-3.803**	**1.329**	**2.885**
PRIMAXX 35 min	**Dev (1/mm)**	**0.540**	**0.065**	**0.025**	**0.015**	**0.060**	**0.532**	**0.078**	**0.031**	**0.081**	**0.180**	**0.078**	**0.155**	**0.282**	**0.222**	**0.266**
WAFER 1	Length (µm)	20	100	200	200	200	20	100	200	200	20	100	150	20	150	200
LOT 2	#Cantilevers	235	237	232	236	239	234	238	233	238	235	232	238	236	238	238
LF - RUN 3	**Average (1/mm)**	**0.477**	**0.289**	**0.106**	**0.111**	**0.416**	**-0.885**	**-0.002**	**0.034**	**0.472**	**-2.612**	**-0.176**	**0.566**	**-4.288**	**0.555**	**0.235**
PRIMAXX 30 min	**Dev (1/mm)**	**0.749**	**0.135**	**0.054**	**0.031**	**0.077**	**0.685**	**0.159**	**0.044**	**0.088**	**0.938**	**0.145**	**0.140**	**0.869**	**0.213**	**0.071**
WAFER 1	Length (µm)	80	40	40	60	150	20	60	60	150	20	60	100	20	80	60
LOT 3	#Cantilevers	113	114	122	115	119	119	119	119	119	119	115	119	119	119	119
LF - RUN 3	**Average (1/mm)**	**1.913**	**-0.280**	**-0.284**	**-0.225**	**0.707**	**-1.631**	**-0.402**	**-0.285**	**0.955**	**-2.404**	**-0.968**	**1.306**	**-4.678**	**2.083**	**2.891**
PRIMAXX 32 min	**Dev (1/mm)**	**0.858**	**0.218**	**0.145**	**0.081**	**0.121**	**0.928**	**0.205**	**0.110**	**0.160**	**1.071**	**0.199**	**0.222**	**1.177**	**0.355**	**0.322**
WAFER 2	Length (µm)	20	40	80	100	150	20	60	100	150	20	60	100	20	80	60
LOT 1	#Cantilevers	241	240	241	241	226	240	241	241	230	241	240	232	240	232	232
LF - RUN 4	**Average (1/mm)**	**-0.134**	**-0.120**	**-0.008**	**-0.040**	**0.608**	**-2.461**	**-0.133**	**-0.141**	**0.829**	**-3.663**	**-0.738**	**1.188**	**-5.080**	**1.820**	**3.226**
PRIMAXX 32 min	**Dev (1/mm)**	0.873	0.132	0.045	0.028	0.076	0.860	0.099	0.049	0.102	0.995	0.121	0.177	1.099	0.299	0.314
WAFER 3 (Backgrinded to 500 µm)	Length (µm)	40	60	80	80	100	20	100	100	100	20	100	100	20	100	60
LOT 1	#Cantilevers	233	233	227	228	220	206	232	227	232	239	230	226	233	229	231
LF - RUN 4	**Average (1/mm)**	**0.490**	**-0.084**	**-0.044**	**0.042**	**0.632**	**-1.441**	**-0.174**	**0.021**	**0.866**	**-3.048**	**-0.370**	**1.202**	**-4.147**	**1.763**	**2.874**
PRIMAXX 32 min	**Dev (1/mm)**	**0.687**	**0.115**	**0.047**	**0.039**	**0.085**	**0.842**	**0.069**	**0.057**	**0.123**	**1.068**	**0.117**	**0.179**	**1.102**	**0.256**	**0.363**
WAFER 1 (Backgrinded to 500 µm)	Length (µm)	20	20	40	80	200	20	40	80	200	20	60	150	20	200	100
LOT 1	#Cantilevers	243	238	240	236	242	243	244	243	244	244	244	244	244	242	243
LF - RUN 5 (FULL PROCESS)	**Average (1/mm)**	**-1.903**	**-0.569**	**-0.296**	**-0.091**	**0.428**	**-3.030**	**-0.771**	**-0.235**	**0.480**	**-4.536**	**-0.868**	**0.521**	**-5.865**	**0.437**	**-0.384**
PRIMAXX 30 min	**Dev (1/mm)**	**0.766**	**0.218**	**0.160**	**0.040**	**0.104**	**0.645**	**0.310**	**0.083**	**0.130**	**1.242**	**0.136**	**0.173**	**0.829**	**0.114**	**0.089**

NR = Not released. NA = Not available.

Table V: CURVATURE MEASUREMENT RESULTS FROM WAFERS FROM A CMOS 0.18 µm PROCESS FROM L-FOUNDRY.

metals with respect to single metals typically ranged from 20 to 40 times. Measured stack curvatures cannot be accurately predicted exclusively by the first RHS term of equation 8, which only takes into account the curvature of single metals and the increased bending stiffness. This indicates that the average stress mismatch between layers plays an important role in the observed curvatures, according to equation 8, if the used W vias do not affect stack curvature.

Theoretically, when the W vias effect is negligible ($M_{Wi} \rightarrow 0$), as for the standard W vias arrays used in this work, the average stress mismatch between single metal layers may be calculated by solving for the stress (σ_i) in equation 8. For example, the stress mismatch between M3 and M2 ($\sigma_3 - \sigma_2$) can be derived from the M2, M3 and M23 curvatures:

$$\sigma_3 - \sigma_2 = \left(K^{23}_{stack} \frac{EI_{stack}}{EI} - K_2 - K_3 \right) \frac{Et^2}{6(t+g)} \qquad (17)$$

Once the stress mismatch value is known, the associated strain mismatch value, which does not depend on the assumed Young's Modulus (E), can be calculated by dividing by E. Results yielded strain mismatch values between adjacent layers lower than 700 ppm for both GF and LF processes. However, under sufficiently high stress/strain mismatch, the applicability of linear equations 8 and 17 is limited by non-linear effects such us localized plastic deformation or partial delamination near the anchor of the W vias. Plastic deformation is more plausible given that no delamination has been observed in SEM images. Either of these mechanisms allow greater expansion/contraction mismatch between the layers, which is absorbed by shear deformation of the stack, relieving part of the stress mismatch that, otherwise, would have led to larger curvature. As a consequence, equation 17 is expected to underestimate stress/strain mismatch. A similar equation can be derived for 3-metal stacks. In that case, numerical simulations show that the Von Mises stress levels near the W via anchor are even larger when more layers are stacked. This is reasonable given that, when more layers are stacked, the curvature is smaller, so the stress mismatch is relieved to a lesser extent. In fact, curvature values from tables IV and V confirm that 3-metal cantilevers curve less than expected if stress/strain mismatches derived from 2-metal cantilevers are assumed, which can be explained by either of the two aforementioned non-linear mechanisms.

D. Variability

For each metal there was 1 test structure per reticle, so within-reticle variations are not included in this work. Curvature varies smoothly across the wafers as can be observed in the wafer maps of figures 10 and 11 for LF process. Matching of curl of adjacent test cantilevers of different lengths from the

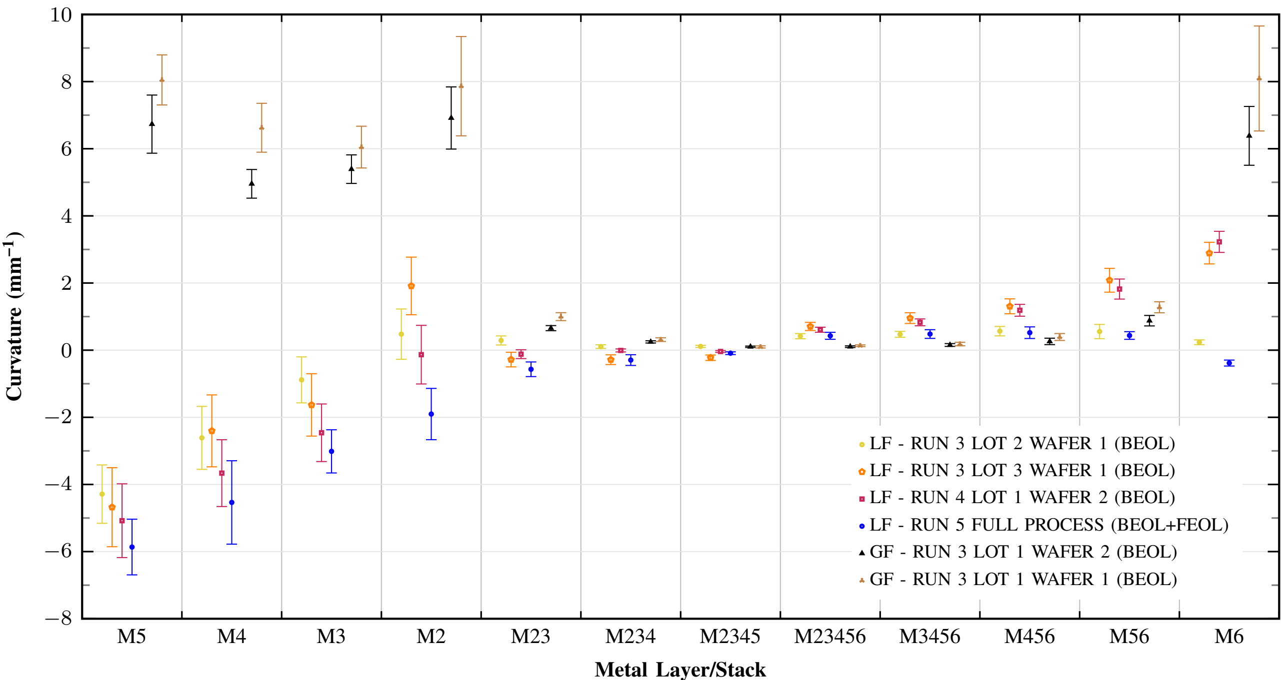


Figure 8: Average curvature and variability of some metal stacks used in 6 different wafers. Stacking of identical metal layers led to a reduced variability and average curvature, which is the typical behavior observed in all the runs analyzed in this work. Stacking of dissimilar metal layers (M6 and others) may not be as efficient (compare M2345 with M23456).

same test array was good (see figures 2b and 6), generally not much larger than the measurement error of table III. This is in agreement with the results reported in [9].

The thickness of the Al-based central layer and the bottom and top thin Ti/TiN layers was measured with SEM. The measured thicknesses are in table I. Thickness variations of the Ti and/or TiN layers lead to curvature variations after cool down from the deposition or other processes temperature due to CTE mismatch with aluminum. Unfortunately, accurate assessments are not possible given that, the relative proportion of Ti and TiN could not be determined and complex phenomena, like plastic deformations [26, 28] and creep (see section V-K), or material properties dependence with thickness [29] may be taking place. However, in order to approximately understand the importance of Ti/TiN thickness variations on single metal curvature due to CTE mismatch after cool down, the following 2 cases were considered: one in which the Ti layer (E=116 GPa) is 15 nm thick, and the rest of the Ti/TiN layer is pure TiN (E=476 GPa [30]); and another identical to the previous one but with a 10% thickness reduction of the top TiN layer. Then, finite-element-analysis (FEA) was employed to assess the effect of a 250 °C cool down, which is not uncommon in CMOS BEOL process steps, which can even go up to 450 °C [31]. FEA yielded a curvature difference between the 2 cases of 0.37 mm^{-1} for LF single metals, and of 0.27 mm^{-1} for GF single metals. The obtained results are approximately linear with thickness variations and temperature cool down: for example, 1 % thickness variations cause a similar mismatch effect to 25 °C variations. These results suggest that thickness variations of the Ti/TiN layers can be playing an important role in the observed single metals curvature variability, which is around 1 mm^{-1} in order of magnitude.

Contrary to single metals, stack curvature also depends on the gap between metals as described by equation 8, where the gap variability changes the value of the bending stiffness (IE_{stack}). This effect is important as, for example, equation 8 predicts a 2-metal stack curvature variability of 13% for a gap variability of 10% and a metal thickness variability of 5%, which is not a bad scenario in conventional metal interconnect. Note that this is just taking into account bending stiffness variations. If single metal curvature variability and measurement errors are included, measured variability exceeds the predicted value in many cases. This probably indicates that stress mismatch variability and plastic deformations should also be considered. On the other hand, no evidence of curvature variability due to the vHF etch was found given that etch time differences as large as 21 minutes did not affect curvature noticeably (see section V-F) and vHF etch WIW variations are around ±1 min [17]. So, while thickness and temperature history can be important for the mean curvature and variability of single metals, gap uniformity and stress mismatch are also important for the curvature of stacks.

Curvature patterns of single metals tend to be transfered to the stacks in LF wafers (see figures 10 and 11), highlighting the importance of the first RHS term of equation 8. Single-metal curvature typically follows a radial-like distribution. Despite stacks of metals also show radial distributions frequently, others like annular and cross-wafer are also observed, generally superimposed to a radial-like background distribution.

Chemical-mechanical-polishing (CMP) is a significant source of IMD oxide thickness/gap variability. It can induce

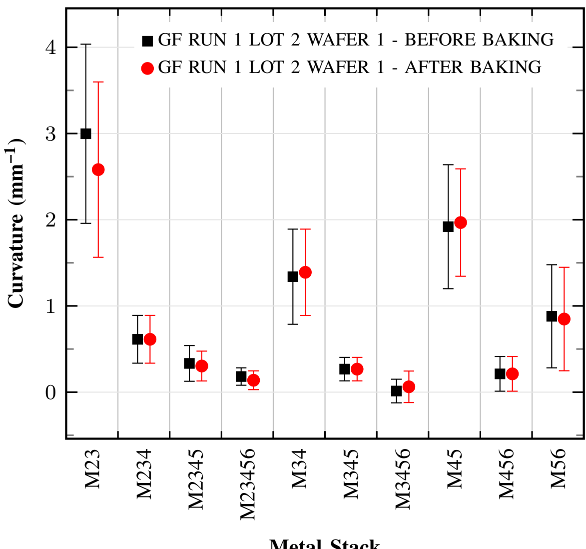


Figure 9: Comparison of the curvature before and after a baking step that consisted on 200 °C during 30 seconds.

complex patterns of radial thickness variation as the observed annular patterns for curvature of stacks. Many MEMS comprise large metal structures that need to break maximum metal size rules of standard CMOS design. This can accentuate the CMP adverse effects as high density metal areas may be overpolished and end up thinner, so dummy metal filling is used to reduce thickness dependence on layout pattern. Also, temperature gradients in radial or cross-wafer directions may be present in process chambers, and spinning of wafers in lithography, and wafer cleaning steps may introduce radial variations [32]. In any case, determination of the exact source of curvature variability would require specifically designed experiments.

E. Baking Step Effects

An important question is if the baking step of the CMOS-MEMS process modifies the curvature of the BEOL metal layers. For this purpose, the curvature characterization was performed on a randomly selected wafer before and after the baking step, which in this case consisted on putting the wafer on a hot plate at approximately 200 °C-250 °C for 30 seconds, which was enough to remove the residues. Characterization results (see figure 9) showed that the curvature did not significantly change. As we shall see, this will be in accordance to the results of section V-K regarding temperature effects on curvature. Some variation is observed for M23 composites, but this is attributed to the reduced accuracy of the 20 µm-long cantilevers used for the characterization in this case.

F. Curvature versus Time

Limited measurements were performed in this respect, but significant curvature changes were not observed with time. Also, in the case of GF wafer 1 from lot 2, run 1, the full wafer was measured before and after the baking step: 4.5 weeks passed between measurements. They were stored at 45% relative humidity. No significant changes were observed. Silicon oxide stress can change significantly due to moisture absorption [33, 34], potentially leading to curvature variations of oxide structures with time. However, the cantilevers of this work do not leave any oxide exposed to ambient air.

G. BEOL versus FEOL+BEOL

Processing wafers with only the BEOL is significantly cheaper than processing full-CMOS wafers, so determining if BEOL wafers are sufficient to replicate the behavior of full-CMOS wafers is very important. For this purpose, both full-CMOS and BEOL wafers were measured. In figure 8 and table V no noticeable differences can be observed between the full-CMOS run and BEOL runs. This result agrees with the fact that the BEOL is processed after the FEOL, so the latter should not affect the former.

Only M6 curvature changed from a typically large positive curvature in BEOL runs to a small negative one, as happened for BEOL run 2 and lot2 from run 3, of LFoundry (see table IV and figure 8). In both cases, some passivation oxide over M6 was remaining after the pad opening step, leaving the Ti/TiN layer and aluminum of M6 intact, contrary to what happened in those cases that showed large M6 curvature. The thickness of the Ti/TiN and Al layers of M6 was measured with FIB cuts, resulting in 40±15 nm and 820±15 nm, respectively. Numerical simulations showed that a composite beam made of a 40 nm layer of TiN below a 820 nm thick layer of Al, and no TiN on top of the Al, curves upwards 3.0 mm^{-1} when cooled down 200 °C from an initially free-stress state, simulating grossly the cool down after a generic deposition process. If the TiN layer were substituted by pure Ti, identical upwards curling would be achieved with a 430 °C cool down. Other combinations of both materials yield similar numbers. Therefore, Ti/TiN etch, and probably some Al etch, are thought to be the source of the M6 curvature differences found.

H. Release Process and Etch Time

The studied wafers were etched with machines from two different vendors, namely, MEMSstar and Primaxx. Gathered data is insufficient to draw an accurate conclusion regarding the curvature dependence on the etching machine and method, but it can be affirmed that no dramatic differences were observed.

Although no specific experiment was set to assess the effect of etching time on curvature, some conclusions can be extracted from several quarters of the same wafers that were etched with the Primaxx machine for different times like the two quarters of wafer 4, lot 1, run 3 from GF: one quarter was etched for 36 min and the other one for 55 min (see table IV). Observed curvature differences between both samples fall within the normal variation between the quarters of a wafer. Also, the bottom surface of the cantilevers from figure 4 were exposed to vHF for different times, in average, depending on the cantilever width. This difference can be estimated by using the vHF etch rate (0.25 µm min^{-1}) reported in [17]. In average, the bottom surface of the 30 µm-wide cantilever was exposed

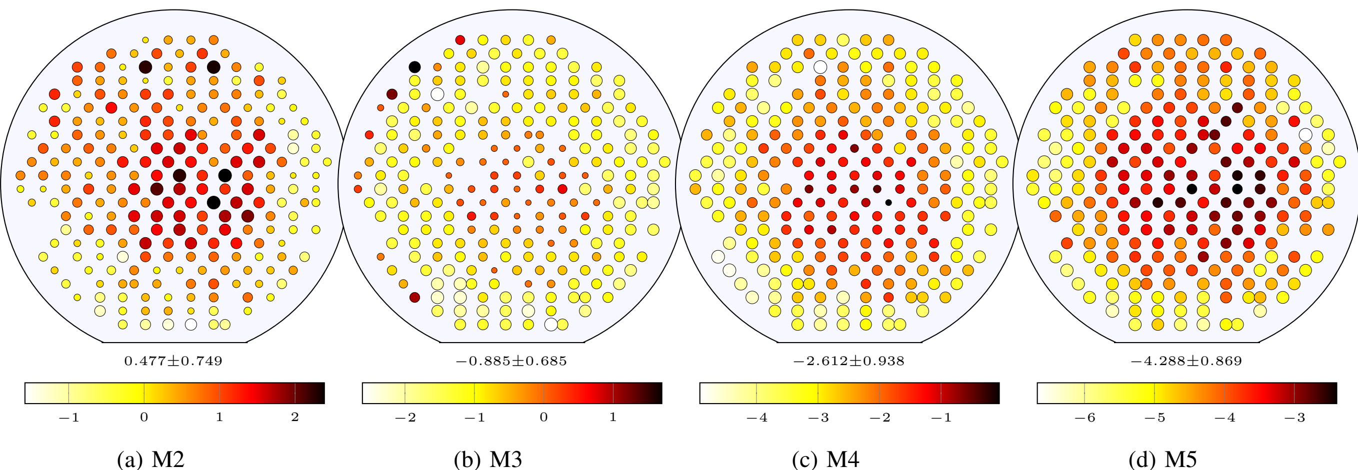


Figure 10: Curvature distribution for some single metals: Wafer 1, Lot 2, Run 3 from LFoundry. Area of markers is proportional to the absolute curvature and was normalized with the maximum absolute curvature value over each wafer.

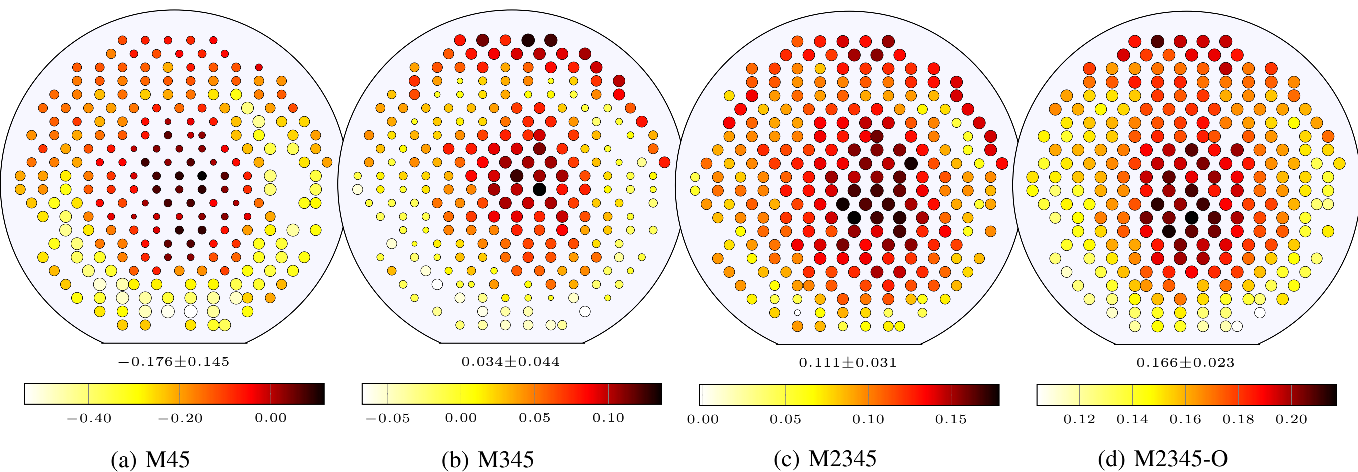


Figure 11: Curvature distribution for some stacks of metals: Wafer 1, Lot 2, Run 3 from LFoundry. Area of markers is proportional to the absolute curvature and was normalized with the value of the maximum absolute curvature over each wafer. Note the scale is different to highlight the differences in wafers with lower variations.

to vHF 25 min longer than the 5 µm-wide cantilever. However, no significant curvature differences are observed in the picture.

Although curvature dependence on etching time cannot be assessed accurately with the extant data, it is by all means significantly less important than other sources of variability. This is in agreement with the vHF high selectivity of silicon oxide to the metals that form the test cantilevers [17, 35–37].

I. Backgrinding

Finally, another important step in wafer processing is the backgrinding, which is useful for reducing the thickness of the wafer prior to subsequently packaging steps. Wafer 3 from lot 1, run 4 from LF was backgrinded to a thickness of 500 µm (see table V) and no noticeable effects were observed when compared to other wafers from the same lot than were not backgrinded.

J. Effect of W Via Desing on Curvature

In order to assess the effect of the W via design on the curvature of stacks of metal, test cantilevers with 4 different via designs were fabricated in M34, M234, M345 and M2345 in two runs. The 4 designs tested and the results obtained are shown in table VI. Via design 1 is the one used in the test cantilevers presented in this work: a standard rectangular array with a via width and via spacing of approximately 0.3 µm. Via design 2 is just a long continuous via that runs along the perimeter of the cantilever, enclosing the IMD oxide between the metal layers. Via design 3 is an array of intersecting perpendicular long continuous vias, which also encloses some IMD oxide between the metal layers. Via design 4 is like design 2, but also with the standard rectangular array of vias.

Results showed a strong correlation between mean curvature and via design. Numerical simulations of the W via design 1 showed that the W vias residual stress does not change the curvature of the stack (third RHS term of equation 8 is zero). The non continuity of the individual vias along the length of the beam is the reason for this effect. This is in agreement with their negligible contribution to EI_{stack} ($\alpha = 0$) as mentioned in section IV-B, and with the measurements shown at the bottom half of table VI, which yielded very similar curvatures for designs 2 and 4 (note that for the M34 stack

		M234	M234	M234	M345	M345	M345	M2345	M2345	M2345
		①	②	③	①	②	③	①	②	③
WAFER 1	Length (µm)	200	200	150	200	200	150	200	200	150
LOT 2	#Cantilevers	232	238	208	233	238	219	236	238	166
LF - RUN 3	**Ave (mm^{-1})**	**0.106**	**0.262**	**1.020**	**0.034**	**0.232**	**0.887**	**0.111**	**0.166**	**0.644**
PRIMAXX 30 min	**Dev (mm^{-1})**	**0.054**	**0.061**	**0.092**	**0.044**	**0.058**	**0.088**	**0.031**	**0.023**	**0.112**
		M34	**M34**	**M34**	**M345**	**M345**	**M345**	**M3456**	**M3456**	**M3456**
		①	②	④	①	②	④	①	②	④
HALF OF WAFER 2	Length (µm)	80	80	60	80	150	100	100	150	100
LOT 1	#Cantilevers	50	51	52	51	48	49	52	52	51
LF - RUN 1	**Ave (mm^{-1})**	**-0.159**	**0.128**	**-0.005**	**-0.257**	**0.119**	**0.119**	**1.223**	**0.804**	**0.879**
PRIMAXX 35 min	**Dev (mm^{-1})**	**0.258**	**0.316**	**0.325**	**0.107**	**0.120**	**0.113**	**0.164**	**0.063**	**0.073**

Table VI: Comparison Table. Effect of Tungsten (W) Vias on Curvature of the Metal Stack.

the variability is large, so assessment is not so accurate as with the 3-metal stacks). Although in design 4 the W vias are joined with IMD oxide, which provides some continuity between the vias, the IMD oxide effect is small, as revealed by the similar bending stiffness (within 10%) and α value of designs 2 and 4. Designs 2, 3 and 4, which run continuously along the cantilever length, do modify the stack curvature. In fact, FEA showed that the curvature change due to residual stress gradients of the W vias (including their corresponding Ti/TiN layers), or due to mismatch between different levels of W vias, is 2.5-3.0 times more pronounced for design 3 than for designs 2 and 4. Measurements confirmed this qualitatively, but showed a greater curvature difference (>4) between designs 3 and 2. Given that no significant thickness variations of the Ti/TiN layers of the single metal layers were observed in SEM images, the discrepancy could be related to localized plastic deformations or partial delaminations near the anchor of the W vias, as curvature data suggested when the residual stress mismatch between single layers was evaluated in section V-C, but it is not possible to confirm this with the extant data.

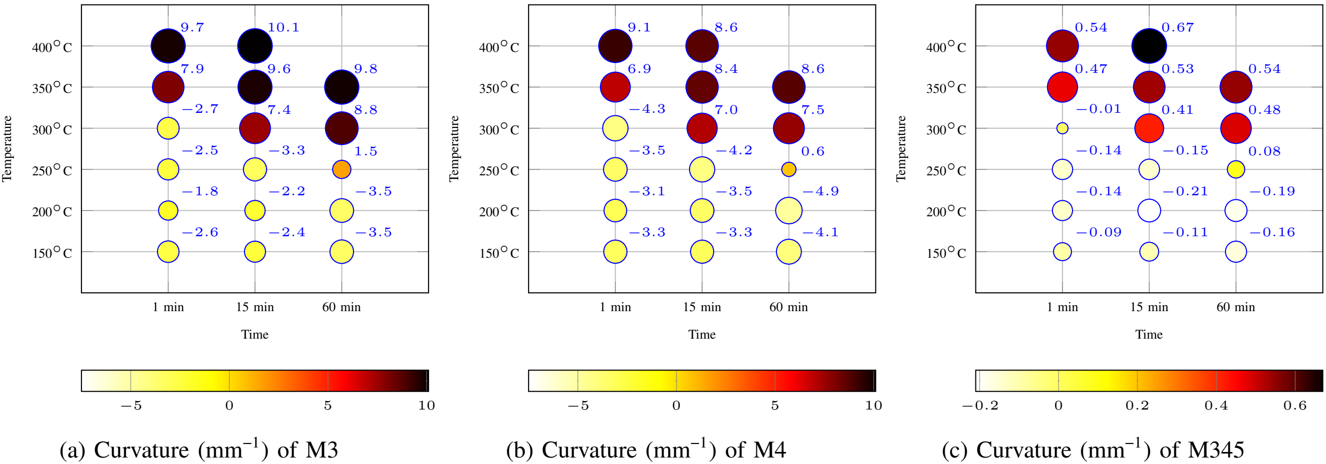
From a design point of view, the most important conclusion is that the curvature of the metal stacks may be tailored up to some degree by the appropriate choice of the W via design used to connect the metal layers. This comes with associated design complexity as the formulas for displacement and resonant frequency of solid cantilevers are no longer applicable. However, in section IV-B we show analytical equations to calculate the bending stiffness of stacked cantilevers with arbitrary W vias design. The coefficient α should be empirically or numerically determined, and it is approximately 0.00, 0.22, 0.44 and 0.25 for W via designs 1, 2, 3 and 4, respectively, according to FEA. The values are the same for LF and GF processes given that the via size and spacings are similar. Once the bending stiffness is known, the resonant frequency or spring constant can be readily calculated as described in [38, 39]. Also, FEA can be simplified using equivalent solid beams with the same bending stiffness as the real stacks (see table II) instead of complex structures.

Finally, high enough via density is required in order to avoid via detachment from the metal layers due to out-of-plane forces. Via detachment has been observed in our preliminary test designs when very low via density was used, but it has not been observed for any of the presented via designs, which were used in several other MEMS structures.

K. Temperature and Time Effects on Curvature

Thermal annealing can modify the curvature of thin-film structures [40, 41]. Also, temperature effects on curvature of released BEOL layers were already identified in [42]. Here, they have been investigated by applying different thermal profiles to 18 samples (3 cm x 3 cm) that resulted from cleaving LF wafer 2 from run 4, lot 1 (see table V). Each thermal profile presented a different maximum temperature (150 °C - 400 °C) and duration (1 min, 15 min or 60 min). The rising ramp was 1 °C s^{-1}, whereas the measured cooling down ramp was 0.3 °C s^{-1}, approximately. The curvature of 4 test cantilevers on each sample was measured after the thermal test, which was carried out in a nitrogen environment. Unfortunately, the sample corresponding to 400 °C and 60 min was damaged during manipulation, so the associated data point is missing. The obtained mean curvature for each sample is plotted in figure 12. Note that the initial curvature of each sample is not exactly the same due to the curvature non-uniformity over the wafer.

Results showed that the qualitative response to temperature of single metals was very similar to those of stacks. For both of them the curvature became more positive the higher the temperature and the larger the time duration. However, the final curvature of the stacks was 10-20 times lower than the curvature of single metals. Also, it seems there is a time-temperature threshold above which the curvature changes quite abruptly: transitions from 250 °C to 350 °C exhibited the larger curvature variations. Also, time effects were most noticeable at 300 °C, where the transition from 1 minute to 15 minutes leads to important curvature variations. At higher temperatures, time effects were much less important and the new more positive



(a) Curvature (mm^{-1}) of M3 (b) Curvature (mm^{-1}) of M4 (c) Curvature (mm^{-1}) of M345

Figure 12: Effect of temperature and time on the curvature of cantilevers after cool down: Wafer 2, Lot 1, Run 4 from LFoundry. Size of data points indicate absolute value of the curvature, whereas color indicates the signed value as described by the scale below the graph.

curvature was more stable with time.

The observed time-temperature threshold cannot be attributed to the W vias of the stacks given that it took place in both single metals (which have no W vias) and stacks. Also, it is difficult to justify that such a large increase in the curvature of the stacks may be caused by sublimation of residues on the surface of the cantilevers. On the other hand, thermal stresses develop with increasing temperature due to the unequal thermal expansion coefficient of the layers that form the cantilevers (Al, Ti and TiN). If the yield stress were surpassed plastic deformation would take place, leaving the cantilevers deformed after cooling down. As a matter of fact, permanent deformation of BEOL CMOS-MEMS cantilevers after being subjected to high temperatures has been attributed [24] to plastic deformation due to aluminum yield strength reduction at high temperatures [26, 43–45]. However, in order to be able to account for the observed time-dependence in our experiments, yield strength time-dependence [45, 46] cannot be neglected as in the mentioned study. In addition, we think that thermal creep mechanisms, highly dependent on stress and temperature levels [47, 48], should also play an important role in the observed permanent deformations, especially for the longer times. In fact, aluminum and its alloys are prone to creep at relative low temperatures given their low melting point (660 °C for pure aluminum and lower for alloys)[46]. Once the cantilevers deform enough to relieve the stress significantly, creep rate should slow down greatly given its very important dependence on stress levels. This could qualitatively explain the more stable, but still time-dependent, new more positive curvatures at 350 °C and 400 °C.

In any case, the presented data can be used for predicting the behavior of BEOL CMOS-MEMS structures after being subjected to high temperatures, like when going through some of the typical packaging steps of MEMS devices, many of which involve important temperature excursions. For example, from these data we could have deduced that the baking step needed after the vHF release [17] should not induce noticeable curvature variations given its maximum temperature (around 200-250 °C) and time duration (around 30 seconds). As a matter of fact, this agrees with the results shown in figure 9 and presented in section V-E.

Data also shows that, theoretically, curvature reduction may be achieved in some cases by applying the right temperature profile to the BEOL structures. For example, 1 min at 300 °C reduced the curvature of M345 from $-0.09\,mm^{-1}$ to $-0.01\,mm^{-1}$ (see figure 12c) or 60 min at 250 °C reduced the M4 curvature from $-4.1\,mm^{-1}$ to $0.6\,mm^{-1}$ (see figure 12b).

VI. Conclusions

Curvature characterization of structural layers is essential for succesful development of MEMS products. Related literature for metal structures of CMOS-MEMS processes is currently very limited. A methodology for measuring cantilever curvature was presented, and its limitations analyzed. In particular, curvature measurement accuracy was discussed and modeled succesfully with an equation applicable for general cantilever curvature measurement techniques. For our setup, $\pm 0.0021\,mm^{-1}$ for 200 µm-long cantilevers was achieved.

Extensive curvature measurement of CMOS-MEMS BEOL released cantilevers was carried out on 0.18 µm wafers from two different CMOS foundries. Test cantilevers composed of several stacked metal layers were included in all the tested runs, and analytical equations that describe their bending behavior as a function of the W via design that join the layers were presented. Remarkably, the W via design most used in this work (standard rectangular arrays of W vias) does not contribute to the bending stiffness of the stack or its curvature. However, important curvature modification of the stacks by employing other W via designs was demonstrated.

Curvature of single metal layers was typically in the order of a few mm^{-1} and its WIW variability between 0.5 and $1.0\,mm^{-1}$. Unfortunately, this imposes serious restrictions to design competitive MEMS that may be circumvented in many cases by stacking several layers. Stacking 4 identical metal layers reduced not only the mean curvature between 1 and 2 orders of magnitude with respect to single metals but also, and more importantly, its variability between 20 and 40 times. The curvature reduction was highly correlated with

the number of stacked layers and was modeled analytically. Curvature reductions varied from case to case, highlighting the importance of stress mismatch between single layers. In addition, gap variations, and consequently CMP uniformity, were shown to be an important factor in stack curvature variability control. WIW variability usually followed a radial distribution although other distributions were also observed for stacks of metals.

Process variations like processing or not the FEOL, back-grinding, the baking step, release machine vendor or release etch duration showed no noticeable curvature effects compared to other sources of variability.

Finally, temperature was found to induce a severe curvature increase of single metals and stacks when a certain time-dependent temperature threshold was surpassed, which approximately ranged from 300-350 °C during 1 minute to 250 °C during 1 hour.

The present work will aid MEMS designers in assessing whether the analyzed CMOS-MEMS processes are suitable for a given MEMS application. Also, the results and the characterization methodology presented herein are useful for MEMS designers who work with a similar manufacturing approach in order to shorten the development time and reduce the number of design iteration loops.

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Juan Valle was born in Lugo, Spain, in 1977. He received the M.Sc. degree in Physics in 2000 and the M.Sc. degree in Industrial Engineering in 2002 from Universidad Alfonso X El Sabio (UAX), Madrid, Spain. He received the International Master's in Theoretical and Practical Application of Finite Element Method and CAE Simulation in 2004 from Universidad Nacional a Distancia (UNED), Madrid, Spain.

From 2001 to 2002, he worked as a Microsystems (MEMS) and Nanotechnology consultant for the INTA (National Institute for Aerospace Technology). He specialized on Multiphysics simulations before joining Delphi Diesel Systems in 2004 as an Analyst Engineer, and joined Baolab Microsystems in 2005 where he researched on the fields of MEMS sensors and micromanufacturing processes for 9 years, where he filled 10 patent applications on related fields. Juan Valle devised design techniques applicable for the MEMS fabrication inside the CMOS BEOL. Using these techniques he is developing the first CMOS-MEMS 3 axis magnetometer aimed at mass production. Currently he is pursuing his Ph.D. in Electronic Engineering at Universitat Politècnica de Catalunya (UPC), Barcelona, Spain.

Daniel Fernández was born in Barcelona, Spain, in 1979. He received the M.Sc. degree in telecommunications engineering, Ph.D. degree (cum laude), and M.B.A. degree from Universitat Politècnica de Catalunya (UPC), Barcelona, Spain, in 2004, 2008 and 2009, respectively.

From 2008 to 2010 he worked as a Postdoctoral Researcher at the Electronic Engineering Department, UPC in the fields of CMOS surface micromachining, circuits and control architectures for MEMS sensors and actuators, translinear circuits for analog signal processing and digital implementations of power converters. From 2010 to 2014 he worked as Principal ASIC Engineer at Baolab Microsystems developing circuits and architectures for CMOS MEMS/NEMS-based products, and as ASIC Design Engineer Contractor for the European Space Agency designing radiation-hardened integrated-circuits and interface blocks for space exploration in interplanetary missions. Currently he is Chief Technology and Science Officer at Nanusens, Bellaterra, Spain, where he works towards the development of innovative circuits and architectures for MEMS sensors signal-conditioning.

Jordi Madrenas Jordi Madrenas (Telecom. Eng. '86, Ph.D. '91, UPC, Barcelona, Catalunya, Spain) is currently Associate Professor at the Department of Electronic Engineering, Technical University of Catalunya (UPC BarcelonaTech). He has participated in 5 European projects and coordinated 5 Spanish national research projects. Also, he has coordinated several contracts with companies. At present, he coordinates a national project on MEMS-on-chip and microsensor bio-inspired signal processing. He has co-authored more than 120 scientific journal and international conference papers, two books and 5 book chapters. Between 2000 and 2003 he was Vice-Dean of Studies of the Telecommunication Engineering School of Barcelona, UPC. His current research interests include analog, mixed-signal and digital VLSI and FPGA design, CMOS-MEMS design and conditioning, ultra low-power design, bioinspired/neuromorphic system implementation and rad-hard mixed-signal circuits.

Laura Barrachina Laura Barrachina was born in Pamplona, Spain, in 1981. She received the M.Sc. degree in Physics in 2004 from Universidad de Zaragoza, and Master of Advanced Studies in Microelectronics from Universidad de Barcelona, Spain.

She joined the National Microelectronics Center in Barcelona for 2 years, where she worked developing a methodology to design a MEMS by modelling in VHDL-AMS a 3-axis accelerometer. From 2006 to 2014, she worked at Baolab Microsystems as a Test and Measurement engineer, performing automated measurements at wafer level, specializing in MEMS sensor characterization. Since 2014, she is working at Owlstone, Cambridge, as a System Engineer in chemical detectors based on field asymmetric ion mobility spectrometry.